Adiabatic Charging in SAR ADCs

Dem Fachbereich Physik, Elektrotechnik und Informationstechnik

der Universität Bremen

zur Erlangung des akademischen Grades einer

DOKTOR-INGENIEUR (Dr.-Ing.)

genehmigte Dissertation

von

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Eingereicht am:	13.02.2024
Tag des Promotionskolloquiums:	02.04.2024

Abstract

Successive Approximation Register (SAR) is an established and well-rounded (Analog-to-Digital Converter) ADC architecture allowing for medium resolution and medium conversion speed while being energy efficient and relatively small in area. Switched-capacitor (Digital-to-Analog Converter) DAC being an essential component of the SAR architecture in certain design configurations might contribute significantly to the overall ADC power consumption. Adiabatic capacitor charging is a method that allows for increasing the charging efficiency using linear voltage or constant current to charge a capacitor. A variation of this approach uses a series of small voltage steps instead of a voltage ramp, which is particularly suitable for switched-capacitor circuits as it does not require analog circuitry such as a voltage ramp generator or a current source.

This work investigates the stepwise capacitor charging approach applied to DAC in SAR ADC in terms of the architectural modifications and their influence on the resulting efficiency improvement.

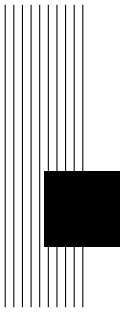
The study begins with an estimation of the stepwise charging applied to a conventional DAC switching scheme. The average energy consumption is derived as a function of the number of charging steps and resolution, the results are verified in MATLAB. For the implementation of the approach, other switching schemes were considered, the selected monotonic switching scheme was then also modelled in MATLAB to evaluate the efficiency improvement depending on the number of charging steps in that case. Stepwise charging requires several intermediate voltage levels in addition to the regular reference voltage. The work includes the discussion and implementation of the onboard DC-DC converter and the MATLAB model includes its influence on energy savings, allowing for a design optimization as well as the selection of the converter's configuration in regards to the number of charging steps, resolution, and DAC unit capacitor size.

Finally, the work describes a fabricated IC with two proof-of-concept ADC prototypes featuring 4-step charging applied to a 10-bit monotonic SAR ADC. The circuits differ in terms of the DAC capacitance and conversion speed. The first prototype has a sampling rate of 165 kS/s and achieves SNDR of 57.63 dB. The

second prototype has a sampling rate of 1 MS/s and achieves SNDR of 56.52 dB. The architecture is designed with separated circuits for the SAR register and adiabatic charging control logic in order to better differentiate the control logic penalty related to stepwise charging. To further identify the power savings in both prototypes, the 1-step versions of each prototype with adiabatic circuitry removed from the layout are simulated in CAD and compared to the 4-step counterparts. The evaluation of the first prototype shows a 26% reduction of the DAC power consumption including all the extra circuitry, whereas the second prototype establishes the limitation of the approach where the energy savings were overpowered by the control logic penalty and DC-DC converter switching losses. The work discusses this limitation in detail describing the applicability area of adiabatic charging. The proposed method allows the inclusion of these types of losses to optimize the configuration and estimate the benefits of the adiabatic switching in each case.

Acknowledgement

I would like to express my endless gratitude to Professor Steffen Paul. This work would not have been possible without his patient guidance, help, and expertise.
I would also like to thank Professor Björn Lüssem, Professor Alberto Garcia-Ortiz, and Professor Andreas Bahr for their very valuable insights and suggestions.
Special thanks to the current and past ITEM members: Dr. Osipov and Dr. Peters-Drolshagen, Ludwig, Maike, Moritz, Pascal, Nils, Hao, Lars, and Max for being there and creating such a positive atmosphere. Additional thanks to the department secretaries, Alexandra and Kerstin, for their hard work, support, and positivity.
I am extremely grateful to my wife, Anastasiia, for embarking on this journey abroad with me and being always by my side.
Finally, I would like to thank my friends and family, whose support is priceless and foundational to all my achievements.



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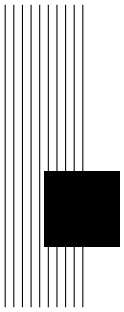


List of Abbreviations

ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

DNL Differential non-linearity

ENOB Effective Number of Bits

FFT Fast Fourier Transform

INL Integral non-linearity

LDO Low-Dropout Voltage Converter

LSB Least Significant Bit

MSB Most Significant Bit

ODE Ordinary Differential Equation

PDK Process Design Kit

PVT Process, Voltage, and Temperature

RHP Right Half-Plane

RMS Root Mean Square

SAR Successive Approximation Register

SC Switched Capacitor

SFDR Spurious-free Dynamic Range

SNDR Signal-to-Noise-and-Distortion Ratio

SNR Signal-to-Noise Ratio

SoC System on a Chip

SPICE Simulation Program with Integrated Circuit Emphasis

THD Total Harmonic Distortion

1 Introduction

1.1. Motivation

ADCs are used in many electronic devices, including those in the Internet of Things category, wearables, advanced driving-assistance systems, and more. Practically any electronic device that interacts with the outside world must have the means to digitize the signals before processing the data. The signals from proximity sensors, light sensors, gyroscopes, and microphones are not processed directly in their analog form but rather in the digital domain. The wireless communication receivers depending on their architecture may also require an ADC to demodulate the signal.
Since many such systems are not stationary and often battery-operated, the electronic circuitry requires close attention to energy efficiency and ADCs are not an exception.

1.2. ADC overview

The type of ADC determines its performance in terms of area, power consumption, resolution, and speed. This overview covers three of the main types of Nyquist-rate ADC architectures and two architectural constructs that combine ADCs of the same or different architectures to enhance performance. Beyond that, there are as well other conversion principles such as Sigma-Delta modulation, oversampling, and noise shaping.

1.2.1. Flash ADC

Flash ADCs are among the fastest converter architectures. Due to their parallel conversion mechanism, they require only one clock cycle to digitize the signal. In flash ADC the input signal is compared to multiple equally distributed voltage levels provided by a resistive ladder as shown in Figure 1.1.

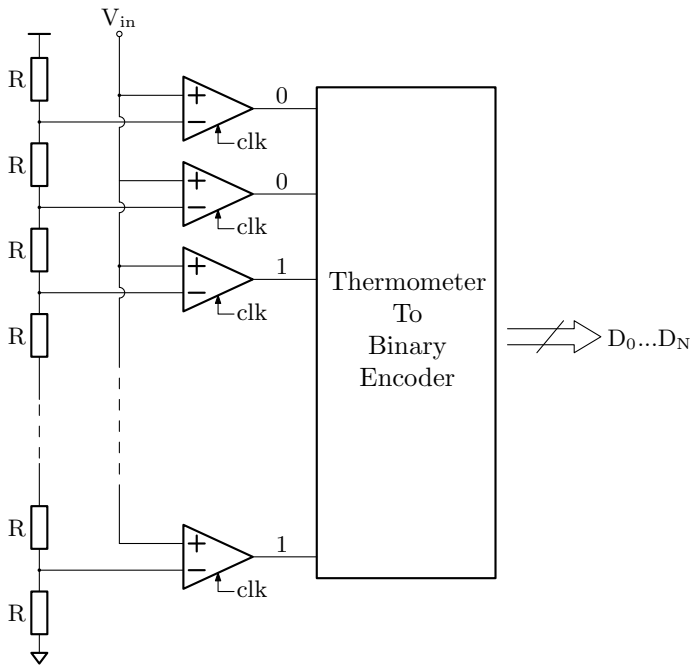


Figure 1.1.: Flash-ADC

The conversion is then performed by dynamic comparators whose combined outputs represent a thermometer output code. All the outputs where the input signal exceeds a certain level on the resistor ladder are the logic ones and the rest are the logic zeroes. To convert this output to binary-weighted code, the output encoder is required.

While the speed of the flash ADCs is very high, this architecture is difficult to scale up in terms of resolution. The number of required voltage levels, and therefore, comparators, grows twice with every extra bit of the binary output code, making the power consumption and area impractically large. The large number of comparators also increases the input capacitance that is signal-depended, thus introducing harmonic distortion. Due to these limitations, traditional flash converters usually have a resolution below 6-bit [Pel22].

1.2.2. Digital Ramp ADC

Digital ramp ADC (Fig. 1.2) converts the input signal by gradually increasing the built-in DAC voltage until it reaches the sampled value. At that point, the comparator changes its output state, thus indicating that the current counter's value matches the output code within the quantization error.

Opposite to flash converter, the digital ramp configuration occupies a significantly smaller area in exchange for a slower conversion rate due to the requirement of 2^N clock cycles for the ramp generator to gradually reach the full-scale voltage.

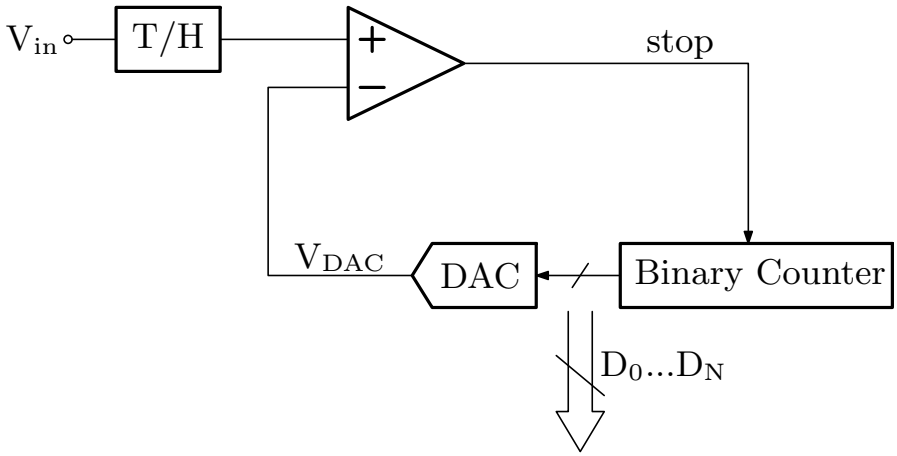


Figure 1.2.: Digital ramp ADC

1.2.3. Successive Approximation Register ADC

SAR ADC has a similar structure to one of the digital ramp, however instead of generating a voltage ramp, it uses the binary search algorithm to control the DAC. The ADC compares DAC bits with the sampled input signal sequentially, from MSB to LSB, thus requiring N cycles for N-bit binary search. Additional 2-3 clock cycles are also necessary to provide reset, sample/hold, and output code transfer. The use of the binary search algorithm significantly improves the conversion rate compared to the digital ramp ADC which requires 2^N clock cycles.

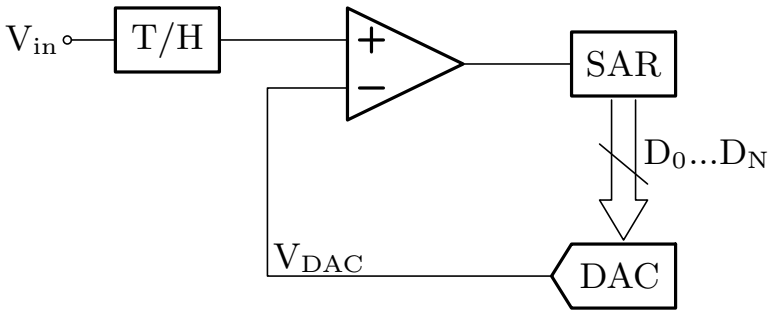


Figure 1.3.: SAR ADC

In modern CMOS processes advanced SAR ADCs can achieve hundreds of megahertz conversion rates [Pel22]. Generally, that type of ADC is used for a resolution of 8-14 bits and conversion speeds in the broad range of approximately 100kS/s-100MS/s [TLS+22].

From a power consumption standpoint SAR ADCs offer a good compromise between the speed, resolution, and power consumption, making them one of the most versatile ADC architectures.

1.2.4. Pipelined ADC

Pipelined ADC architecture uses several stages connected in series to evaluate several bits of the input signal at a time. A simplified pipelined ADC circuit is shown in Figure 1.4. Every stage has a fast built-in ADC such as flash [Ahm10] resolving the first m bits. The evaluated code is then restored using the DAC and subtracted from the input signal. The resulting residue is then amplified to accommodate the input range of the next stage where the next m bits are evaluated.

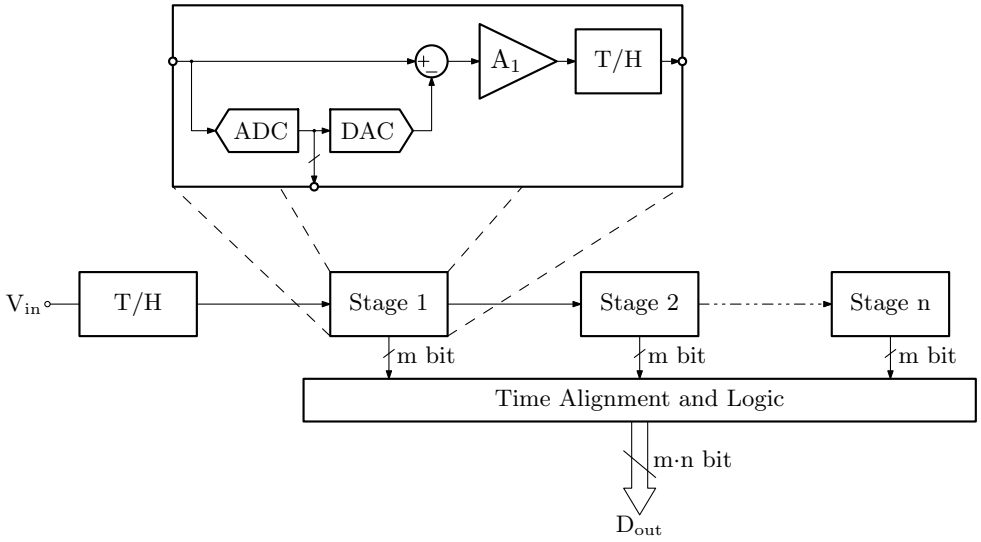


Figure 1.4.: Pipelined ADC

Pipelined architecture has an increased latency due to several stages that should finish the conversion for the signal to reach the last stage and complete the output code. However, the overall conversion speed is high because it is limited by the conversion speed of a single stage, which in the case of a flash-type ADC stage is only 1 clock cycle. Once the first stage has finished the conversion, during the next clock cycle the result is passed down the pipeline while the input stage starts converting a new sample.

Pipelined architecture reaches higher speeds than the SAR ADC. Unlike flash ADC pipelined architecture is significantly more compact while maintaining high conversion speed. Trade-offs of this architecture are latency and power consumption being larger than that of an SAR ADC.

Pipelined architecture provides a good platform for hybridization. Combining different types of ADCs in pipelined stages balances the benefits and the trade-offs creating a well-rounded design for a specific application. SAR-assisted pipelined ADC [JZZ+19, CWH+18] in particular can reduce the power consumption com-

pared to a traditional pipelined ADC while increasing the conversion speed and reducing the area of traditional SAR.

1.2.5. Time-interleaved ADC

Time interleaving is a technique used to improve the conversion rate of energy-efficient and slow ADCs [Pel22]. By using multiple demultiplexed ADC cores as shown in Figure 1.5, higher speeds can be achieved, while the power consumption grows at almost the same rate as the speed. That compromise is worthwhile for high-speed ADCs: for the same resolution, the power consumption of a single ADC often grows at a higher rate when increasing the conversion speed due to increased complexity.

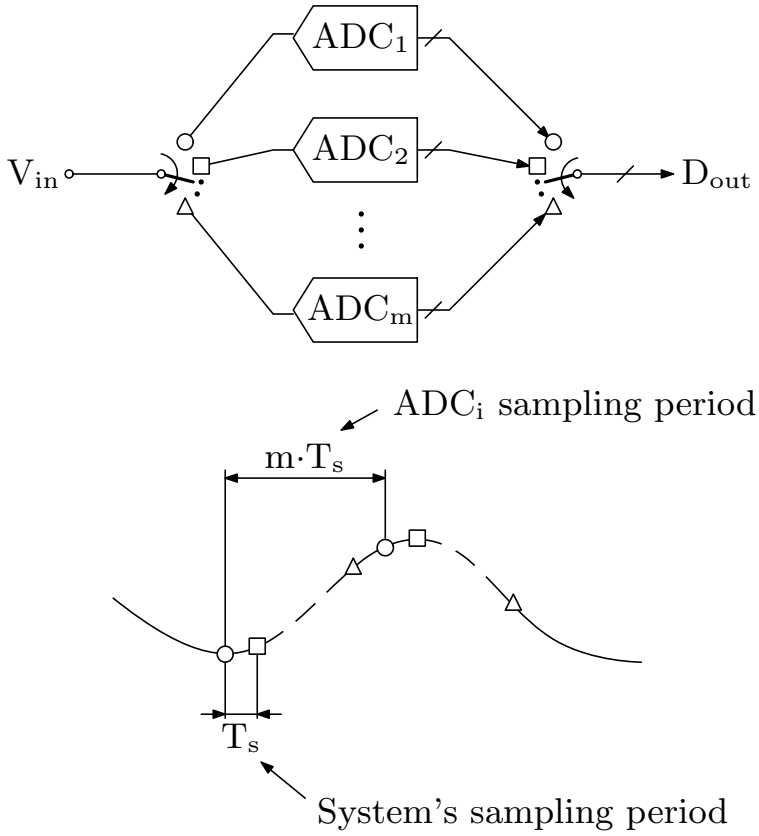


Figure 1.5.: Time-interleaving of several ADCs increases system's sampling speed

2 SAR ADC

2.1. Binary Search

The SAR ADC converts analog signal to digital using the binary search algorithm. The generalized binary search approach is a strategy to locate a certain value within a given array by comparing it with the mid-value, to identify the half of the array in which it is located. If the value is larger than the mid-value, then the cell of interest is located in the right (larger) half of the array. If the value is less, then it is located in the left half. The algorithm continues to compare the value of interest to the mid-values of the identified parts of the array. This approach is illustrated in Figure 2.1. In the case of an SAR ADC, the set of input

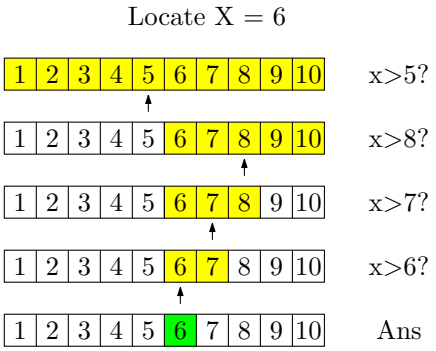


Figure 2.1.: Binary search procedure

voltages is infinite and not presented in the array as an exact value. The binary search is therefore used not to locate, but to assign the input to the closest value in the array. A DAC in SAR ADC is used to generate the reference values for comparisons.

The input signal in most SAR ADCs is sampled directly on the capacitive DAC, and therefore, instead of using the DAC only to generate a predefined set of reference voltages, the switched-capacitor DAC (SC-DAC) is used to add or subtract the binary weights from the sampled signal by charging or discharging corresponding capacitors. The binary search procedure above is therefore not

implemented as "x>$V_{mid-value}$?" but as "x-$V_{mid-value}$>0?".
The set of mid-values subtracted by the N-bit binary-weighted DAC is represented by "weights" ranging from the most significant bit (MSB) = 2^{N-1} - the middle of the complete code array, down to the least significant bit (LSB) = 2^0=1. Another

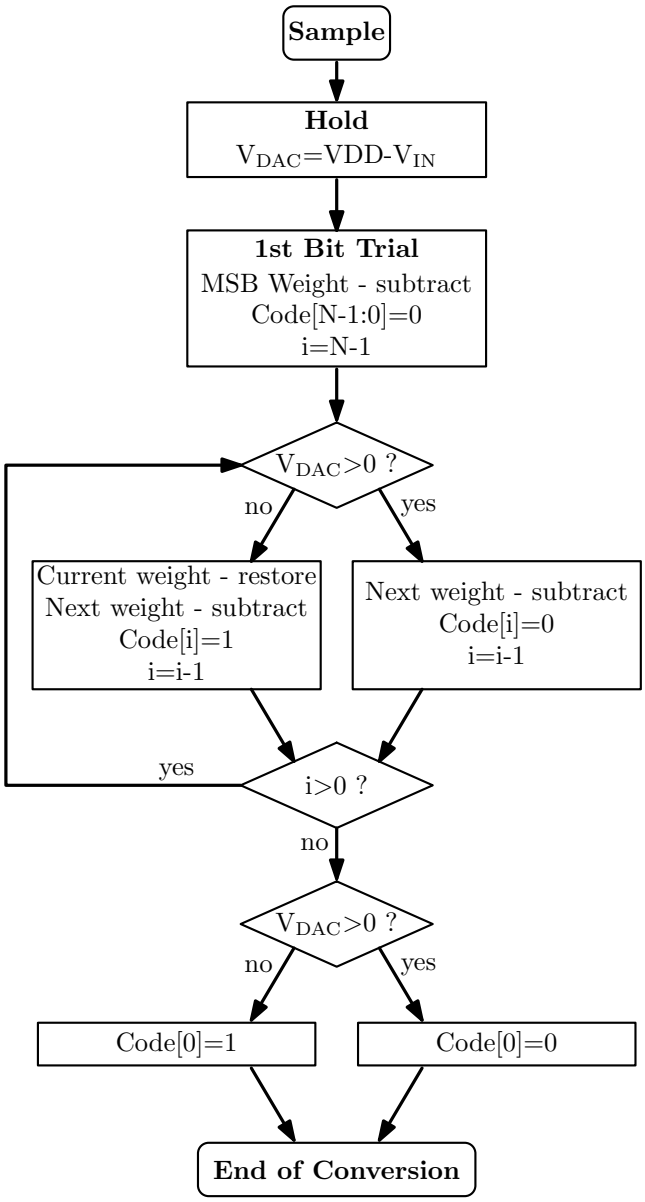


Figure 2.2.: N-bit SAR ADC binary search procedure block diagram

modification of the binary search when applied to a conventional SAR ADC is the sampling procedure. Conventional SAR ADC tracks the input signal from the bottom plate of the capacitor, while the top plate is connected to the ground node. The reason for that will be explained further in Section 2.2. After sampling, it switches to the hold mode, where the top plates are disconnected from the ground, and the bottom plates are set to VDD. Effectively this makes the value X undergoing the binary search equal to VDD-V_{IN}, whereas the actual value of

interest should be V_{IN}. In other words, for V_{IN}=VDD, the sampled value will be 0V, and for the V_{IN}=0, it will be VDD. To compensate for that, the output code is inverted which makes the conversion results match the input voltage. The block diagram of the resulting procedure is shown in Fig 2.2. The described algorithm

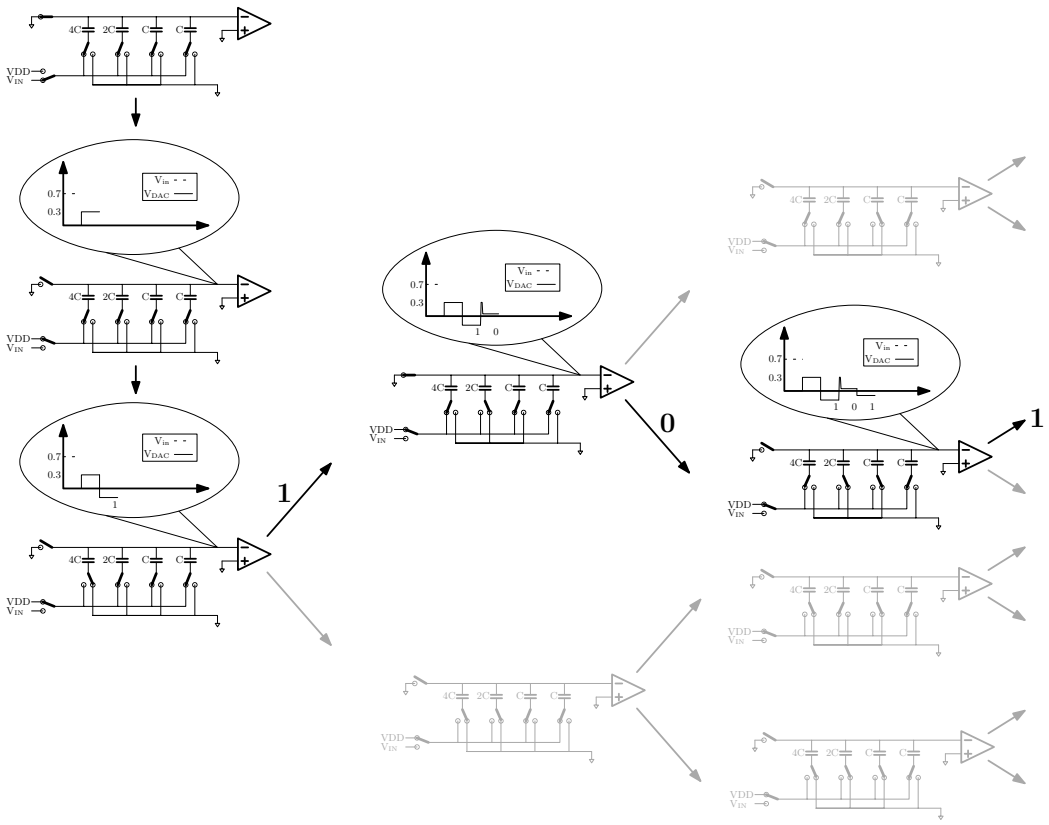


Figure 2.3.: Conventional 3-bit SAR ADC conversion tree

as performed by the 3-bit ADC is illustrated in Figure 2.3. Here, the complete conversion tree is shown with one of the branches highlighted. The supply voltage in the given example is equal to 1V and the input voltage equals 0.7 Volt. After the sampling, the top plates of the DAC disconnect from the ground node, the input switches set to VDD making the DAC output voltage equal to 1V-0.7V=0.3V. Then, the first 0.5V weight (MSB) is subtracted, changing the DAC voltage to -0.2V. The comparator's decision at this step results in the first code value: "1". According to the block diagram, DAC is then restoring the MSB weight back (shown on the waveform as a spike), and subtracting the next 0.25V weight from the sampled voltage, making the DAC output equal to 0.05. The result for the second bit therefore is "0". The last switching is then a simple subtraction of the 0.125V (LSB), leaving the final DAC output voltage equal to -0.075V, resulting in the LSB code of "1". The resulting output code is then "101".

2.2. Top- and Bottom-plate sampling, Charge injection

One of the issues that cause sampling and conversion errors in switched capacitor circuits is the charge injection. Charge injection, as the name suggests, is an effect when the charge is injected into (or withdrawn from) the storing capacitor causing a change in voltage. This happens due to the parasitic capacitances built-in within the switch. The condition for charge injection to happen is a resistive path from the opposite plate of the capacitor to a low-impedance node such as a voltage source or ground (Fig. 2.4).
If both plates of a capacitor have a switch connected to them, a charge injection occurs when the switch on one plate turns off, and the switch on the opposite plate is still connected to a voltage source.

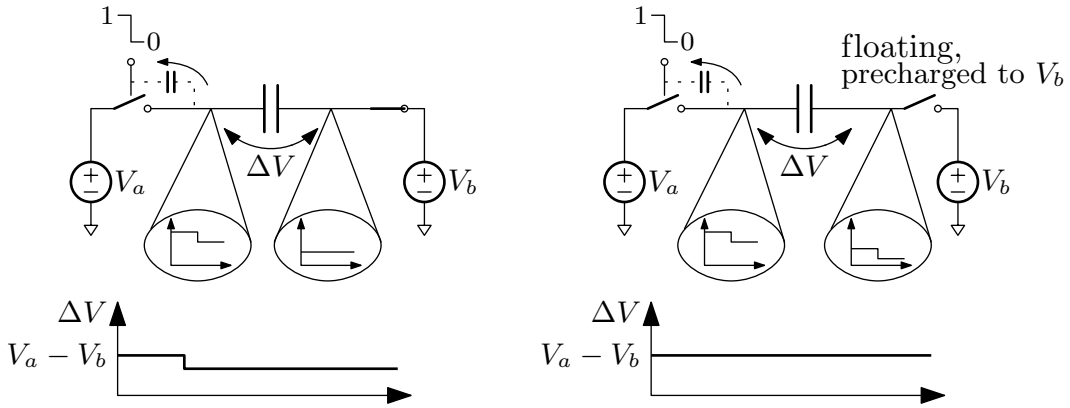


Figure 2.4.: Charge injection occurs (left), no charge injection (right)

The injected charge in the case of a single MOSFET switch can be expressed with Eq. (2.1), [Bak10], where Vth can be expressed as (2.2):

$$Q = C'_{ox} \cdot W \cdot L \cdot (V_{gs} - V_{th}) \tag{2.1}$$

$$V_{th} = V_{th0} + \gamma(\sqrt{|2V_{fp}| + V_{sb}} - \sqrt{|2V_{fp}|}) \tag{2.2}$$

The dependence of the charge Q on V_{gs} means that it depends on the input voltage, which produces the gain error. The dependence of threshold voltage V_{th} on the source-bulk voltage V_{sb} translates to the V_{th} dependence on the input voltage, thus introducing nonlinearity and harmonic distortion into the system.
If the first switch to disengage in a sampling sequence is a switch to the reference voltage or ground, the charge injection only happens at this transition. This makes V_{gs} and V_{sb} of this switch independent from the input voltage, thus introducing only DC offset without non-linearities. This approach called bottom-plate sampling

is shown in Fig. 2.5.

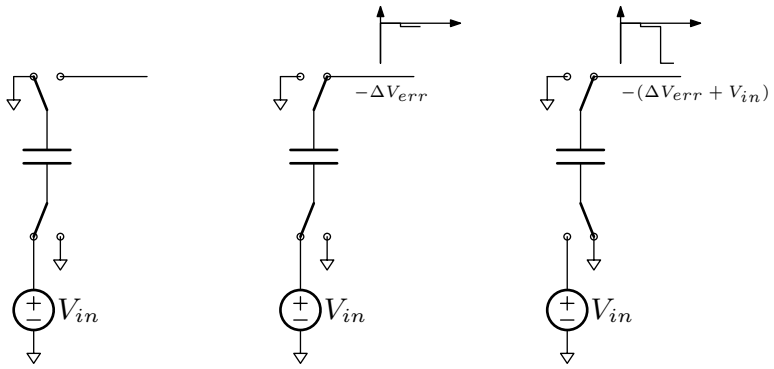


Figure 2.5.: Bottom-plate sampling

Charge-injection-related errors can also be reduced by optimizing the switches rather than the sampling sequence. A dummy or a complementary switch can be used for that purpose. A dummy switch (Fig. 2.6, left) is a transistor with the source and the drain connected together. It is controlled by the inverted clock signal, allowing it to intercept the charge from the main switch. The dummy switch has to be two times smaller due to the total parasitic capacitance of the dummy switch $C_{gs,dummy}+C_{gd,dummy}$ being required to match with only the C_{gs} of the main switch.

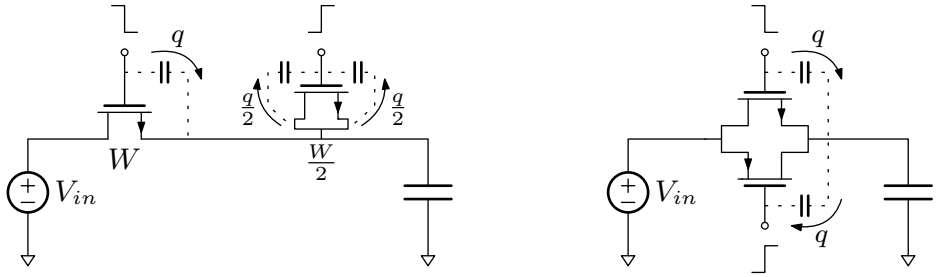


Figure 2.6.: Dummy switch (left), Complementary switch (right)

A complementary switch (Fig. 2.6, right) consists of a pair of NMOS and PMOS transistors. The opposite polarity of the PMOS clock allows it to cancel out some of the charge injected by the NMOS. Additionally, this type of switch has better transmission performance since at least one of the transistors remains open within the entire range of V_{in} from GND to VDD. Whereas a single MOS switch is not able to cover the full range of the input signals (e.g. V_{in} near and above VDD-V_{th} will not provide a sufficient V_{gs} for a simple NMOS switch to open). Nonetheless, the charge injection canceling effect of a complementary or a dummy switch is hard to maintain due to the strict timing requirements for inverted clock signal over the range of corners and temperatures.

Another design called bootstrapped switch is shown in Fig. 2.7. Similar to the

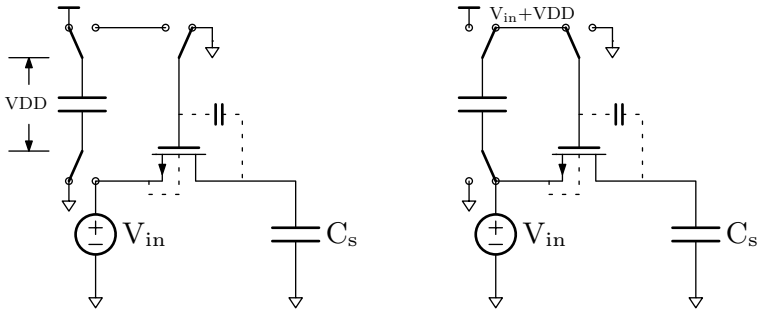


Figure 2.7.: Bootstrapped switch

bottom-plate sampling, it is aimed to keep the charge injection constant across the input voltage range rather than reduce it. This way produced voltage change will not introduce harmonic distortion. The introduced static distortion can further be canceled out using a differential architecture.

The way the constant charge injection is achieved is by applying the gate voltage that is always higher than the input voltage by the same VDD value. First, a capacitor is charged between VDD and GND, then the bottom plate is connected to the input, and the top plate is connected to the gate of the NMOS transistor. This makes V_{gs} of the NMOS always equal to VDD. If the process allows, connecting the bulk terminal to the source will also keep V_{sb} constant. Together, this makes the injected charge Q independent from the input voltage as can be seen from the eq. (2.1)-(2.2). The second-order effects, however, will still limit the bootstrap switch performance. Advanced design techniques allow resolution of up to 16-bit [BSK+11].

2.3. Switching scheme efficiency and SoA

During the binary search procedure, SC-DAC subtracts or adds successively reducing binary weights to the sampled voltage throughout the conversion steps. Various switching schemes are aimed to optimize the energy efficiency of that process. The benefits of other switching schemes over a conventional approach can be demonstrated using an example in Fig. 2.8. The figure shows the comparison between a 2-bit conventional and split-capacitor array [GC07] DAC down-transition. In the conventional DAC (Fig. 2.8, top), in order for it to decrease the voltage, it is required to simultaneously switch the previous bit (C_2) down and the next bit (C_1) up. The split-capacitor array switching scheme has the MSB split into two capacitors $C_{2,0}$ and $C_{2,1}$. Therefore, for the down transition, it is only required to switch one of the halves of MSB down which requires 5 times less energy. This approach reduces the overall DAC switching power by 37% compared to the conventional scheme. Additionally, it improves settling time and is more robust against mismatch.

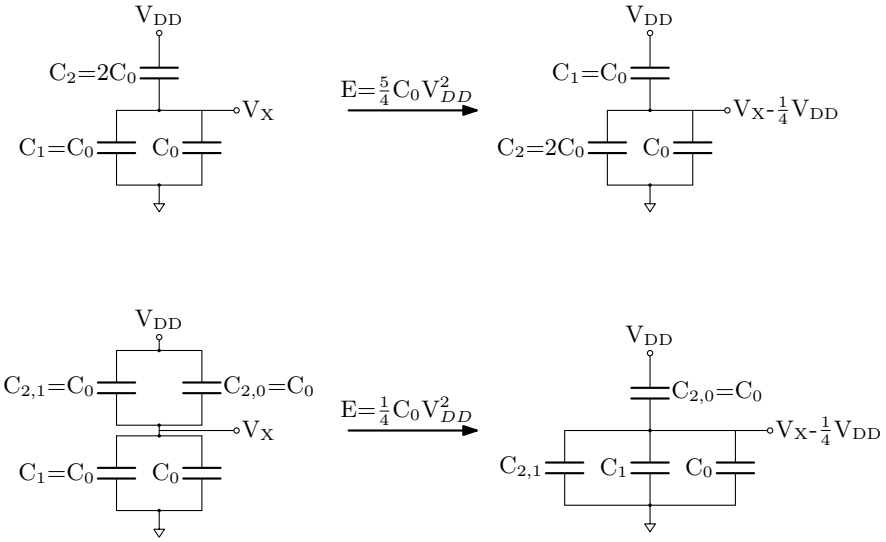


Figure 2.8.: Down transition of a conventional DAC (top) and Split-DAC (bottom). Image recreated from [GC07]

A number of other switching schemes were proposed over the years. Many of them require an additional common-mode voltage source V_{CM}=1/2V_{REF}. The introduction of the extra reference voltage V_{CM} broadens the variety of possible DAC capacitor commutations enabling various energy-efficient charging techniques. A good overview of published switching schemes was presented in [CZT19]. Table 2.1 shows a comparison between the switching schemes in terms of the switching energy, reset energy, and sensitivity to the intermediate voltage accuracy. The switching schemes that only use one reference voltage and ground are marked with

a dash in the according column. The table shows a significant amount of switching schemes that rely on an additional intermediate voltage source to reduce energy consumption. Besides schemes such as [ZCC+10] where the common-mode voltage source is always symmetrically present and doesn't affect the differential voltage at all conversion cycles, the scheme reported in [YKS16] requires V_{CM} to be stable even though the nominal voltage is not required to be precisely $1/2V_{REF}$. Many other switching schemes show sensitivity to the accuracy of the common-mode voltage ratio to V_{REF}, which also implies that the voltage source must be stable and accurate. This, in turn, puts extra requirements on the system level. The design of a highly efficient and stable reference voltage source for such applications is challenging, and there is also a trade-off between power consumption, accuracy, and speed.

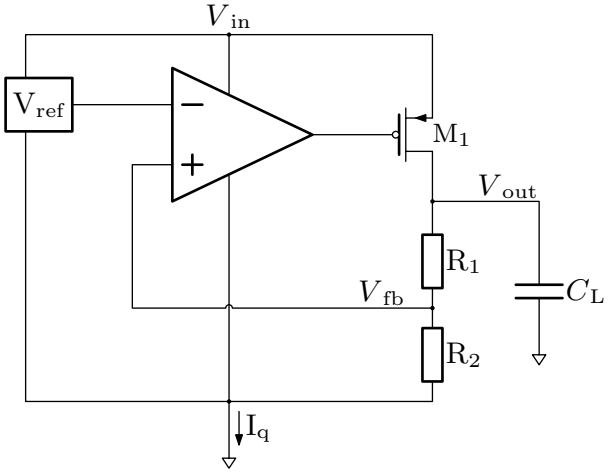


Figure 2.9.: Traditional PMOS-pass transistor type LDO circuit diagram

A Low-Dropout (LDO) Voltage Converter is a common choice for such applications. The circuit (Fig. 2.9) consists of a pass transistor controlled by an error amplifier. The operational amplifier equalizes both its inputs due to the large open-loop gain, making the feedback voltage V_{fb} close to V_{ref}. This sets the current through R_2 and consequently through R_1 as well. The output voltage V_{out} is therefore determined by the R_1/R_2 ratio.
The efficiency of the conversion η is directly proportional to the ratio between V_{out} and V_{in} (2.3), and further degrades with increasing of the quiescent current I_q.

$$\eta = \frac{I_{out}V_{out}}{(I_{out} + I_q)V_{in}} \cdot 100\% \tag{2.3}$$

In the case of direct conversion from V_{DD} to V_{CM}=$V_{DD}/2$, the maximum theoretical efficiency is only 50% in an ideal case where $I_q = 0$.
Another challenge with using an LDO converter is the output voltage range.

Today's ADCs supply voltage lies in the range of 0.6 - 1.2V which translates into the V_{CM} range of 0.3 - 0.6V. The design of an LDO for such an input and output range is not trivial. Examples of such designs reported in [LLL+18, SWM17] show I_q values of 10-20 uA. For the power supply of roughly 1V that gives the DC power consumption of 10-20 uW. State-of-the-art ADCs can have a power consumption of less than 100 uW [LCH+10] and down to 0.2 uW [YC14, HCvR13b, HH18]. Therefore, the additional power consumption of an LDO can be comparable to or even higher than the power consumption of the whole ADC. Despite the design blocks that consume DC power being undesirable in the switched-capacitor circuits in general, such a large power consumption makes the LDO voltage source excessive unless the ADC is part of a larger SoC that requires an LDO for other purposes as well.
In addition, a large number of switching schemes is dependent on the intermediate voltage value being precisely a half of the reference voltage. The precision of this ratio influences the accuracy of such switching schemes to a certain degree. The majority shows sensitivity starting from the second or third-bit decision.
That makes switching schemes that are sensitive to the Vcm accuracy, such as [CZT19, DBZ16, LDLZ18], mode demanding on the system level due to potential calibration requirements to compensate for the Vcm conversion inaccuracy in high-resolution designs.
Generally, the drawbacks of the switching schemes fall into three categories:

- *extra power consumption on reset phase:* some of the switching schemes require a specific pre-charged DAC initial condition at the start of conversion. This step consumes extra power and therefore requires to be taken into consideration when estimating the efficiency of the approach. The importance of that can be seen in Table 2.1 in schemes of [XSW+17, LZ18, YKS16]: the reset energy in these cases is several times larger than the overall switching energy of the DAC.

- *extra logic complexity:* complex switching procedures increase the control logic gate count, which therefore can significantly increase the power consumption of the digital part of the ADC.

- *a requirement to use additional precise voltage sources:* as was previously described in an example with the LDO, the requirement to use an additional precise voltage source specifically for the ADC may require more energy on the system level than it would be saved by the switching scheme. This limits the application of the switching schemes with V_{CM} sensitivity in Table 2.1.

Switching scheme	**Avg. sw. en. ($C_0V_{ref}^2$)**	**Reset en. ($C_0V_{ref}^2$)**	**Total ($C_0V_{ref}^2$)**	**Sensitivity to $V_{cm}/V_{ref}=1/2$**
Conventional	1363.3	0	1363.3	no
Monotonic [LCH+10]	255.5	0	255.5	-
VCM-based [ZCC+10]	170.17	0	170.17	no
Tri-level [YL12]	42.42	0	42.42	From 2nd bit
VMS [ZXS13]	31.88	0	31.88	From 2nd bit
Sanyal and Sun [SS13]	21.3	95.75	117.05	From 3rd bit
Charge redistribution [YKS16]	31.88	117.2	149.08	no
Tong and Ghovanloo [TG15]	15.88	50.84	66.72	From 3rd bit
Xie [XSW+17]	21.2	121.2	142.4	Only LSB
Wu and Wu [WW17]	21.3	64	85.3	Only LSB
Tong [TC17]	15.88	83.59	99.47	From 2nd bit
Wang [WXCC19]	26.54	0	26.54	From 2nd bit
Liang [LZ18]	7.94	128	135.94	From 3rd bit
Asymmetric [LDLZ18]	13.53	0	13.53	From 2nd bit
Trade-off [DBZ16]	26.54	0	26.54	From 2nd bit
LSB split [GAS+17]	10.8	48.12	58.92	From 3rd bit
Vaq-based [HZC+21]	5.3	53.88	59.18	From 2nd bit
Yousefi [YDY18]	0	62	62	No
Two-Stage Mixed [CZT19]	2.9	0	2.9	From 2nd bit

Table 2.1.: Comparison of SAR ADC switching schemes [CZT19]

2.4. Noise in SAR ADC

2.4.1. Quantization noise

An ideal ADC accuracy is limited. The input voltage is assigned to a finite set of digital codes which can not cover the infinite amount of possible input voltage values. The relation between the output code and input voltage is shown as a transfer function in Figure 2.10 using a 3-bit ADC as an example. The horizontal axis is the normalized input voltage, and the vertical axis is the code. The dashed line represents the voltage ramp as it is applied to the ADC input. The difference

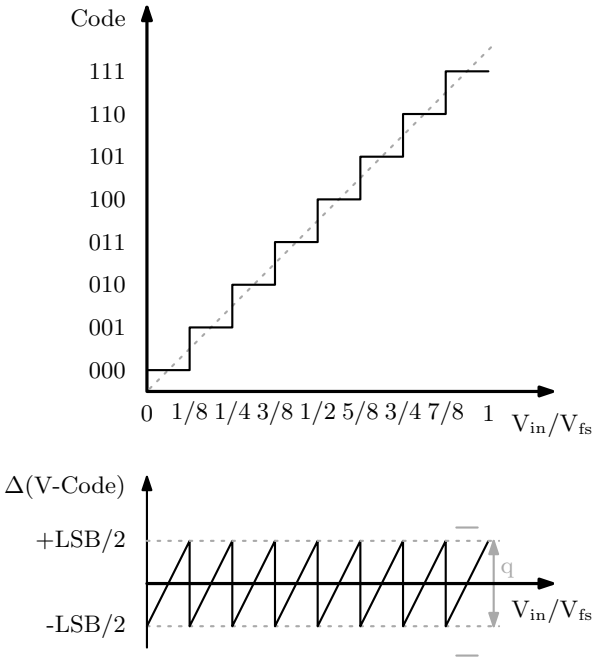


Figure 2.10.: ADC quantization error

between the voltage ramp and the output codes is shown at the bottom of Figure 2.10. The resulting error is a sawtooth waveform with the RMS value expressed as (2.4).

$$e_{rms} = \frac{q}{2\sqrt{3}} \tag{2.4}$$

To calculate the signal-to-noise ratio of an ideal ADC, the sinusoidal voltage is applied to the input. The RMS value of the input full-scale sinusoidal voltage expressed as 2^{N}LSB is shown in eq. (2.5):

$$V_{sine,\ rms} = \frac{V_{fs}}{2\sqrt{2}} = \frac{q \cdot 2^N}{2\sqrt{2}} \tag{2.5}$$

Calculating the SNR gives the following:

$$SNR_{dB} = 20\log_{10}\left(\frac{V_{sine,\ rms}}{e_{rms}}\right) = 20\log_{10}2^N + 20\log_{10}\sqrt{\frac{3}{2}} \tag{2.6}$$

$$SNR_{dB} = 6{,}02 \cdot N + 1{,}76\ dB \tag{2.7}$$

Equation (2.7) is also a measure against which the comparison between a real and an ideal ADC can be made. An ADC's non-idealities are expressed with the signal-to-noise-and-distortion ratio (SINAD). If SNR in the eq. (2.5) is replaced with SINAD, then N would represent the effective number of bits (ENOB) of the non-ideal ADC. Deriving the ENOB then gives:

$$ENOB = \frac{SINAD_{dB} - 1{,}76}{6{,}02} \tag{2.8}$$

2.4.2. Sampling noise

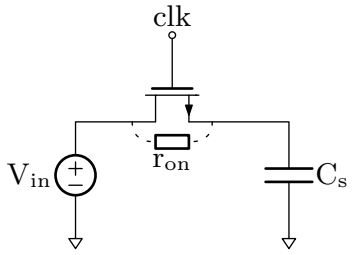


Figure 2.11.: ADC sampling noise

During the sampling, when the input switch is open, the combined finite switch resistance and DAC capacitance represent the low-pass filter. The total thermal output noise power generated is expressed as (2.9). The output noise does not depend on the resistance value but is determined by sampling capacitance. Choosing a unit capacitor's size so the noise power is below the quantization error power, determines the minimum unit capacitor's value for Nyquist-rate ADCs.

$$\overline{V}^2_{n,o} = \frac{kT}{C} \tag{2.9}$$

$$\frac{kT}{C} < e^2_{rms} \tag{2.10}$$

2.4.3. Comparator noise

The StrongARM comparator topology (Fig. 2.12) is among the most frequently used topologies for its absence of static bias requirements, high gain, and overall robustness. The operation of the circuit can be described using 4 phases [Raz15b]:

1st phase occurs when clk is high, $V_{x,y}$ and outputs $V_{on,\,op}$ are reset. The next three phases occur after the transition of the clock from high to low and are depicted in Fig. 2.12 as follows: first, the input transistors $M_{1,2}$ turn on, operating as a differential pair. Once the common mode at $V_{x,y}$ approaches threshold voltage $V_{th,p}$, the first two transistors of the latch $M_{3,4}$ begin to turn on, thus, raising the output voltage $V_{on,\,op}$. That, in turn, opens transistors $M_{5,6}$ which invokes the positive feedback and latches the output.

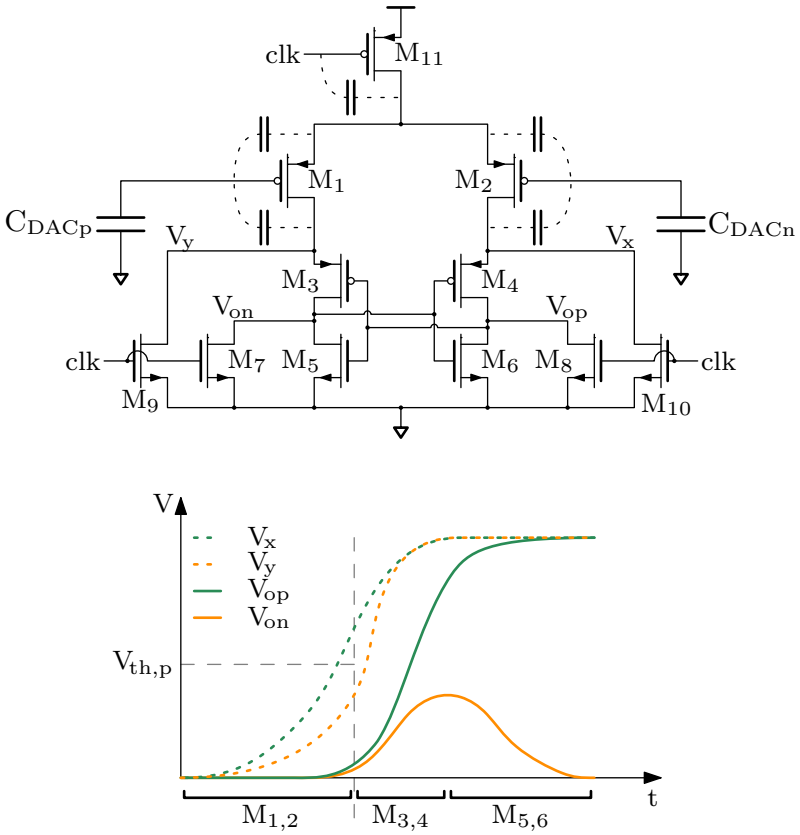


Figure 2.12.: StrongARM latch operation, redesigned for PMOS input transistors [Raz15b]

A change in the comparator's output voltage draws charge from the gate terminal of its input transistors through parasitic capacitances. This affects the capacitive DAC's charge and voltage. The parasitic capacitances involved in this process are shown in Fig. 2.12. This effect called kickback noise has differential and common-mode components. Common-mode kickback due to the tail transistor M_{11} drawing currents symmetrically from $M_{1,2}$ is usually dominant [Raz15b]. However, it can be canceled out by the differential ADC architecture. The non-dominant differential kickback is not canceled out that way and therefore it degrades the ADC accuracy. The differential kickback charge is mainly caused by the difference in slope at $V_{x,y}$ created during the phase when $M_{1,2}$ are active. A larger input voltage produces a larger difference in the slopes, thus increasing the error.

Apart from the kickback-induced DAC error, the comparator's accuracy is affected by thermal noise. During the amplification and metastability phase, voltage fluctuates due to noise prior to the latching, which can lead to a wrong comparator decision. The work [NDBTVdP08] reports that the noise is mostly contributed by $M_{1,2}$ via thermal noise and switches $M_{9,10}$ via the noise that they sample after the reset, contributing it into the nodes $V_{x,y}$, affecting the initial phase. Depending on the comparator's sizing, the contribution of $M_{1,2}$ in total output noise power varies from 39 to 56%, and the contribution of switches $M_{9,10}$ is 28-36%. The sum of both contributions in each sizing example varies from 75 to 83%.

2.5. Comparator offset

The mismatch between transistors in the left and right branches of the comparator in Fig. 2.12, as well as the difference in parasitic and load capacitances at the nodes $V_{x,y}$ and $V_{on,\,op}$, leads to the built-in difference in the slopes at the comparator's nodes $V_{x,y}$ and $V_{on,\,op}$. It requires a certain voltage difference to be applied to the comparator's input in order to overpower the built-in imbalance and restore the branches settling back to being symmetrical. The required input offset is inversely proportional to the comparator's gain A, eq. (2.11).

$$V_{os} = \frac{V_{os,out}}{A} \tag{2.11}$$

Measuring the latched comparator's offset requires taking the time resolution into consideration. Since the clock signal is necessary to make a comparison, there is an error component introduced when measuring an offset with a ramp input voltage. During the time between the clock cycles, the signal changes to a certain amount. Measuring the offset on both, rising and falling slopes of the ramp, and averaging the result cancels out this error as shown in Figure 2.13.

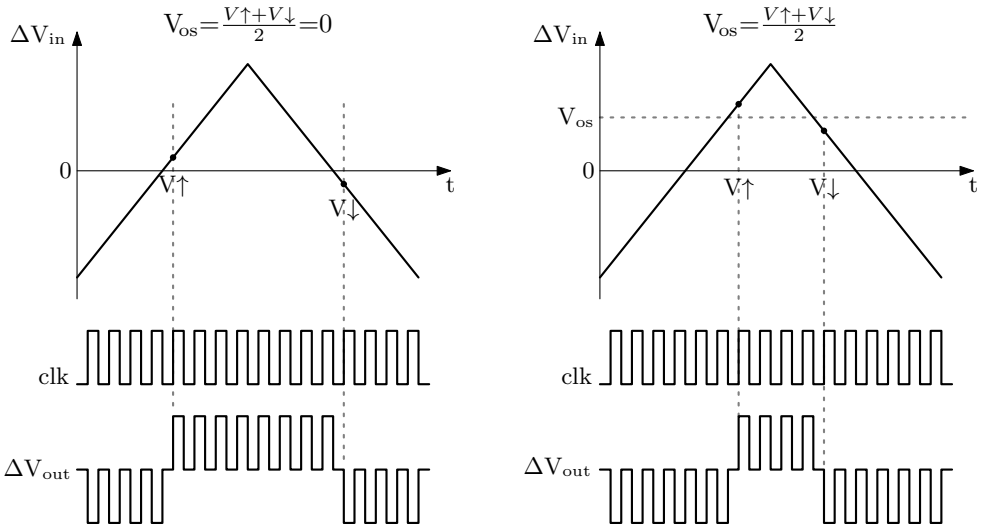


Figure 2.13.: Comparator's offset measurement with canceling out the resolution error

Figure 2.14 shows the input-referred offset equivalent circuit applied to the ADC. The offset can be represented as a DC voltage source connected in series to the ideal comparator, either as a true value to a positive input (Fig. 2.14, left) or as an inverted value to the negative input (Fig. 2.14, right). Depending on the sign of the offset, this value adds or subtracts from the input signal, causing a shift in the transfer function of the ADC (Fig. 2.15).

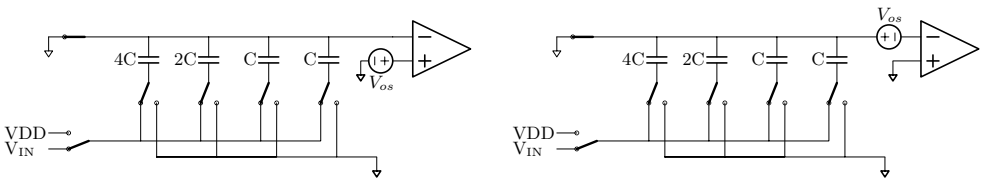


Figure 2.14.: ADC with comparator offset

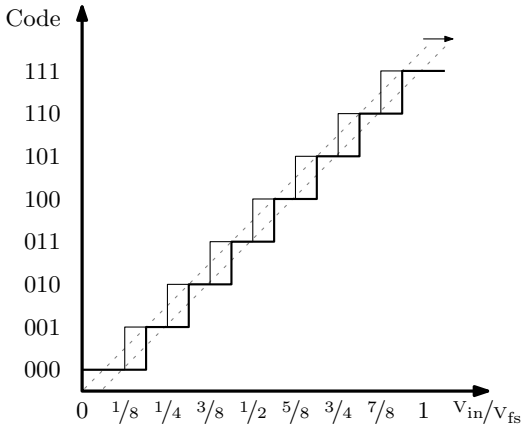


Figure 2.15.: ADC transfer function with static offset

A dynamic offset can further degrade the ADC accuracy: since the input-referred offset is dependent on the gain of the comparator, the shift in the transfer function is only equal for each code if the gain does not change. In switching schemes where the comparator input common mode voltage is not kept constant throughout conversion this introduces an additional source of error. Common mode variation alters the operating point at the comparator's inputs causing a change in gain during the amplification phase. The input-referred offset then becomes code-dependent and introduces non-linearities. The conventional single-ended switching scheme (Fig. 2.16, top) has this issue, whereas if used as differential architecture, it has a constant common mode voltage (Fig. 2.16, bottom).
Other more efficient switching schemes are often designed with varying common mode voltage. In these ADCs, the use of the biased comparator [LCHL10] reduces the errors related to the dynamic offset. Compared to the StrongARM latch, the biased comparator circuit (Fig. 2.17) has a current source M_8 that keeps the gate-source voltage of the input transistors constant across the range of the input common-mode voltages as well as controls the tail current. This makes the circuit more robust against gain variations with common mode voltage. The downside is a bias requirement that increases overall power consumption.

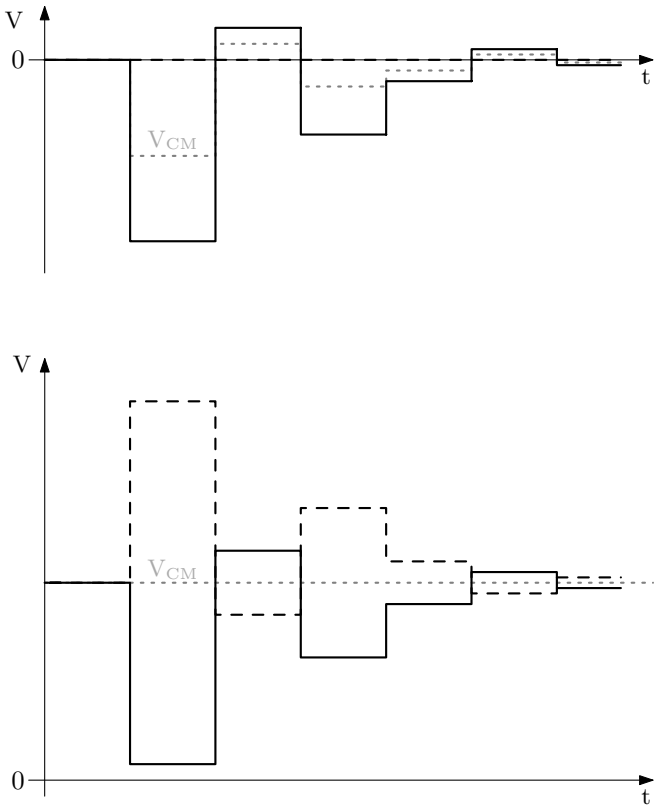


Figure 2.16.: ADC common mode voltage (dashed line) for a single-ended(top) and differential (bottom) conventional switching scheme.

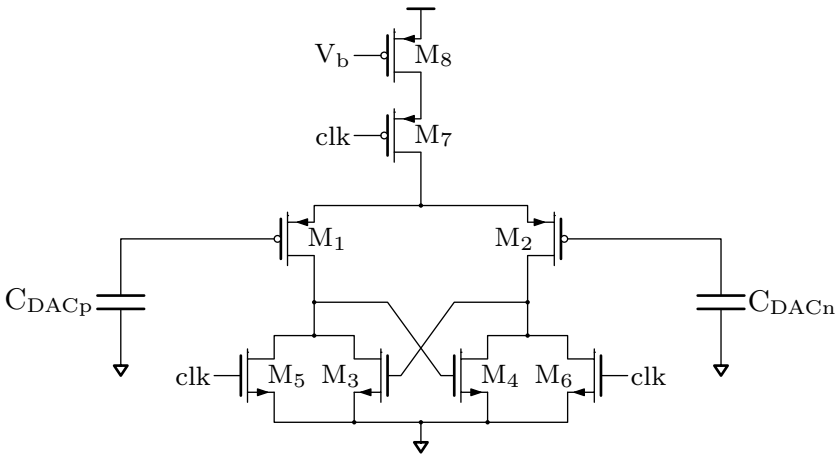


Figure 2.17.: PMOS biased comparator

2.6. Mismatch in the SC DAC

The mismatch in the SC-DAC is critical for ADC accuracy. Using an exaggerated example of 25% variation of the MSB capacitor in a 3-bit SC-DAC matrix, it can be seen from Fig. 2.18 how it affects the output voltage.

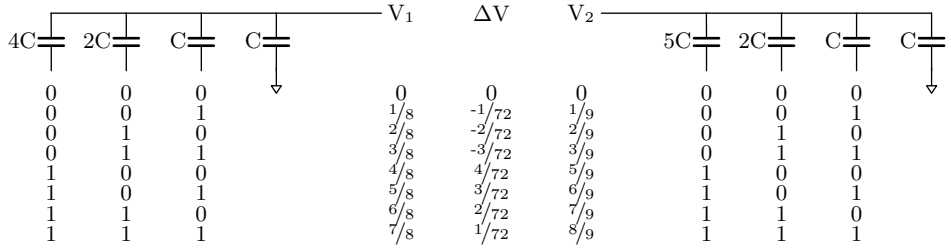


Figure 2.18.: DAC output voltage with MSB mismatch

The total capacitance of the matrix changes, increasing the common denominator and introducing gain error. The maximum output voltage changes accordingly. Compared to the original matrix, the largest voltage difference occurs during the 011 to 100 transition. Generalizing the output voltage in and including the mismatch gives the expressions (2.12)-(2.13) for these two codes:

$$^{01...11}V_{DAC,out} = \frac{C_{LSBs} + \Delta C_{LSBs}}{C_{LSBs} + C_{MSB} + \Delta C_{LSBs} + \Delta C_{MSB} + C} \tag{2.12}$$

$$^{10...00}V_{DAC,out} = \frac{C_{MSB} + \Delta C_{MSB}}{C_{LSBs} + C_{MSB} + \Delta C_{LSBs} + \Delta C_{MSB} + C} \tag{2.13}$$

Here, C_{LSBs} and ΔC_{LSBs} are the sum of all the nominal capacitances except the MSB, and the sum of all the errors in those capacitances accordingly. Similarly, C_{MSB} and ΔC_{MSB} are the nominal capacitance and the error capacitance of the MSB.

The mismatch applied to the ADC transfer function is shown in Figure 2.19. Compared to the ideal transfer function, the voltage steps are spread unevenly, which increases the error beyond the regular quantization error level. Differential non-linearity (DNL) and integral non-linearity (INL) are the metrics of the transfer function non-idealities. The differential non-linearity is a difference between the width of a voltage range for a certain code and the width voltage range of the ideal transfer function. The normalized DNL (2.14) is the DNL divided by the ideal code width [Pel22, Araa].

$$DNL_{b,LSB} \stackrel{\text{def}}{=} \frac{W_b - W_{ideal}}{W_{ideal}} \tag{2.14}$$

The width of code 011 is illustrated in Figure 2.19 as W_4. The ideal width W_{ideal} is the same across all the codes.

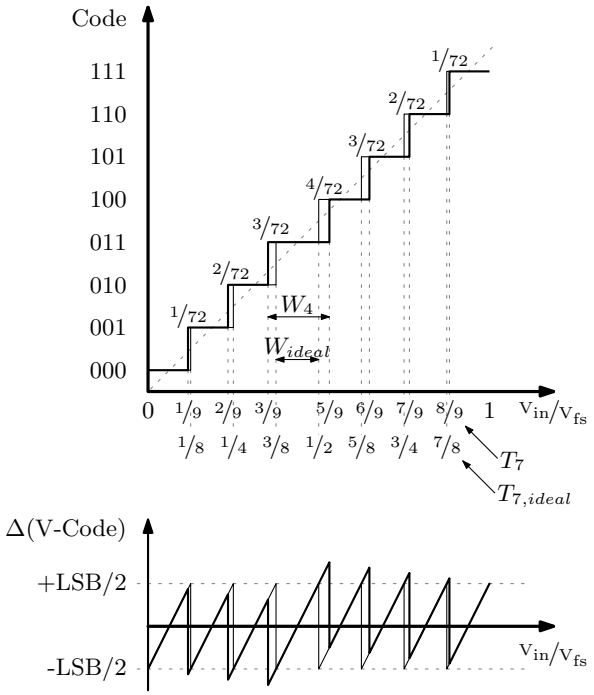


Figure 2.19.: ADC transfer function with MSB mismatch

The integral non-linearity is a difference between transition voltages of the current and ideal code. The normalized INL is then the INL divided by the ideal code width [Pel22, Arab] as shown in the eq. (2.15):

$$INL_{b,LSB} \stackrel{\text{def}}{=} \frac{T_b - T_{b,ideal}}{W_{ideal}} \tag{2.15}$$

It can be seen from Figure 2.19 that the transition voltage of a certain code is a sum of bit widths of the previous codes. Therefore, the INL of a given code can also be represented as a sum of DNLs of the prior codes as shown in eq. (2.16)

$$INL_{b,LSB} = \sum_{i=1}^{b-1} DNL_b \tag{2.16}$$

$$1 \leq b \leq 2^N - 1 \tag{2.17}$$

The mismatch-oriented sizing of an SC-DAC capacitor matrix assumes the choice of the smallest possible unit capacitor size that would still satisfy the DNL variation below a chosen value. For use in further calculations, the topology and indexing of a 3-bit binary weighted capacitor matrix are explained in Fig. 2.20. The matrix consists of the capacitors C_0- C_4: the active capacitors are C_1- C_3, and capacitor C_0 serves the scaling purpose, in order to make the common denominator equal to 8 and adjust the gain so the MSB voltage is exactly a half of the V_{ref}.
Switch control signals are labeled d_0-d_3, where d_0 is only required to provide

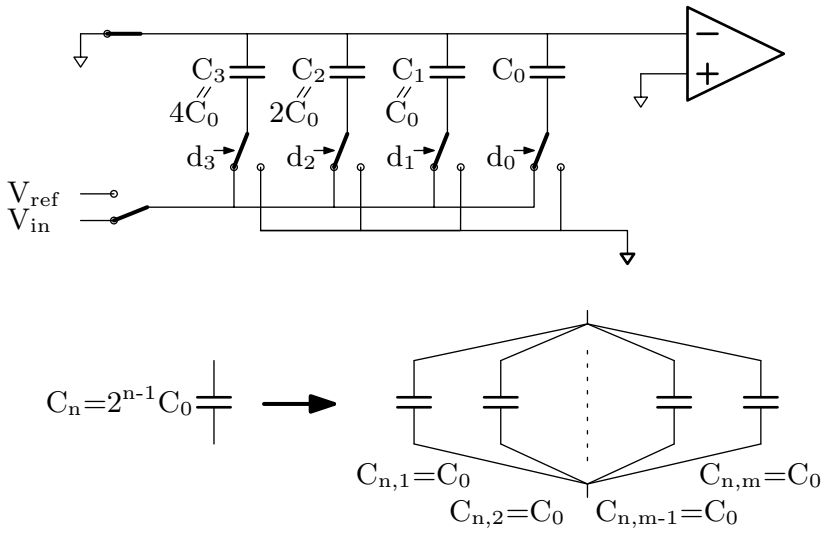


Figure 2.20.: Conventional SAR ADC

the bottom-plate sampling procedure: it is not involved in bit-decisions after sampling.

The capacitors larger than the unit capacitor are combined from a group of unit capacitors connected in parallel. The naming of each group (Fig. 2.20, bottom) is as follows: the n-th capacitor C_n with a capacitance of $2^{n-1}C_0$ consists of a 2^{n-1} unit capacitors connected in parallel, where each capacitor within the group is labeled from $C_{n,m}$, where m is in the range from 1 to n-1.

The approach of estimating the variance of the mismatch-induced error in binary-weighted DAC was described in [GC07]. Considering the mismatch in the SC-DAC from Fig. 2.20 and assuming that the deviation from the size of each unit capacitor has zero mean value and is independent, the size of the unit capacitor can be expressed as (2.18) where $C_{0,nom}$ is a target nominal size of a unit capacitor and δ_0 is the deviation from this value. The variance of this deviation (2.19) equals σ_0^2 - the square of a standard deviation of the unit capacitor.

$$C_0 = C_{0,nom} + \delta_0 \tag{2.18}$$

$$Var(\delta_0) \stackrel{\text{def}}{=} E[(\delta_0 - E(\delta_0))^2] \stackrel{\text{def}}{=} \sigma_0^2 \tag{2.19}$$

Similarly, applied to the C_n, the deviation δ_n from the C_n value is a sum of the deviations of the unit capacitors $C_{n,1}$-$C_{n,m}$. The variance of δ_n can therefore be expressed via the standard deviation of the unit capacitor:

$$C_n = 2^{n-1}C_{0,nom} + \delta_n \tag{2.20}$$

$$\delta_n = \sum_{m=1}^{2^{n-1}} \delta_{n,m} \tag{2.21}$$

$$\begin{aligned} Var(\delta_n) &= Var\left(\sum_{m=1}^{2^{n-1}} \delta_{n,m}\right) \\ &= \sum_{m=1}^{2^{n-1}} Var(\delta_{n,m}) \\ &= \sum_{m=1}^{2^{n-1}} Var(\delta_0) \\ &= 2^{n-1}\sigma_0^2 \end{aligned} \tag{2.22}$$

Deriving the DAC output voltage using the above calculations gives the expression (2.23) where d_n is the binary state of the signals controlling the DAC switches.

$$\begin{aligned} V_{dac,out} &= \frac{\sum_{n=1}^{N} C_n d_n}{\sum_{n=1}^{N} C_n + C_0} V_{ref} \\ &= \frac{\sum_{n=1}^{N} (2^{n-1}C_{0,nom} + \delta_n) d_n}{2^N C_{0,nom} + \sum_{n=0}^{N} \delta_n} V_{ref} \end{aligned} \tag{2.23}$$

The term $\sum_{n=0}^{N} \delta_n$ creates the constant shift in the denominator and does not depend on the code, resulting in the gain-error and contributing to INL. Omitting this term would marginally affect the DNL calculation accuracy, but will lead to a simpler expression (2.24), where the DAC output voltage error is separated from the nominal value:

$$V_{dac,out} \approx \underbrace{\frac{\sum_{n=1}^{N} 2^{n-1} C_{0,nom} d_n}{2^N C_{0,nom}} V_{ref}}_{V_{dac,out,nom}} + \underbrace{\frac{\sum_{n=1}^{N} \delta_n d_n}{2^N C_{0,nom}} V_{ref}}_{V_{dac,out,err}} \tag{2.24}$$

The derivation of the variance of the output voltage error gives:

$$\begin{aligned} Var(V_{dac,out,err}) &= Var\left(\frac{\sum_{n=1}^{N}\delta_n d_n}{2^N C_{0,nom}} V_{ref}\right) \\ &= \frac{V_{ref}^2}{2^{2N} C_{0,nom}^2} Var\left(\sum_{n=1}^{N}\delta_n d_n\right) \\ &= \frac{V_{ref}^2}{2^{2N} C_{0,nom}^2} \sum_{n=1}^{N} Var(\delta_n d_n) \\ &= \frac{V_{ref}^2}{2^{2N} C_{0,nom}^2} \sum_{n=1}^{N} 2^{n-1}\sigma_0^2 d_n \\ &= \frac{V_{ref}^2 \sigma_0^2}{2^{2N} C_{0,nom}^2} \sum_{n=1}^{N} 2^{n-1} d_n \end{aligned} \tag{2.25}$$

Substituting (2.25) into the worst-case non-normalized DNL expression (2.26) and finding the variance yields:

$$DNL_{worst-case} = {}^{10\ldots00}V_{dac,out,err} - {}^{01\ldots11}V_{dac,out,err} \tag{2.26}$$

$$\begin{aligned} Var(DNL_{worst-case}) = Var({}^{10\ldots00}V_{dac,out,err}) + Var({}^{01\ldots11}V_{dac,out,err}) \\ \underbrace{- Cov({}^{10\ldots00}V_{dac,out,err}, {}^{01\ldots11}V_{dac,out,err})}_{=0} \end{aligned} \tag{2.27}$$

$$Var(DNL_{worst-case}) = \frac{V_{ref}^2 \sigma_0^2}{2^{2N} C_{0,nom}^2} \underbrace{\left(\sum_{n=N}^{N} 2^{n-1} + \sum_{n=1}^{N-1} 2^{n-1}\right)}_{2^N-1} \approx \frac{V_{ref}^2 \sigma_0^2}{2^N C_{0,nom}^2} \tag{2.28}$$

For a selected DNL variance, the expression (2.28) specifies the maximum value of the of the unit capacitor's standard deviation σ_0. The value of σ_0 inversely related to capacitor area and consequently, $\sigma_{0,\max}$ defines the minimum allowed unit capacitor area $C_{0,\mathrm{nom,min}}$ for a chosen DNL. From here, the relationship between the unit capacitor's size and σ_0 can either be found in the PDK documentation or extracted from a statistical simulation in CAD.

Alternatively, (2.28) can be used to find normalized DNL expressed in LSBs, as in (2.14). The standard deviation of DNL is:

$$\sigma_{DNL(w.c.)} = \sqrt{Var(DNL_{worst-case})} = \frac{V_{ref}}{\sqrt{2^N}} \cdot \frac{\sigma_0}{C_{0,nom}} \tag{2.29}$$

Normalizing the result to express it in LSBs:

$$\sigma_{DNL(w.c.),LSB} = \frac{\frac{V_{ref}}{\sqrt{2^N}} \cdot \frac{\sigma_0}{C_{0,nom}}}{\frac{V_{ref}}{2^N}} = \sqrt{2^N} \cdot \frac{\sigma_0}{C_{0,nom}} \tag{2.30}$$

Where for the target worst-case DNL the required $\frac{\sigma_0}{C_{0,nom}}$ can be first derived and then adjusted in CAD using statistical simulation. For example, if worst-case DNL is required to be below ± 1 LSB within $\pm 3\sigma$ for the resolution of 10 bit, then $\frac{\sigma_0}{C_{0,nom}}$ requires to be less than 1.042%. The minimum area that would provide that error can be found using parametric statistical simulation on a standalone unit capacitor.

2.7. Synchronous and asynchronous approach

From the system level perspective, the synchronous approach relying on the system clock with a frequency F can provide sampling speed up to $F_{clk}/N+1$ where N is the SAR ADC resolution. A clock multiplier such as PLL is required to provide higher sampling frequencies in the case of the synchronous approach. Alternatively, introducing the ADC's internal clock feedback loop although increasing the ADC's power consumption, removes the requirement for a PLL which can result in better overall power consumption on the system level.

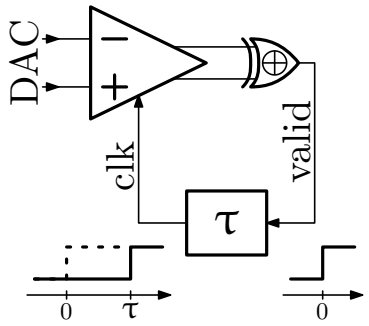


Figure 2.21.: Clock loop in asynchronous SAR ADC

Structurally, the clock loop uses the comparator's outputs to generate the clock signal. During the reset both comparator's outputs are grounded, and during the active state they are differential. Therefore, an XOR gate connected to the outputs can provide a signal that is at logic high during the active state and at logic low during the reset. This extracted "valid" signal resembles the clock. Passed through the delay line valid signal represents the feedback clock loop in the locked state during conversion.
In order to launch the loop, provide the necessary number of clock cycles, and stop the conversion, the controlling circuit can be implemented as shown in Fig. 2.22. The start of conversion (soc) signal switches to logic high and initializes the register by releasing the D flip-flops from the reset state. Simultaneously, the output of the triple OR gate passes the valid signal enabling the delayed clock feedback loop. The conversion then continues until the last D flip-flop in the line sets to the logic high locking the OR gate in its high output level. The flip-flop outputs also provide the signals to enable the DAC switches during each conversion step.

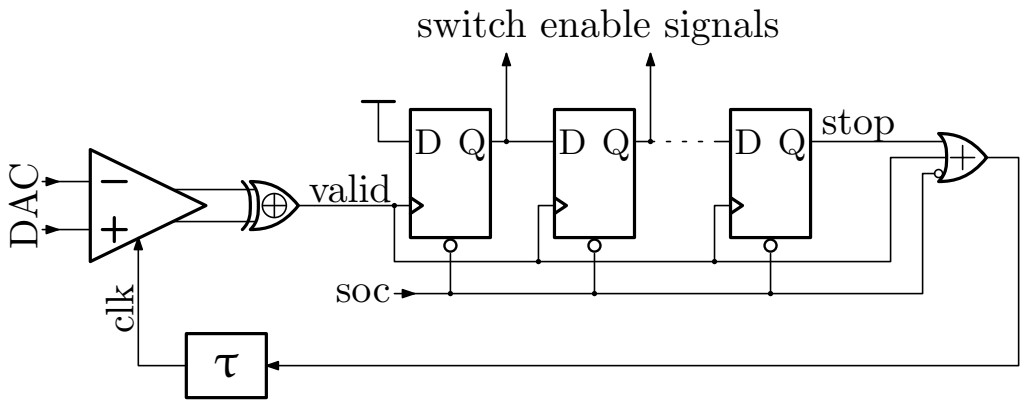


Figure 2.22.: Clock loop control circuit

2.8. Delay line

The delay line together with the comparator propagation delay is responsible for the asynchronous ADC conversion speed. Therefore, the requirements for the delay line besides the energy efficiency are also robustness against the process, supply voltage, and temperature (PVT).
The delay line is combined from the delay elements connected in series. While there are different delay elements available, their robustness against PVT is limited, which makes asynchronous ADCs very sensitive to those factors.
The simplest delay line (Fig. 2.23) is combined from a chain of inverters with increased channel length. The extra length reduces the current flow, and increased parasitic capacitances provide slower rising and falling slopes resulting in a larger propagation delay. The last inverter in the chain can be of standard size in order to restore the rising/falling time to the regular value. The inverter chain is attractive for its simplicity as well as better-than-average robustness against temperature and process variations. The impact of increasing the channel length, however, is limited. Another downside of this approach is large power consumption due to short-circuit current spikes in the middle of the transition when both channels of PMOS and NMOS transistors are open.

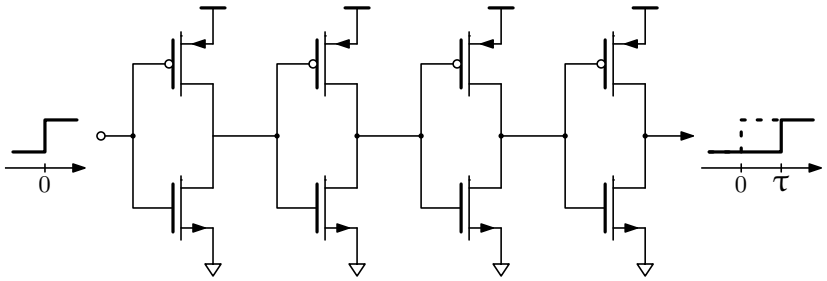


Figure 2.23.: Inverter chain delay line

Limiting the short-circuit current of an inverter helps to increase the delay time and limit the power consumption. It also allows controlling the delay time by adjusting the current over the range of process corners, temperatures, and supply voltages using compensation circuits. The effect of slowing down the rising/falling edges is significantly more prominent in this type of delay line compared to the inverter chain, therefore it requires a careful approach to restoration of the edges' slopes. An inverter at the output can potentially increase the power consumption due to a long time operating in the short-circuit region. An example of using the inverter chain delay and the current-starved delay in an ADC can be found in [HCvR13a].
An alternative method of delay chain design is the self-supply modulation of the inverters [OLP20]. The circuit diagram of this approach is shown in Fig 2.25. The

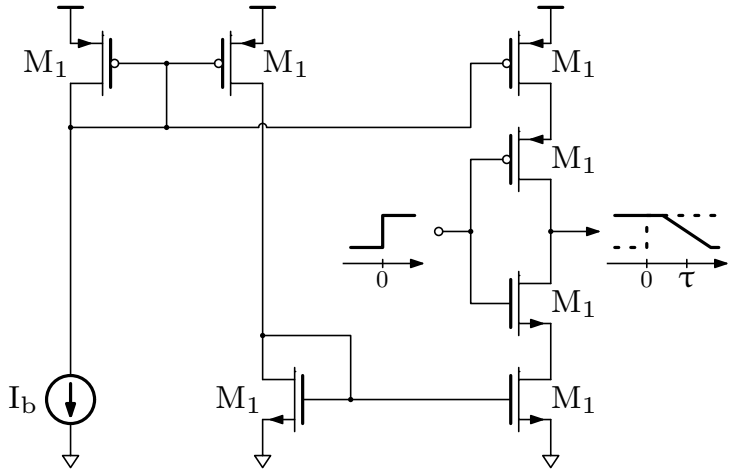


Figure 2.24.: Current-starved delay element

self-supply modulation approach implies connecting the next inverter's supply to the output of the inverter before the preceding one. This results in the channel of the PMOS transistor limiting the short circuit current in the latter inverter. The effect becomes more prominent as the chain grows longer. The propagation time of the self-supply modulation chain grows parabolically with the number of cells, whereas in the regular inverter chain delay grows linearly with the number of inverters. This property makes the approach more energy efficient for larger delay times compared to the inverter chain, however, the tradeoff is higher process and temperature sensitivity.

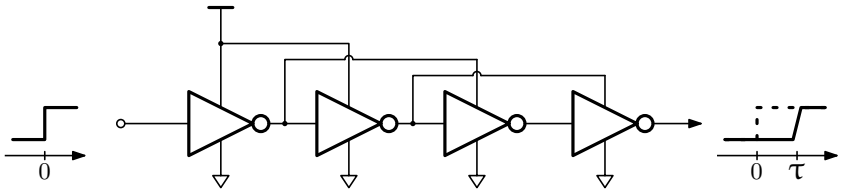


Figure 2.25.: Self-supply modulation delay chain

3 Adiabatic Charging

3.1. Charging of a capacitor

Applied to a DAC in SAR ADC, a switched-capacitor design provides lower power consumption than alternatives such as current-steering or resistive DAC circuits can offer. A switched-capacitor DAC also has the advantage of not consuming DC power aside from leakage. The input signal can be sampled directly on DAC capacitors thus eliminating the need for a separate sample and hold circuit which simplifies the architecture.
One of the issues with capacitor charging, however, is the efficiency of that process. Consider the circuit in Figure 3.1. The resistor R is always present in the form of wire resistance, output resistance of the voltage source, or channel resistance of a MOSFET switch. With the switch closed, the circuit represents a simple RC

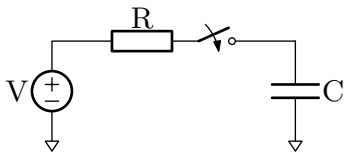


Figure 3.1.: Charging of a capacitor

network. The output voltage and current are then the step-response of the circuit with no initial charge expressed as (3.1). To calculate the energy spent at the voltage source, integration can be performed.

$$\begin{cases} I(t) & = \dfrac{V}{R} e^{\frac{-t}{RC}} \\ V_{out}(t) & = V(1 - e^{\frac{-t}{RC}}) \end{cases} \tag{3.1}$$

The energy E_{source} is a work done by the voltage source to move the charge q. The integrated energy is then expressed as (3.2). The voltage V is the DC output

voltage of the voltage source. The current I(t) is the same for all circuit elements and is taken from (3.1).

$$\begin{aligned} E_{source} &= \int V\,dq \\ &= \int V I(t)\,dt \\ &= \frac{V^2}{R}\int_0^\infty e^{\frac{-t}{RC}}\,dt \\ &= -CV^2 e^{\frac{-t}{RC}}\Big|_0^\infty = CV^2 \end{aligned} \tag{3.2}$$

Similarly, integrating the energy at the capacitor gives (3.3) and results in only half of the energy from the voltage source being stored at the capacitor. The rest of the energy is dissipated as heat at the resistor.

$$\begin{aligned} E_C &= \int V_{out}\,dq \\ &= \int V_{out}(t) I(t)\,dt \\ &= \int_0^\infty \frac{V^2}{R} e^{\frac{-t}{RC}}(1 - e^{\frac{-t}{RC}})\,dt \\ &= -\frac{1}{2}CV^2 e^{\frac{-2t}{RC}}\left(2e^{\frac{t}{RC}} - 1\right)\Big|_0^\infty = \frac{1}{2}CV^2 \end{aligned} \tag{3.3}$$

With half of the energy being dissipated at the resistor, the efficiency of such charging is limited to 50%. However, one important detail about that result is the energy consumption that grows linearly with the capacitor size whereas the dependency on the voltage is squared. Applied to a capacitive DAC, this behavior makes switching schemes that rely on capacitor-splitting to reduce the energy consumption (Ch. 2.3, Fig. 2.8) generally less efficient compared to the approaches that reduce voltage step size using common-mode voltage.

3.2. Charging with linear voltage

If the same circuit as in Fig. 3.1 is being charged with a voltage ramp instead of a step, the charging efficiency increases [PSN00]. Consider the ramp with maximum voltage V and the rise time T as shown in Figure 3.2. The input voltage function

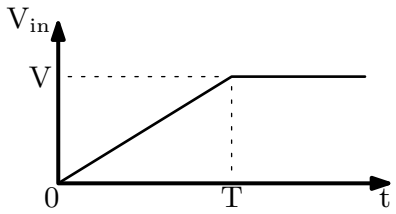


Figure 3.2.: Input voltage ramp

is then described as in the eq. (3.4), where V/T is the slope of the ramp.

$$V_{in}(t) = \begin{cases} 0 & t < 0 \\ \dfrac{Vt}{T} & 0 \leq t < T \\ V & t \geq T \end{cases} \tag{3.4}$$

The impulse response of the RC circuit is:

$$h(t) = \frac{e^{\frac{-t}{RC}}}{RC} u(t) \tag{3.5}$$

The output voltage is then a convolution of the input voltage (3.4) and the impulse response (3.5) that results in (3.6):

$$V_{out}(t) = \begin{cases} \dfrac{1}{T} V(RC(e^{\frac{-t}{RC}} - 1) + t) & 0 < t \leq T \\ \dfrac{1}{T} V e^{\frac{-t}{RC}}(Te^{\frac{t}{RC}} - RCe^{\frac{T}{RC}} + RC) & t \geq T \end{cases} \tag{3.6}$$

The current I(t) therefore is:

$$I(t) = C\frac{dV_{out}(t)}{dt} \tag{3.7}$$

The input voltage can be expressed as the sum of voltage drops on the resistor and the capacitor:

$$V_{in} = I(t)R + V_{out} = CR\frac{dV_{out}}{dt} + V_{out} \tag{3.8}$$

The energy dissipated on the resistor is responsible for the loss of efficiency. The integrated energy dissipation is the integral of the current through the resistor

multiplied by the voltage drop. In the case of the resistor, the voltage drop is the difference between input and output voltages. Deriving V_{in}–V_{out} from (3.8) and multiplying it to the current (3.7) gives:

$$\begin{aligned} E_{diss,R} &= \int I(t)V_R(t)\,dt \\ &= \int I(t)(V_{in}(t) - V_{out}(t))\,dt \\ &= \int C\frac{dV_{out}(t)}{dt}CR\frac{dV_{out}(t)}{dt}\,dt \\ &= RC^2\int_0^\infty \frac{dV_{out}(t)}{dt}\frac{dV_{out}(t)}{dt}\,dt \\ &= RC^2\left[\int_0^T \left(\frac{V - Ve^{\frac{-t}{RC}}}{T}\right)^2 dt\right] \\ &\quad + RC^2\left[\int_T^\infty \left(\frac{V(e^{\frac{T}{RC}} - 1)e^{\frac{-t}{RC}}}{T}\right)^2 dt\right] \\ &= RC^2\frac{V^2(RC(e^{\frac{-T}{RC}} - 1) + T)}{T^2} \end{aligned} \tag{3.9}$$

The result of (3.9) exhibits a dependence on the ramp rise time T. Analyzing the result further shows that when the rise time approaches 0, the energy dissipation is the same as when a capacitor is charged with a voltage step (eq. (3.10)). However, as the rise time approaches infinity, the energy loss at the resistor approaches zero (eq. (3.11)).

$$\lim_{T\to 0} E_{diss,R} = \frac{CV^2}{2} \tag{3.10}$$

$$\lim_{T\to \infty} E_{diss,R} = 0 \tag{3.11}$$

To analyze the reduction of energy loss in more detail, the rise time can be represented via its ratio to the time constant RC as shown in eq. (3.12).

$$x = \frac{T}{RC} \tag{3.12}$$

Substitution of (3.12) into the result of (3.9) gives the expression for the energy loss in the resistor (3.13).

$$E_{diss,R} = \frac{e^{-x} + x - 1}{x^2}CV^2 \tag{3.13}$$

$$E_{cap} = \frac{1}{2}CV^2 \tag{3.14}$$

$$E_{source} = E_{diss,R} + E_{cap} \tag{3.15}$$

The efficiency of the charging process η is therefore expressed as a ratio between the energy stored in the capacitor (3.14) and the energy withdrawn from the source (3.15). The resulting efficiency is expressed as (3.16), where x is the ratio between the rise time of the input voltage ramp and the time constant RC:

$$\eta = \frac{E_{cap}}{E_{source}} = \frac{E_{cap}}{E_{diss,R} + E_{cap}} = \frac{x^2}{x^2 + 2e^{-x} + 2x - 2} \tag{3.16}$$

The charging efficiency for the rise time values of 0.01-50RC is plotted in Figure 3.3. The data for the red waveform was calculated using the eq. (3.16). The blue waveform shows data taken from a SPICE simulation. The plot demonstrates a quickly increasing benefit of charging with a ramp using rise times in the range of approx. 2-10RC. Increasing the rise time further does not improve the efficiency at the same pace as the graph approaches a plateau.

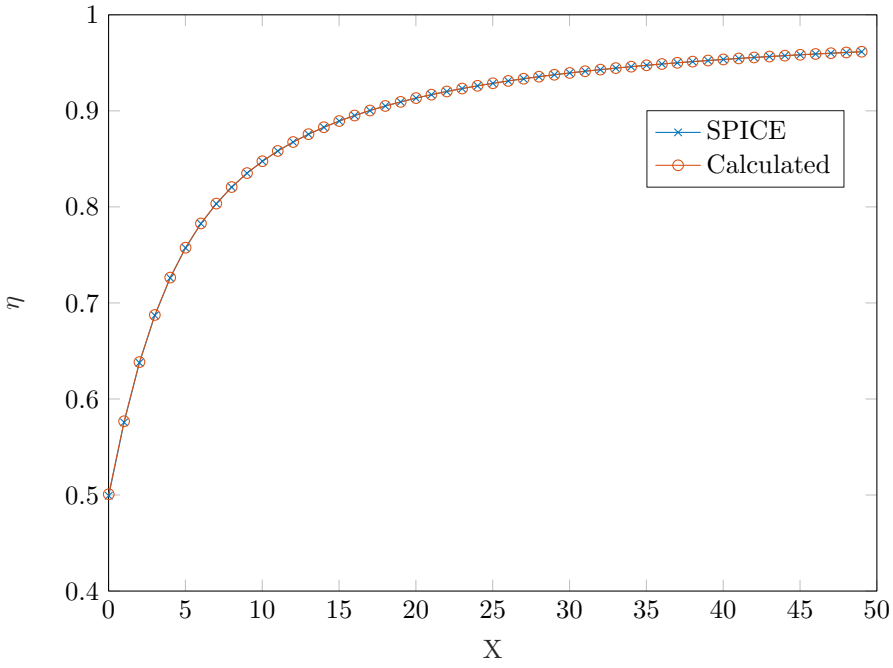


Figure 3.3.: Efficiency of charging a capacitor using voltage ramp with varied rise time of x*RC

3.3. Stepwise adiabatic charging

Linear voltage charging requires a voltage ramp generator which limits the application of this technique in SAR ADCs. The ramp generator circuitry introduces excessive power consumption if compared to the benefit of energy saving during the charging of the DAC's capacitors. The regular DAC capacitance values are not large enough to justify the use of such circuits.
Additionally, the discrete-time nature of the SAR architecture, including the SC-DAC operation, comparator, and digital control logic, makes this architecture suitable for various applications, including those where ADC is only used on-demand because it consumes very little power in a standby mode. Introducing the ramp generator would imply using continuous-time circuits narrowing the application range of this architecture, which is not desirable.

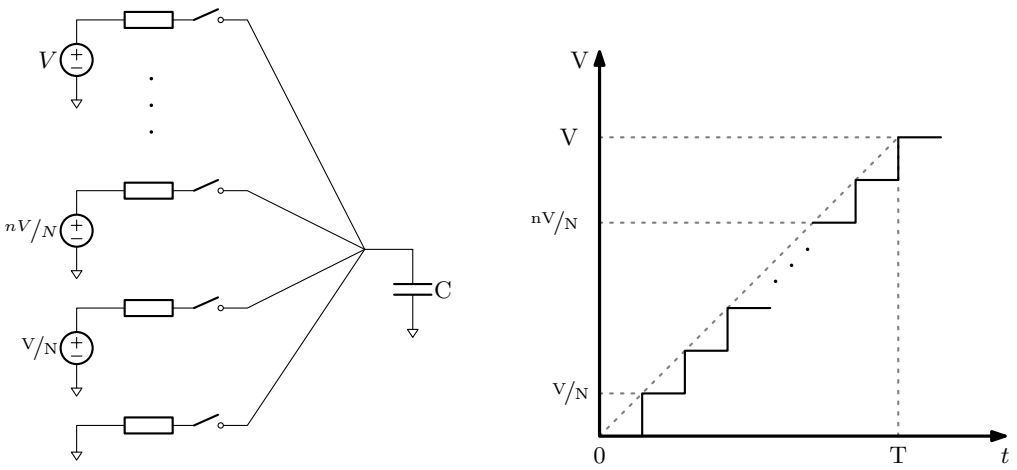


Figure 3.4.: Stepwise adiabatic charging: N voltage steps replace the linear ramp

In order to better accommodate the switched-capacitor architecture, the linear ramp can be replaced with a series of smaller voltage steps as shown in Fig 3.4. The energy required to charge the capacitor C from its current state to the next voltage level is:

$$\begin{aligned} E_{source,n} &= V_n \int_{Q_{n-1}}^{Q_n} dq \\ &= V_n(Q_n - Q_{n-1}) \\ &= V_n(CV_n - CV_{n-1}) \end{aligned} \tag{3.17}$$

Assuming that all N voltage steps are equal gives:

$$\begin{aligned} E_{source,n} &= V_n C \Delta V \\ &= \frac{nV}{N} C \frac{V}{N} \\ &= \frac{nCV^2}{N^2} \end{aligned} \tag{3.18}$$

The total amount of energy consumed from all voltage sources is then the sum of the energies:

$$\begin{aligned} E_{source,total} &= \sum_{n=1}^{N} \frac{nCV^2}{N^2} \\ &= \frac{CV^2}{N^2} \cdot \frac{N(N+1)}{2} \\ &= \frac{CV^2}{2} + \frac{CV^2}{2N} \end{aligned} \tag{3.19}$$

The first term in the result of (3.19) is the energy stored at the capacitor in the same manner as in the simple 1-step charging (3.3) and linear charging (3.14). The second term represents the total energy dissipated on all switch resistors [CKBY12]:

$$E_{diss,total} = \frac{CV^2}{2N} \tag{3.20}$$

$$E_{cap} = \frac{CV^2}{2} \tag{3.21}$$

The charging efficiency therefore is:

$$\eta = \frac{E_{cap}}{E_{source}} = \frac{E_{cap}}{E_{diss,total} + E_{cap}} \tag{3.22}$$

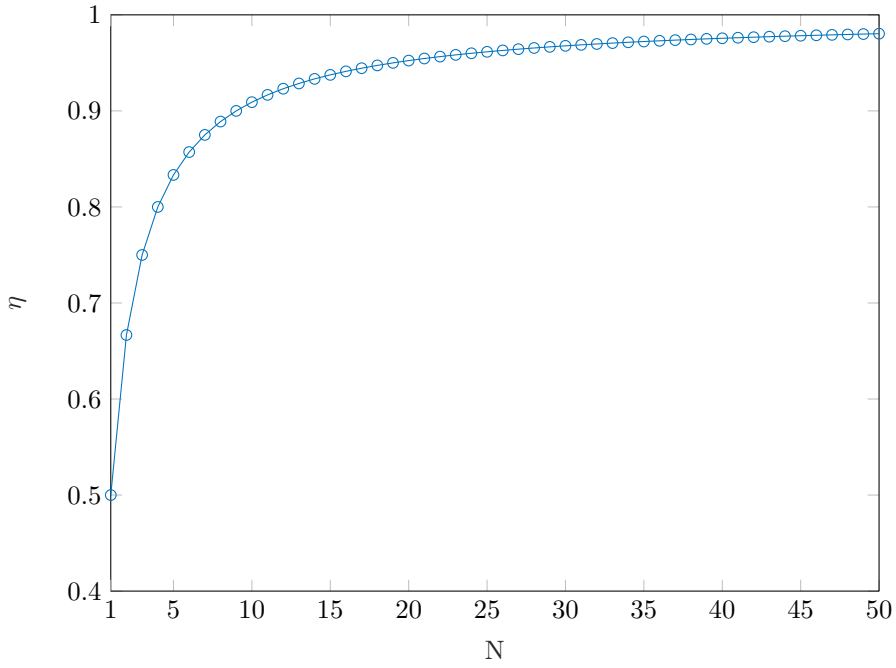


Figure 3.5.: Efficiency of charging a capacitor using the stepwise approach with a varied number of steps N

The calculated efficiency for various numbers of charging steps is shown in Figure 3.5. The plot shows similar behaviour to the efficiency of charging with a linear voltage ramp (Fig. 3.3). However, this approach is better suited for integration into the switched-capacitor architecture: the efficiency improvements are configurable with the number of voltage steps, and the approach requires only DC voltage sources without the requirements for continuous-time waveform generators such as a linear ramp generator.

3.4. Stepwise adiabatic charging applied to SC-DAC

Applied to the DAC capacitor array the stepwise charging reduces energy consumption without compromising the accuracy. It is sufficient that the first (Gnd) and the last (Vref) steps are stable voltage references. That way, charging, as well as discharging, will always finish on a precise value if sufficient settling time is provided. Inaccuracies of the intermediate steps only affect energy savings.
Little published data is available on the adiabatic charging applied to DAC as a part of SAR ADC. Designs presented in [vEvTG+08, OP16, OP17] utilize the charging of capacitors with 2 or 3 steps, however, the reported work does not concentrate on the application of the adiabatic charging approach in general, and does not investigate the variety of configurations.

3.4.1. A conventional 3-bit ADC

To demonstrate the stepwise charging influence on the DACs switching energy, a 3-bit differential ADC can be considered. The conventional switching scheme in its single-ended form was discussed in Chapter 2.1. In the case of the differential architecture, an additional negative DAC follows the same procedure in an inverted manner. That doubles the input dynamic range, cancels out the charge injection during the sampling, and cancels out the common-mode comparator kickback. The conversion tree of the resulting ADC is shown in Figure 3.6.

- *Sampling:*
  The input signal is sampled on positive and negative DAC matrices against the common-mode voltage (V_{cm}=0.5V_{ref}), using the bottom-plate sampling approach. Once the matrices are charged from the input sources, the bottom plates switch from V_{in+}(V_{in-}) to Gnd(V_{ref}) The common-mode voltage is disconnected prior to that in order to preserve the sampled voltage. Since the charge is preserved during that step, no energy is spent.
  Upon connection of the switches in positive DAC to GND, the voltage at the positive DAC becomes equal to GND+V_{CM}-V_{IN+}, and similarly, the negative DAC switches' connection to V_{REF} makes the negative DAC output voltage equal to V_{REF}+V_{CM}-V_{IN-}. Effectively that spreads the DAC differential output voltage range: depending on the input voltage, the positive DAC output at this step lies within the range of [-V_{cm}; V_{cm}], and similarly, the negative DAC output lies within the range of [V_{cm}; 1.5V_{ref}]. Figure 3.7 illustrates that mechanism.

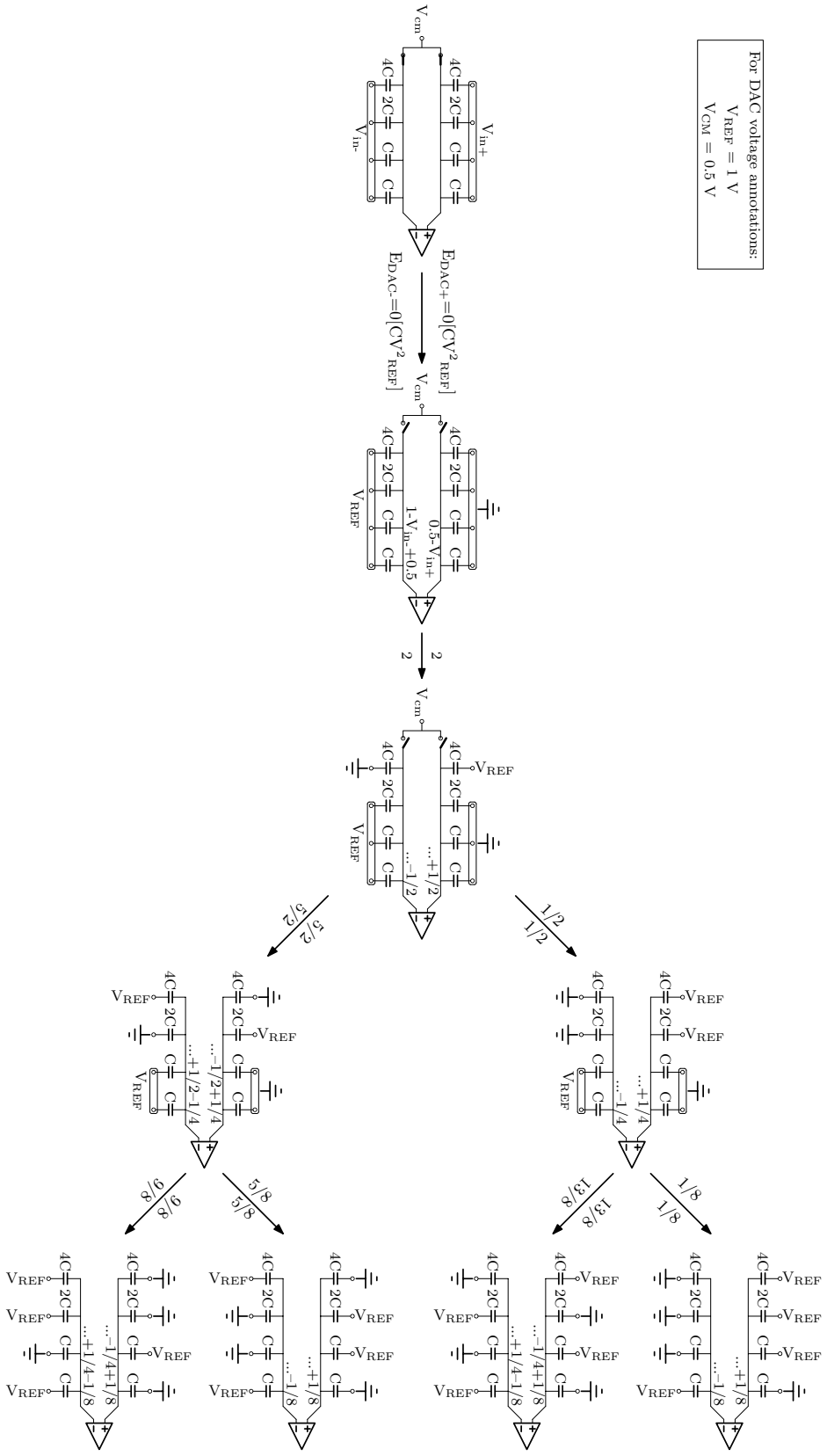


Figure 3.6.: Switching energy tree of a conventional 3-bit SAR ADC

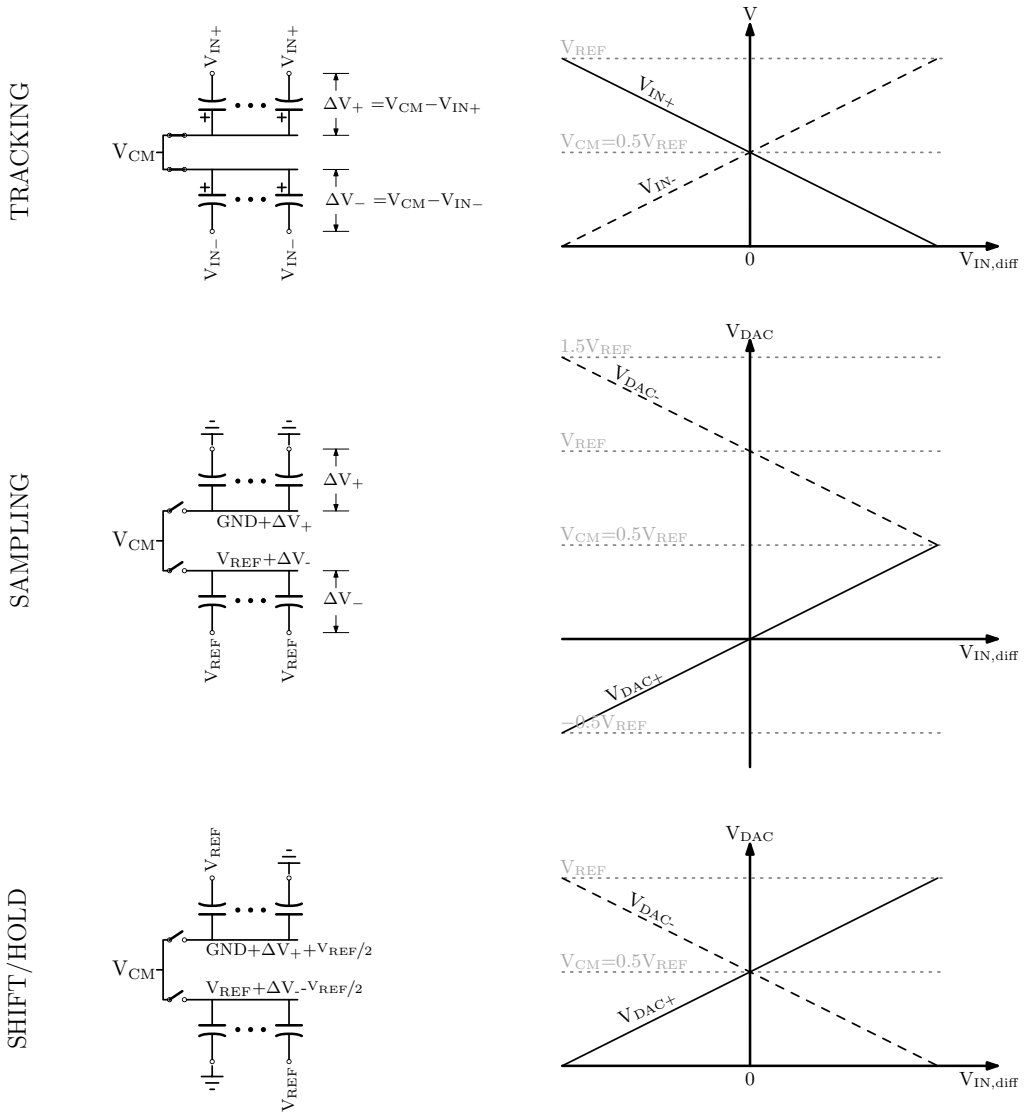


Figure 3.7.: Sample and hold DAC voltage for various input voltages

- *Shift and Hold:*
  To bring the signals back to the range of [0; V_{ref}], the positive DAC is required to switch the MSB up, and the negative DAC switches the MSB down. The resulting sampled signal is inverted and lies within the appropriate voltage range (Fig 3.7, bottom).
  Additionally, the mentioned MSB pre-set allows the DAC to later perform a downshift in case the comparator result is negative: the downshift requires the MSB switch to reset and the next bit to set. Otherwise, the only direction the DAC could go is to further increase the voltage.

- *Conversion:*
  Depending on the result of the comparison, DAC performs either the upshift or downshift. In the case of the 3-bit DAC, there are only 2 conversion cycles required, since the last bit decision is taken directly from the comparator without further need to switch the DAC voltage.

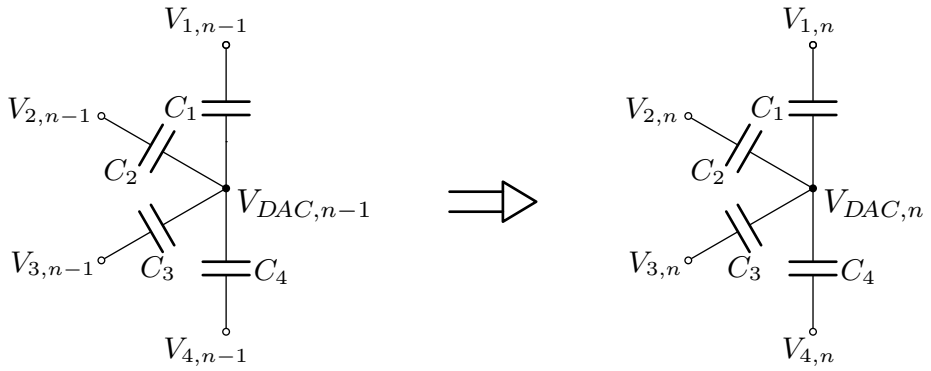


Figure 3.8.: Star capacitor network charging with multiple voltage sources

The energy spent on DAC's capacitors can be calculated similarly to (3.17) except that in DAC the opposite plate of a capacitor is not connected to the ground. The SC-DAC topology essentially represents a star, where all the top plates (tp) are connected to one node, which is the DAC output, and the bottom plates (bp) are switched between various voltage sources as illustrated in Fig. 3.8. For a single DAC capacitor that at the n-th conversion step is connected to a voltage source V_n, the energy withdrawn from that source is:

$$\begin{aligned} E_n &= V_n \int_{Q_{n-1}}^{Q_n} dq \\ &= V_n(Q_n - Q_{n-1}) \\ &= V_n \left[C(V_{bp,n} - V_{tp,n}) - C(V_{bp,n-1} - V_{tp,n-1})\right] \\ &= V_n \left[C(V_n - V_{DAC,n}) - C(V_{n-1} - V_{DAC,n-1})\right] \end{aligned} \tag{3.23}$$

which can be rewritten as:

$$E_n = CV_n \left(\Delta V_n - \Delta V_{DAC,n}\right) \tag{3.24}$$

To further calculate the switching energy at a given conversion step, a downshift after the first comparator's decision can be used as one of the most representative examples: each DAC has 2 capacitors switched simultaneously in different directions, exhibiting the complete variety of possible combinations. Applying the eq. (3.24) to all capacitors in both DACs, the switching energy at this conversion step can be expressed as:

$$\begin{aligned} E_{sw,DAC+} = 4C \ \cdot \ 0 \ \cdot \ \left(-V_{ref} - (-\frac{V_{ref}}{4})\right) \\ + 2C \cdot V_{ref} \cdot \left(V_{ref} - (-\frac{V_{ref}}{4})\right) \\ + C \cdot 0 \cdot \left(0 - (-\frac{V_{ref}}{4})\right) \\ + C \cdot 0 \cdot \left(0 - (-\frac{V_{ref}}{4})\right) \\ = \quad \frac{5}{2} C V_{ref}^2 \end{aligned} \tag{3.25}$$

$$\begin{aligned} E_{sw,DAC-} = 4C \ \cdot \ V_{ref} \ \cdot \ \left(V_{ref} - \frac{V_{ref}}{4}\right) \\ + 2C \cdot 0 \cdot \left(-V_{ref} - \frac{V_{ref}}{4}\right) \\ + C \cdot V_{ref} \cdot \left(0 - \frac{V_{ref}}{4}\right) \\ + C \cdot V_{ref} \cdot \left(0 - \frac{V_{ref}}{4}\right) \\ = \quad \frac{5}{2} C V_{ref}^2 \end{aligned} \tag{3.26}$$

Applied to the rest of the branches in the 3-bit ADC conversion tree the calculated switching energy is included in Fig. 3.6. The average switching energy can then be calculated with an assumption that every code is equiprobable. Therefore, for a full-scale linear input voltage ramp, all the resulting output codes will be encountered for an equal number of times. Every branch in every fork will then also be taken an equal number of times, giving:

$$\overline{E_{sw}} = CV_{ref}^2 \left(4 + \frac{{}^2\!/_2 + {}^{10}\!/_2}{2} + \frac{\frac{{}^2\!/_8 + {}^{26}\!/_8}{2} + \frac{{}^{10}\!/_8 + {}^{18}\!/_8}{2}}{2}\right) = 8{,}75 CV_{ref}^2 \tag{3.27}$$

3.4.2. A conventional 3-bit ADC with 4-step stepwise charging

Stepwise adiabatic charging applied to a 3-bit conventional ADC introduces additional steps in the conversion cycle. Every conversion step becomes divided by a series of smaller equidistant voltage steps. At the DAC outputs, the steps are equidistant within a given conversion step, meaning, if originally the conversion step required DAC to subtract $\frac{1}{4}\mathrm{V_{ref}}$ with one step, after introducing a 4-step stepwise charging the DAC would subtract a quarter of this value for 4 times. Within the next conversion cycle, the DAC will subtract (or add) 4 quarters of the next weight of $\frac{1}{8}\mathrm{V_{ref}}$.
The comparator's bit decisions are taken after the stepwise charging is complete at every conversion step. The binary search procedure is therefore not modified. The conversion tree of the resulting 3-bit ADC featuring 4-step stepwise charging is shown in Fig. 3.9. Noticeably, compared to the original ADC in Fig. 3.6, the switching energy of every conversion step is significantly reduced and some of the branches exhibit negative energy values, indicating the energy is taken from what was stored in the capacitive matrix after sampling and returned back to the voltage sources.
A more detailed look at the negative switching energy can be taken at the upward conversion after the first-bit decision in Fig. 3.9. The charging sequence of this branch is depicted in detail in Fig. 3.10.
Applying the same logic as in (3.25) and neglecting capacitors connected to Gnd as they only produce terms in the equations that are multiplied by 0, the switching energy derives as:

$$\begin{aligned} E_{1,1,DAC+} &= 4C \cdot V_{ref} \cdot \left(0 - \frac{1}{4}\frac{V_{ref}}{4}\right) + 2C \cdot \frac{1}{4}V_{ref} \cdot \left(\frac{1}{4}V_{ref} - \frac{1}{4}\frac{V_{ref}}{4}\right) \\ &= -\frac{5}{32}CV_{ref}^2 \end{aligned} \tag{3.28}$$

$$\begin{aligned} E_{1,2,DAC+} &= 4C \cdot V_{ref} \cdot \left(0 - \frac{1}{4}\frac{V_{ref}}{4}\right) + 2C \cdot \frac{2}{4}V_{ref} \cdot \left(\frac{1}{4}V_{ref} - \frac{1}{4}\frac{V_{ref}}{4}\right) \\ &= -\frac{2}{32}CV_{ref}^2 \end{aligned} \tag{3.29}$$

$$\begin{aligned} E_{1,3,DAC+} &= 4C \cdot V_{ref} \cdot \left(0 - \frac{1}{4}\frac{V_{ref}}{4}\right) + 2C \cdot \frac{3}{4}V_{ref} \cdot \left(\frac{1}{4}V_{ref} - \frac{1}{4}\frac{V_{ref}}{4}\right) \\ &= \frac{1}{32}CV_{ref}^2 \end{aligned} \tag{3.30}$$

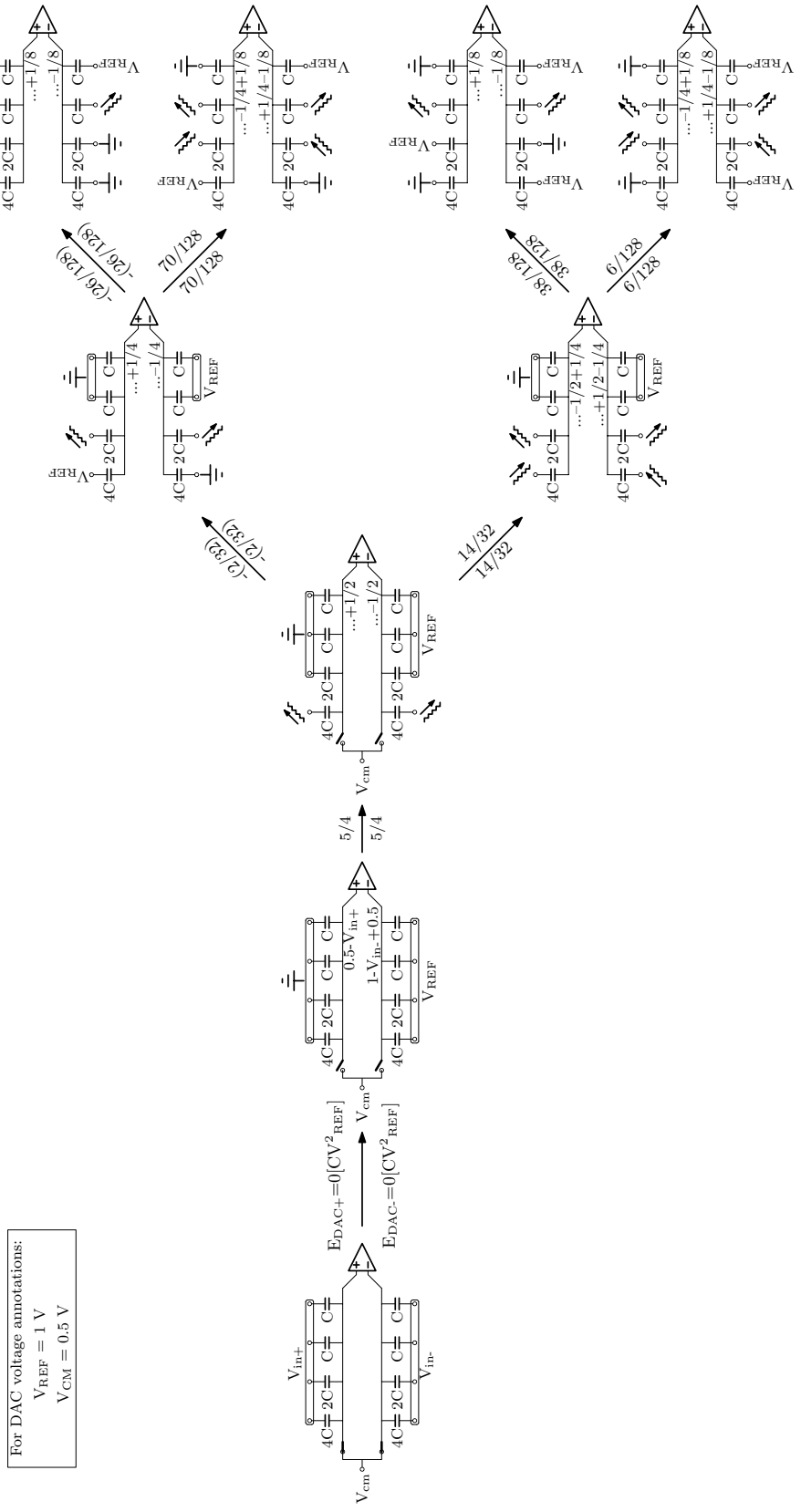


Figure 3.9.: Switching energy tree of a conventional 3-bit SAR ADC featuring 4-step stepwise charging

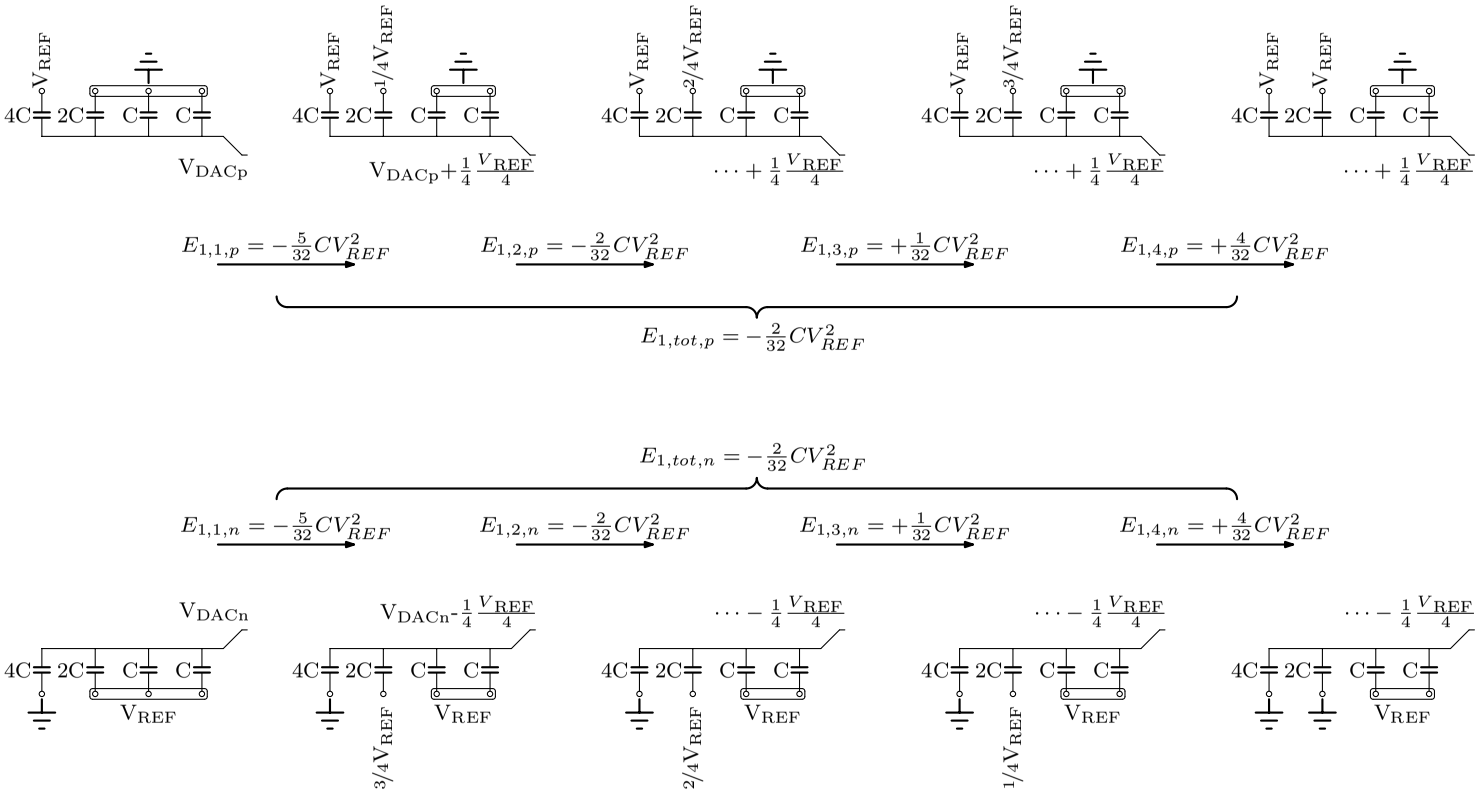


Figure 3.10.: Detailed switching energy of a 3-bit SAR ADC with 4-step stepwise switching for a single conversion step

$$E_{1,4,DAC+} = 4C \cdot V_{ref} \cdot \left(0 - \frac{1}{4}\frac{V_{ref}}{4}\right) + 2C \cdot \frac{4}{4}V_{ref} \cdot \left(\frac{1}{4}V_{ref} - \frac{1}{4}\frac{V_{ref}}{4}\right) \quad (3.31)$$
$$= \frac{4}{32}CV_{ref}^2$$

The negative DAC mirrors the same behaviour and has the same energy consumption as the positive DAC at every step of the stepwise charging.
Following the same procedure as in (3.27) and using values from Fig. 3.9, the average DAC switching energy across all codes can be derived as:

$$\overline{E_{sw}} = CV_{ref}^2 \left({}^{10}/_{4} + \frac{{}^{-4}/_{32} + {}^{28}/_{32}}{2} + \frac{\frac{{}^{-52}/_{128} + {}^{140}/_{128}}{2} + \frac{{}^{76}/_{128} + {}^{12}/_{128}}{2}}{2} \right) \quad (3.32)$$
$$= \frac{103}{32}CV_{ref}^2 \approx 3{,}22CV_{ref}^2$$

The resulting average switching energy is 63.2% less than in the case of 1-step conventional 3-bit ADC (3.27). This energy consumption improvement is larger than 50% in the case of the single capacitor stepwise charging. The more complex circuits such as the star-topology with multiple voltage sources, allow for the energy to be transferred back into the voltage sources as shown in (3.28)-(3.29). That, applied to the limited pre-defined number of switching combinations allows reduction of the average DAC switching energy beyond 50%.

3.4.3. Generalized conventional N-bit ADC with M-step stepwise charging

To generalize the case of using the stepwise charging in a conventional N-bit SAR ADC, two properties of this circuit can be used to simplify the derivation:

- both, positive and negative DAC switching energies are equal, which makes it possible to consider only one of them for calculations and multiply the result by 2.

- at a given conversion step (bit-decision), the average energies of every fork are equal. It is illustrated using a schematic conversion tree in Fig. 3.11. The average energies in the same column are equal. That makes it possible to select the branches for the calculation of the average switching energy of the DAC.

The branches selected for calculation are highlighted in 3.11 and the resulting sequence is expanded in Fig. 3.12. After the sampling, the selected branches are the downward-shifting ones. After every downward transition, there is a fork with

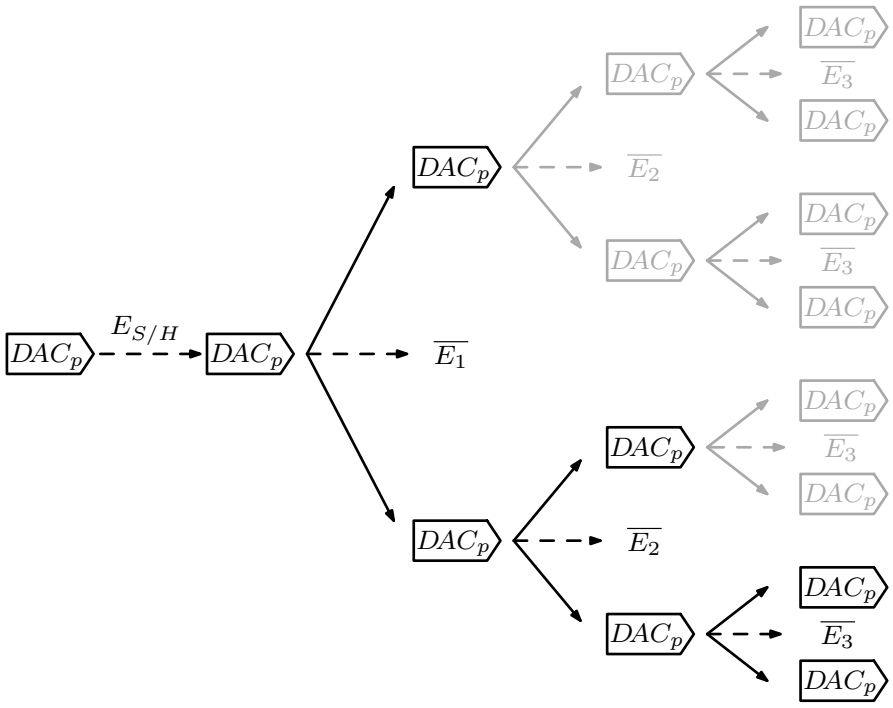


Figure 3.11.: Average energy tree: all $\overline{E_n}$s within the same index are equal. Highlighted are the branches used for calculation

an upward and a downward transition that is used to calculate the average energy of the given conversion step. Then, the next fork originates from the downward branch of the current one. If only a positive DAC is considered, these branches have only two capacitors that are not connected to the ground at each conversion step, which is convenient for the derivation.
The resulting sequence from Fig. 3.12 has 2 parts:

- *Sampling-Hold-Shift:*
  The input signal is sampled on the matrix and the MSB capacitor is switched-on. The energy consumption during that process is marked as $E_{S/H}$

- *Conversion:*
  In this part, the converter executes a sequence of bit-decisions. Here, the average energy of both possible conversions is to be calculated at every step as $\overline{E_n}$. The initial state for the next bit-decision then originates from the downward conversion branch of the current decision. The total number of conversion steps is 1 less than the resolution of the ADC since the last bit decision is taken directly from the comparator's output and therefore does not require DAC to switch.

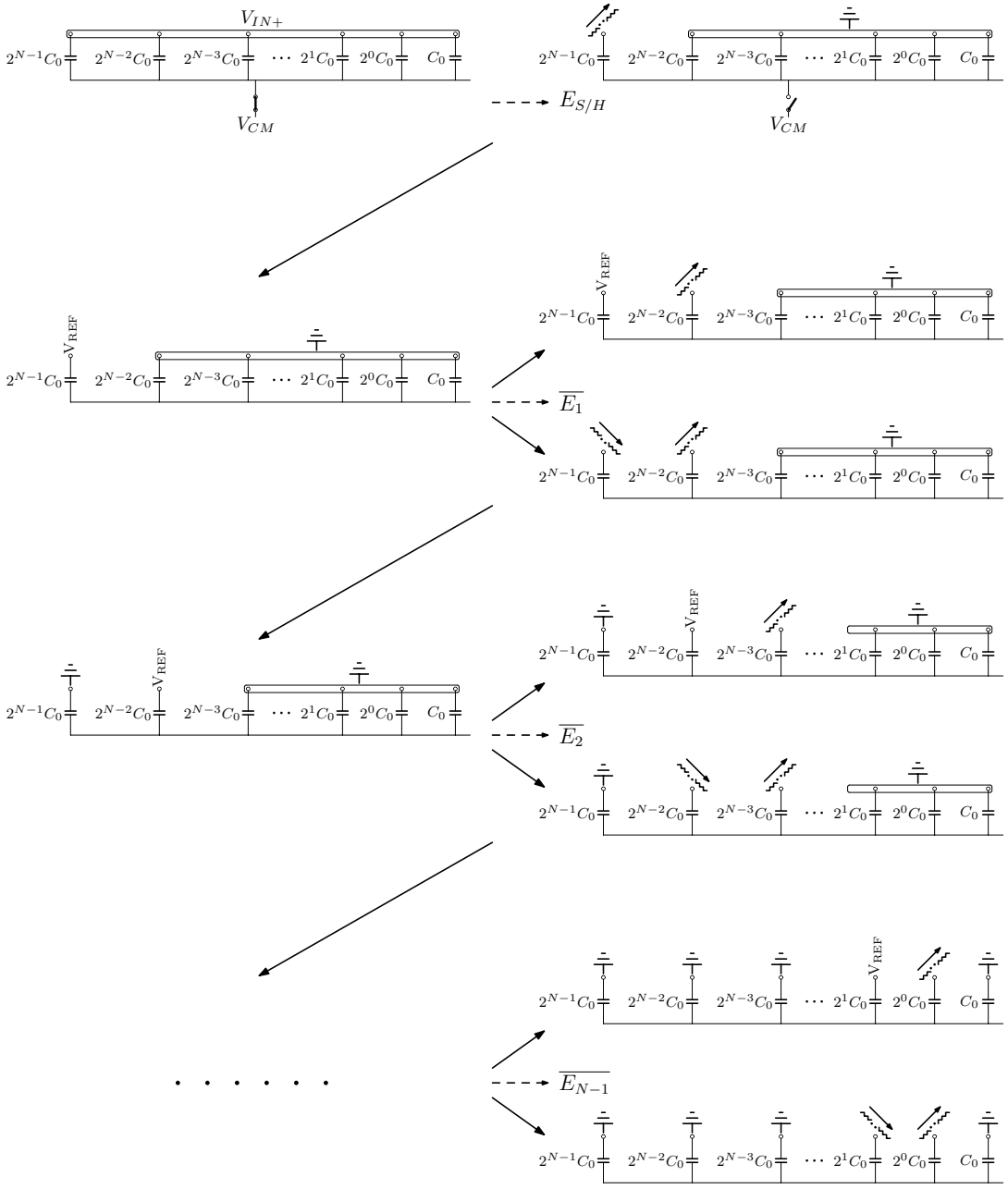


Figure 3.12.: N-bit conventional SAR ADC average energy calculation sequence

The overall average energy can then be derived as:

$$\overline{E_{sw,DAC}} = 2 \cdot \overline{E_{sw,DACp}} = 2 \cdot \left[E_{S/H} + \sum_{n=1}^{N-1} \overline{E_n} \right] \tag{3.33}$$

Figure 3.13 shows the switching sequence for $E_{S/H}$ calculation in detail.

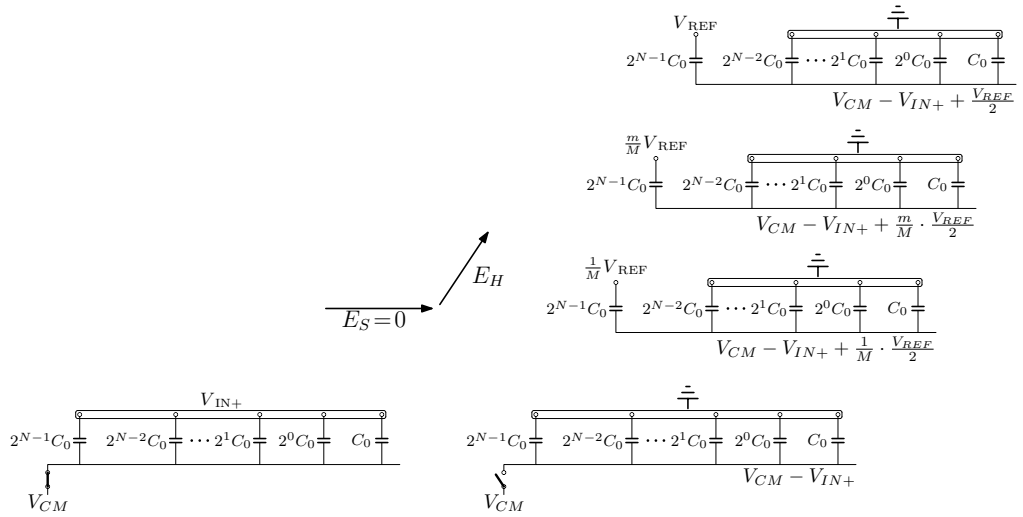


Figure 3.13.: Generalized sampling and hold procedure of an N-bit M-step stepwise conventional SAR ADC

During the first transition marked as E_S DAC does not consume energy since the charge on the matrix is preserved. The energy consumption during every step in the follow-up sequence of M transitions E_H can be derived in a similar manner to (3.24). For a single step that gives:

$$E_{H,m} = 2^{N-1} C_0 V_{source,m} \left(\Delta V_{source} - \Delta V_{DAC} \right) \tag{3.34}$$

Throughout stepwise charging sequence, the nominal value of $\mathrm{V_{source,m}}$ transitions from $\mathrm{V_{REF}/M}$ to $\mathrm{V_{REF}}$, whereas increments $\Delta \mathrm{V_{source}}$ and $\Delta \mathrm{V_{DAC}}$ remain the same for each charging step of the sequence, i.e.:

$$V_{source,m} = \frac{m}{M} V_{REF} \tag{3.35}$$

$$\Delta V_{source} = \frac{1}{M} V_{REF} \tag{3.36}$$

$$\Delta V_{DAC} = \frac{1}{M} \frac{V_{REF}}{2} \tag{3.37}$$

Therefore, the energy consumption $E_{S/H}$ can be represented as:

$$\begin{aligned} E_{S/H} &= \sum_{m=1}^{M} 2^{N-1} C_0 \frac{m}{M} V_{REF} \left(\frac{1}{M} V_{REF} - \frac{1}{M} \frac{V_{REF}}{2} \right) \\ &= \frac{2^{N-1} C_0 V_{REF}^2}{2M^2} \sum_{m=1}^{M} m \\ &= \frac{2^{N-1} C_0 V_{REF}^2}{2M^2} \frac{M(M+1)}{2} \\ &= 2^{N-3} C_0 V_{REF}^2 \frac{M+1}{M} \end{aligned} \tag{3.38}$$

During the conversion phase, the n-th conversion step when the stepwise charging is applied, can be represented as shown in the Fig. 3.14. At every bit-decision, there is a two-way fork with an upward and a downward conversion marked accordingly as $E_{n,up}$ and $E_{n,down}$. Each of these conversions consists of M charging steps.

During the upward conversion, at n-th conversion step the DAC's capacitor $2^{N-n}C_0$ remains connected to V_{REF} and the next capacitor $2^{N-n-1}C_0$ is charged with a series of M steps. Similarly to the sample-hold charging energy derivation, the increments at the voltage source side and the DAC's output remain the same across all M steps, which gives the charging energy of the m-th step of the upwards transition during the n-th conversion cycle $E_{n,m,up}$:

$$\begin{aligned} E_{n,m,up} = {} & 2^{N-n} C_0 V_{REF} \left(0 - \frac{1}{M} \frac{V_{REF}}{2^{n+1}} \right) \\ & + 2^{N-1-n} C_0 \frac{m}{M} V_{REF} \left(\frac{1}{M} V_{REF} - \frac{1}{M} \frac{V_{REF}}{2^{n+1}} \right) \end{aligned} \tag{3.39}$$

The procedure during the downward conversion is similar to the upward with the exception of the larger, $2^{N-n}C_0$ capacitor, which does not remain connected to the reference voltage source, but instead, it is discharged with the series of M steps. That results in the voltage source increment for this capacitor being equal to $-\frac{1}{M}V_{REF}$ and the nominal source voltage at m-th step equal to $\frac{M-m}{M}V_{REF}$. The DAC's output voltage increment will also change the sign compared to the upward conversion. Since the twice as large capacitor switches in the opposite direction to the smaller one, the output voltage will decrease to $\frac{1}{M}\frac{V_{REF}}{2^{n+1}}$ with each step instead of increasing, thus providing the downward conversion. The energy consumption in this case can be expressed as:

$$\begin{aligned} E_{n,m,down} = {} & 2^{N-n} C_0 \frac{M-m}{M} V_{REF} \left(-\frac{1}{M} V_{REF} - (-\frac{1}{M} \frac{V_{REF}}{2^{n+1}}) \right) \\ & + 2^{N-1-n} C_0 \frac{m}{M} V_{REF} \left(\frac{1}{M} V_{REF} - (-\frac{1}{M} \frac{V_{REF}}{2^{n+1}}) \right) \end{aligned} \tag{3.40}$$

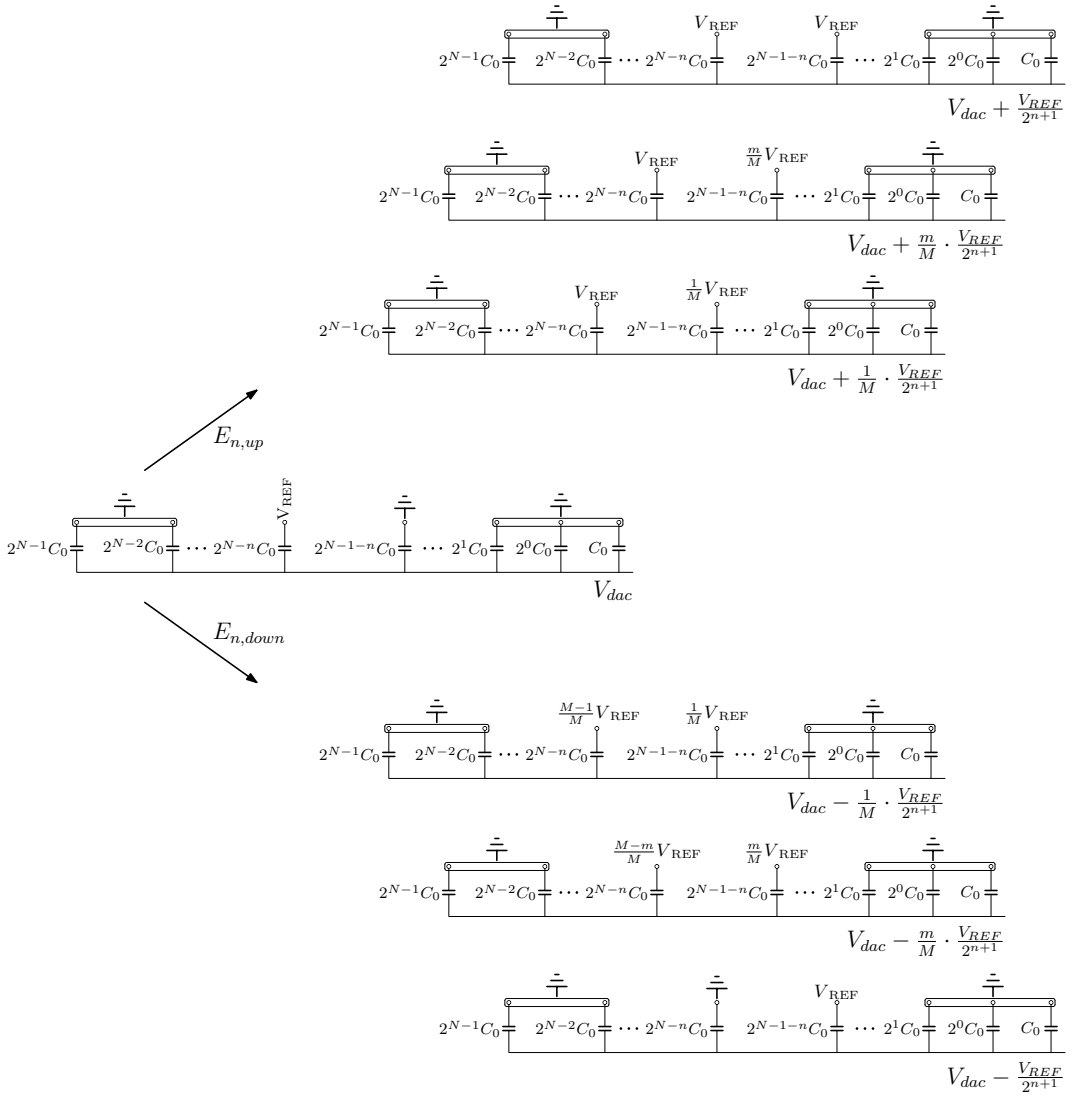


Figure 3.14.: Generalized switching fork of an n-th conversion step of an N-bit M-step stepwise conventional SAR ADC

The average energy consumption during the n-th conversion step can therefore be written as:

$$\overline{E_n} = \frac{\sum_{m=1}^{M} E_{n,m,up} + \sum_{m=1}^{M} E_{n,m,down}}{2} \tag{3.41}$$

Substituting the (3.39) and (3.40) into (3.41) yields the average switching energy during the n-th conversion step:

$$\overline{E_n} = \frac{1}{2} 2^{N-n} C_0 V_{REF}^2 \left[\left(1 - \frac{1}{2^{n+2}} \right) \frac{M+1}{M} - 1 \right] \tag{3.42}$$

The detailed derivation of the (3.42) can be found in the Appendix A.1.
The overall average DAC switching energy on an N-bit M-step stepwise conventional SAR ADC can therefore be expressed by summing up the (3.42) for all the conversion steps from 1 to N-1, adding the sample/hold energy consumption (3.38), and multiplying the result by 2 in accordance with (3.33):

$$\begin{aligned} \overline{E_{sw,DAC}} &= 2 \cdot \left[E_{S/H} + \sum_{n=1}^{N-1} \overline{E_n} \right] \\ &= 2^{N-2} C_0 V_{REF}^2 \frac{M+1}{M} + C_0 V_{REF}^2 \sum_{n=1}^{N-1} 2^{N-n} \left[\left(1 - \frac{1}{2^{n+2}} \right) \frac{M+1}{M} - 1 \right] \end{aligned} \tag{3.43}$$

In the case of a regular 1-step capacitor charging M=1, and (3.43) becomes:

$$\overline{E_{sw,DAC}} \overset{M=1}{=} C_0 V_{REF}^2 \left(2^{N-1} + \sum_{n=1}^{N-1} \left(2^{N-n} - 2^{N-2n-1} \right) \right) \tag{3.44}$$

Assuming an extreme case of stepwise charging when the number of steps approaches infinity, the term $\frac{M+1}{M}$ in (3.43) approaches 1, giving:

$$\overline{E_{sw,DAC}} \overset{M \to \infty}{=} C_0 V_{REF}^2 \left(2^{N-2} - \sum_{n=1}^{N-1} 2^{N-2n-2} \right) \tag{3.45}$$

Applying (3.44) and (3.45) to ADCs with various resolutions, the improvement in the energy consumption approximates 87.5% in each case as shown in the Table 3.1.
The average energy consumption for a variety of stepwise charging configurations is illustrated by the example of a 10-bit ADC in Fig. 3.15. As can be seen from the plot, introducing stepwise charging improves the energy consumption the most for 2-to-8-step charging, increasing the number of charging steps further is less and less beneficial as the plot approaches its asymptotic limit of $170.7 C_0 V_{REF}^2$.
Further analysis of the energy consumption of an N-bit stepwise conventional

Resolution N [bits]	8	10	12
$\mathbf{E_{avg,DAC,M=1}[C_0V_{REF}^2]}$	339.3	1363.3	5459.3
$\mathbf{E_{avg,DAC,M\to\infty}[C_0V_{REF}^2]}$	42.7	170.7	682.7
Reduction [%]	87.4	87.5	87.5

Table 3.1.: Switching energy improvement vs. resolution

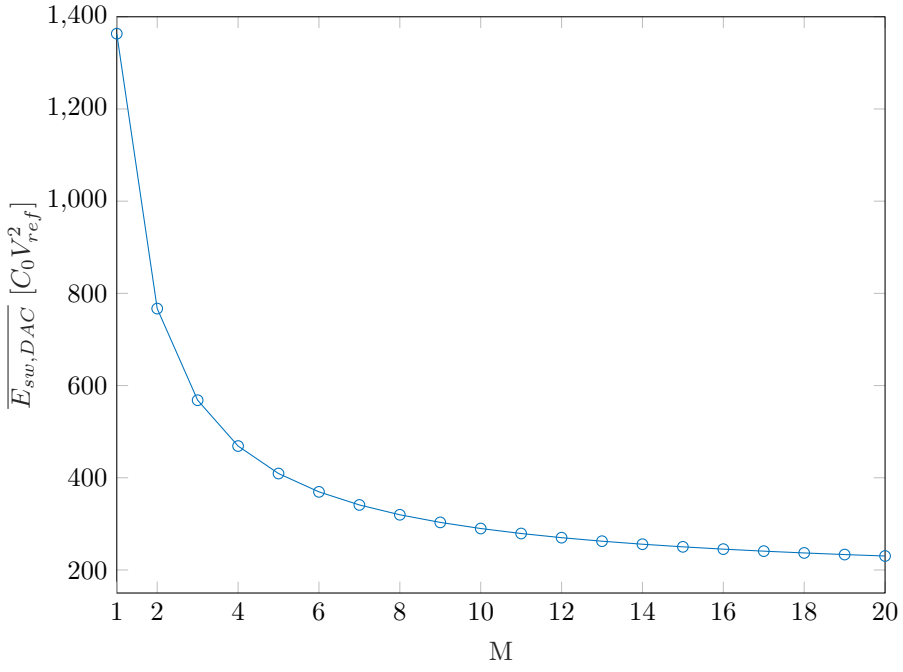


Figure 3.15.: Average DAC switching energy for N=10 bit for stepwise charging with various numbers of steps M

ADC with M-step charging can be demonstrated using MATLAB. The simulated MATLAB model is available in the appendix A.2. Figure 3.16 shows the codewise DAC switching energy of 10 different configurations of 10-bit ADCs: each waveform represents the codewise DAC energy of an ADC with 1- to 10-step stepwise charging approach applied. Notably, the asymmetrical plot of the regular 1-step conventional ADC restores the symmetry as the number of steps used in the charging process increases. The DAC switching procedure for the code 0 requires the DAC to perform only the downward transitions during each bit-cycle as opposed to the case of the full-scale input voltage (code 1024), where the DAC is only performing the upward transitions. As was shown in the section 3.4.1, the energy required for the downward transition in the case of a conventional switching scheme is more than for an upward transition since two capacitors have to switch simultaneously as opposed to only one. That causes the asymmetry in the codewise switching energy distribution. However, when stepwise switching is applied, improved charging efficiency eliminates the losses, improving the symmetry.

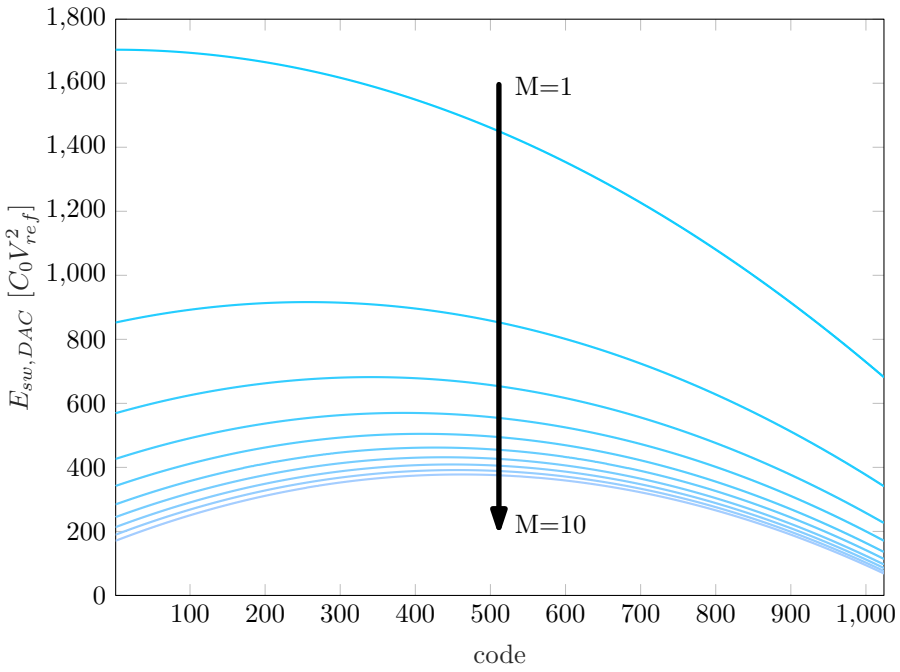


Figure 3.16.: DAC switching energy for N=10 bit vs. ADC output code for stepwise charging with various number of steps M

4 Implementation

4.1. Selection of a switching scheme for prototyping

The stepwise charging approach improves capacitor charging efficiency in general, and therefore it can be applied in conjunction with a variety of switching schemes. To select a scheme for the implementation, an important aspect is the sensitivity to the intermediate voltage source accuracy V_{cm}. As was mentioned in section 2.3, efficient and precise voltage conversion is possible if the load current is significantly larger than the quiescent currents of a converter, which can be the case if the converter is used on the system level for multiple purposes rather than only for the ADC. If the converter is used specifically to supply the ADC, the extra power consumed on biasing can be comparable to or even exceed the savings on DAC switching energy. The proof of concept for stepwise charging requires taking voltage sources' power consumption into account in order for the approach to be considered a standalone improvement applicable across various system-level conditions. The circuits that require precise reference voltage conversion were therefore not considered. Switching schemes with no such requirement are shown in Table 4.1.

Switching scheme	**Avg. s. energy**	**Reset energy**	**Total**	**Sensitivity to $V_{cm}/V_{ref}=1/2$**
Conventional	1363.3	0	1363.3	no
Monotonic [LCHL10]	255.5	0	255.5	-
VCM-based [ZCC+10]	170.17	0	170.17	no
Charge-redistribution [YKS16]	31.88	117.2	149.08	no
Yousefi [YDY18]	0	62	62	no

Table 4.1.: Comparison of SAR ADC switching schemes insensitive to V_{cm} to V_{ref} ratio. The provided values are for 10-bit resolution.

The switching scheme introduced by Yousefi, Dabbaghian, and Yavari [YDY18] only consumes energy during reset, distinguishing this scheme from the others. Although the stepwise switching could improve the reset energy as well, there are other factors influencing the decision. The [YDY18] switching scheme re-organizes the capacitors' connection rather than recharges them. The trade-off of that mechanism is high sensitivity to the charge injection due to the switches being placed at the comparator's inputs. Besides that, placing the switches at these parts of the circuit makes it susceptible to parasitics. As illustrated in Fig. 4.1, the routing from the capacitors' top plates to the switches becomes a part of the DAC's charge redistribution mechanism only during commutation, in contrast to the top-plate routing parasitics always being present in a typical star-topology. The former introduces code-dependent errors and affects linearity, whereas the latter doesn't have this issue and results only in a gain error reducing the input voltage range without affecting linearity. Therefore, for the Yousefi switching scheme, extra care is required to keep the routing to the switches identical. That is hard to achieve as the capacitor array is usually implemented as a large common-centroid structure placed separately from the switches.

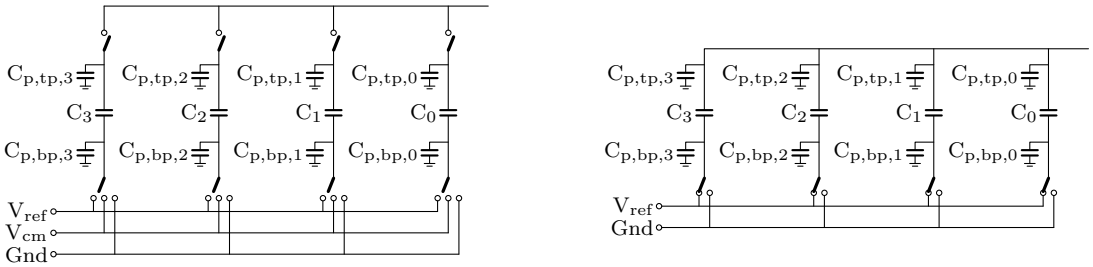


Figure 4.1.: Left: the case of [YDY18] introducing code-dependent commutation of the parasitics. Right: regular case, always present top-plate parasitic capacitance introducing gain error.

The charge-redistribution [YKS16] switching scheme's conversion tree is shown in Fig. 4.2. The switching scheme does not require V_{ref} and solely uses V_{cm} voltage during the conversion. Therefore in this scheme, V_{cm} sets the full-scale voltage and hence it is required for it to be stable and accurate. Effectively, V_{cm} replaces V_{ref} and sets the same requirements for the common-mode voltage source. Although in total there is still only one voltage reference required, using this scheme for supply voltages around 1-1.2V would require V_{cm} to be in the range of 0.5-0.6V which adds design challenges for such a source. Despite that, the charge redistribution scheme theoretically has potential if paired with stepwise charging: the energy consumption of the scheme happens mostly during the reset. It could be sufficient to use stepwise charging only during the reset phase to gain substantial benefits. However, to test the stepwise charging as a general approach it would not be

optimal to choose the switching scheme where the main savings would come from the reset energy reduction.

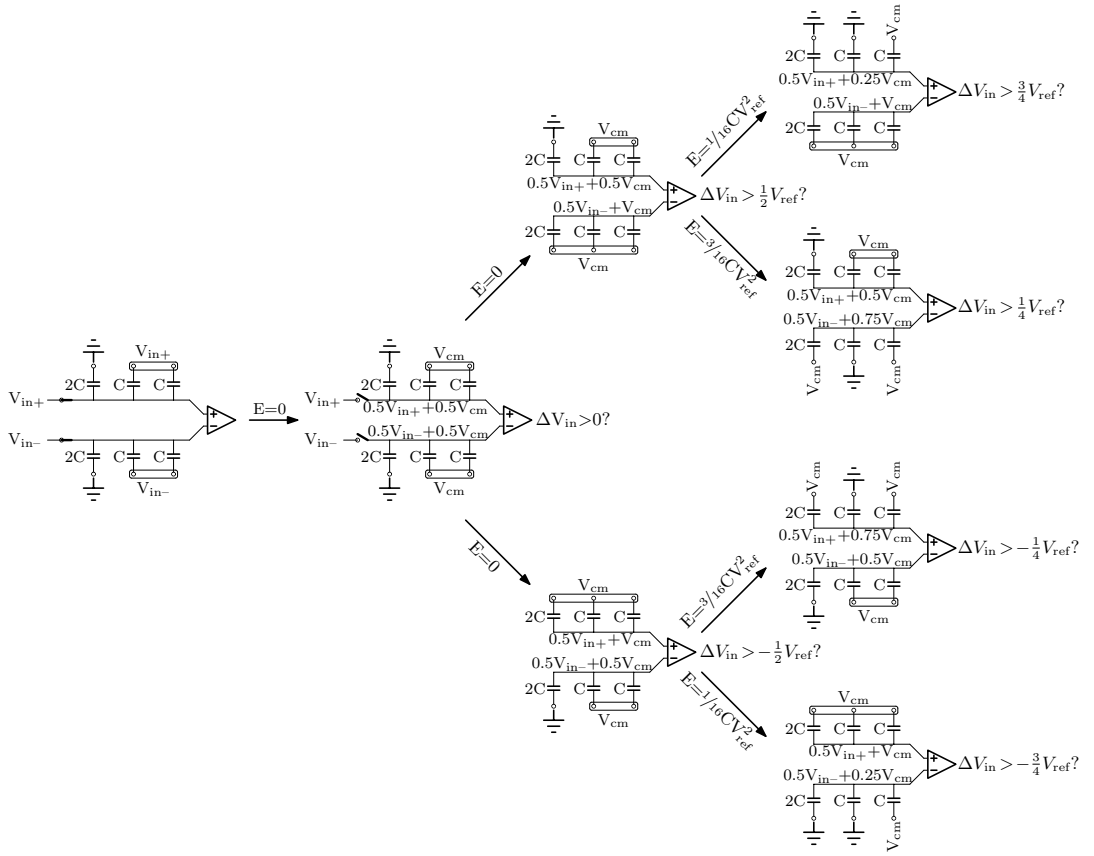


Figure 4.2.: Charge-redistribution [YKS16] switching scheme conversion tree. V_{cm}=0.5V_{ref}

Unlike the charge-redistribution scheme, the VCM-based [ZCC+10] switching scheme (Fig. 4.3) does not use V_{cm} exclusively, but in addition to V_{ref}. The use of intermediate voltage in this scheme helps with reducing the switching energy without relying on V_{cm} to set the full-scale voltage. Additionally, the switching is organized in a symmetric manner where V_{cm} is connected to both, positive and negative DACs via the same bit capacitors at all conversion steps. Such a connection makes the circuit tolerant to fluctuations in V_{cm} since they cancel out without affecting the differential voltage. The scheme also does not consume the power on reset phase, making it a suitable candidate for a proof of concept.

Another suitable choice for the switching scheme is the monotonic [LCHL10] scheme also referred to as set-and-down. The scheme's conversion tree is shown in Fig. 4.4. The idea of the monotonic switching scheme is to switch only one capacitor in only one DAC during every conversion step. As a result, it translates to one-directional transitions of either positive or negative DAC. If it is required to subtract a certain weight from the differential voltage, the positive DAC switches

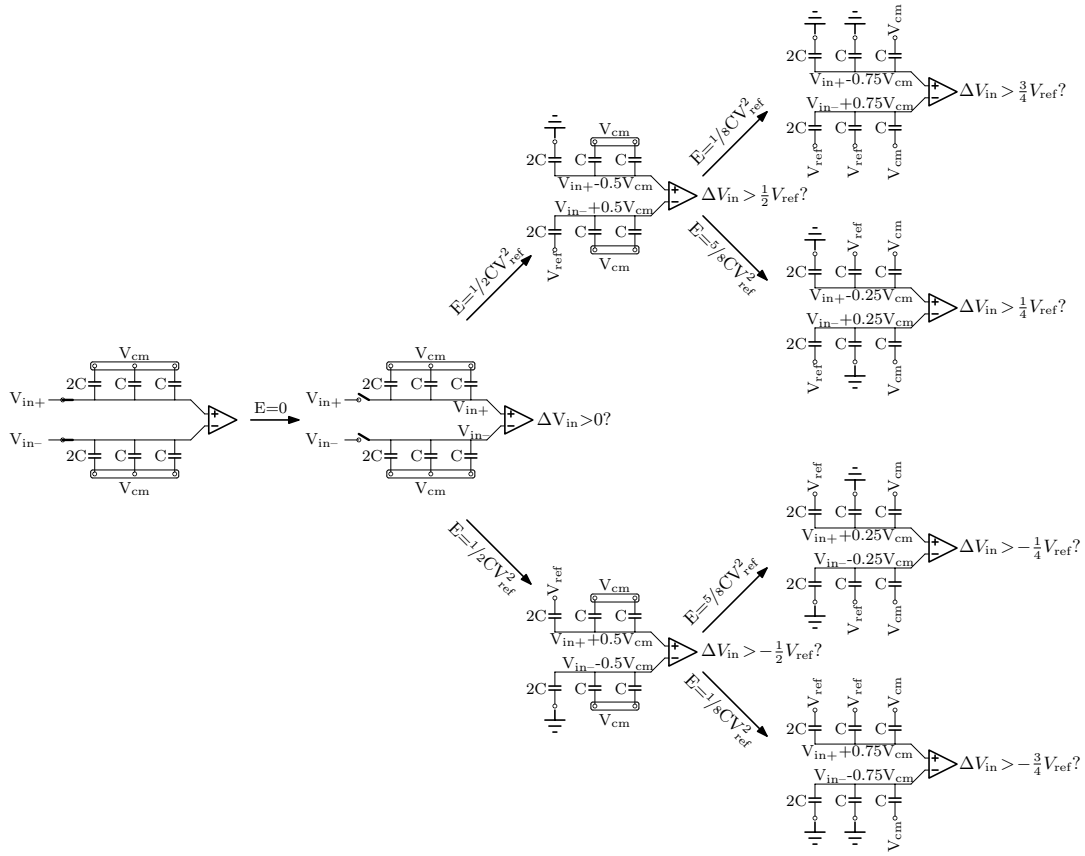


Figure 4.3.: VCM-based [ZCC+10] switching scheme conversion tree

down, and when it is required to add a certain weight, the positive DAC is kept set, but instead, the negative DAC performs a downward transition effectively increasing the differential voltage. The trade-off in this case is the common-mode component of the resulting differential voltage at the comparator's inputs. Since only one DAC takes a step down at every conversion step, the common mode component decreases by half of that value. In order to preserve the accuracy of comparison, extra care should be taken when designing a comparator for the monotonic switching scheme. A biased differential input stage is required to decrease the sensitivity of the gain to the common mode voltage, and the overall gain of the comparator should be large enough to keep the input-referred offset value fluctuation with common-mode voltage within appropriate limits. Besides the requirements for a more advanced comparator, the monotonic switching scheme shows significant energy efficiency, no reset power consumption, low control logic complexity, and it is the only scheme in the Table 4.1 that does not require a common mode voltage source.

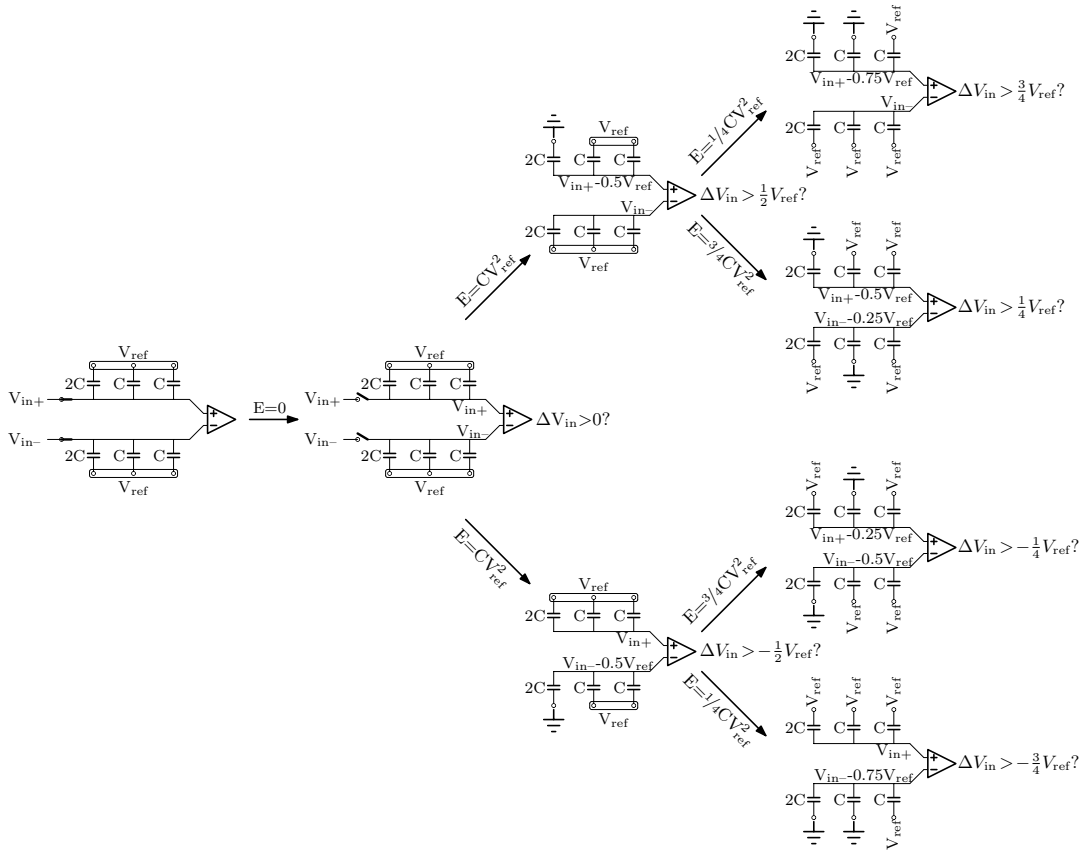


Figure 4.4.: Monotonic [LCHL10] switching scheme conversion tree

Both switching schemes, the VCM-based and Monotonic are suitable for applying the stepwise charging in a proof of concept prototype. They are both preferred over the conventional switching scheme for their higher energy efficiency, making

the proof of concept cover the application scenarios where DAC's power budget is more balanced within the overall ADC power consumption.
Although the VCM-based switching scheme uses the common-mode voltage source, the requirements for the accuracy of this voltage are low. Upon closer inspection, if V_{cm} in the VCM-based scheme in Fig. 4.3 is replaced with V_{ref}, the circuit would still be accurate, but it will essentially become identical to the monotonic switching scheme (Fig. 4.4). This demonstrates that the VCM-based switching scheme uses the common-mode voltage to trade the voltage drop on each DAC to reduce the switching energy. It is especially noticeable during the MSB decision: the VCM-based scheme consumes 2 times less power due to the quadratic relationship between the switching energy and voltage. If in the monotonic switching scheme only 1 MSB capacitor switches down from V_{ref} to Gnd, consuming $C_0V_{ref}^2$ Joules, in the case of the VCM-based scheme both DACs switch their MSB capacitors by $0.5V_{ref}$, reducing the voltage step twice, thus making each DAC energy consumption 4 times lower, which for both DACs gives in total $0.5C_0V_{ref}^2$ Joules. These savings are based on a similar principle of reduction of the voltage step as the stepwise charging. To better distinguish the benefits provided by stepwise charging from the benefits of the switching scheme, the monotonic switching scheme is preferable over the VCM-based for a proof-of-concept prototype.

4.1.1. Monotonic SAR as a platform

As mentioned in the previous chapter, the monotonic switching scheme utilizes a one-directional DAC switching approach to add or subtract a certain binary weight equivalent from the differential voltage. That eliminates the need to charge the other capacitors allowing to switch only one capacitor in only one DAC during each conversion step. The following disadvantage of that approach is that affects the common mode component of the resulting differential voltage. Since only one DAC changes the output voltage, the common mode component changes by half of this value. As a result, the common mode voltage at the DAC outputs during the sampling starts at $0.5V_{ref}$ and reduces to the 0.5LSB by the end of conversion. This behaviour is illustrated in Fig. 4.5 with the examples of two input voltages: on top is the full-scale positive differential input voltage conversion waveform and at the example at the bottom is the input signal slightly above differential zero, which matches the middle of the code range of the ADC within 1 LSB margin (01..11). In the case of negative full-scale input voltage or in the case of the voltage slightly below differential zero, the waveforms will be similar, except for the positive DAC voltage (solid) and negative DAC (dashed) interchange.

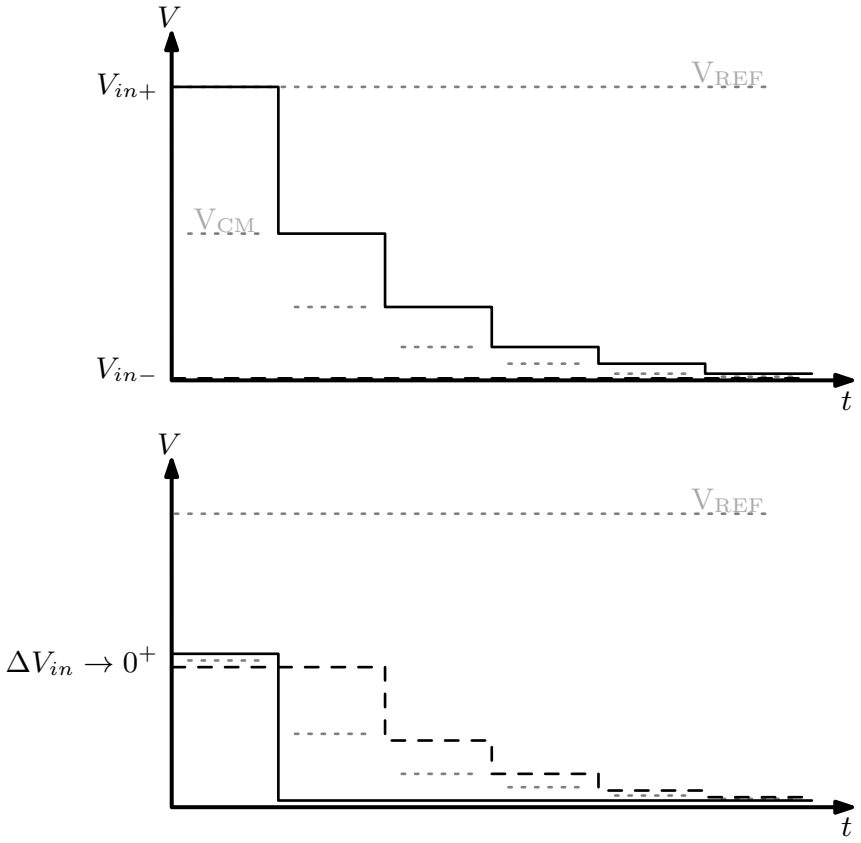


Figure 4.5.: Monotonic switching scheme common mode component variation during the conversion

The gain of the comparator can be sensitive to common-mode fluctuations, and since the input-referred offset of the comparator is dependent on the gain value, the resulting input-referred offset voltage of the comparator will be different for every conversion step, causing the loss in accuracy. Therefore, this dynamic offset issue should be addressed in the design of the comparator.

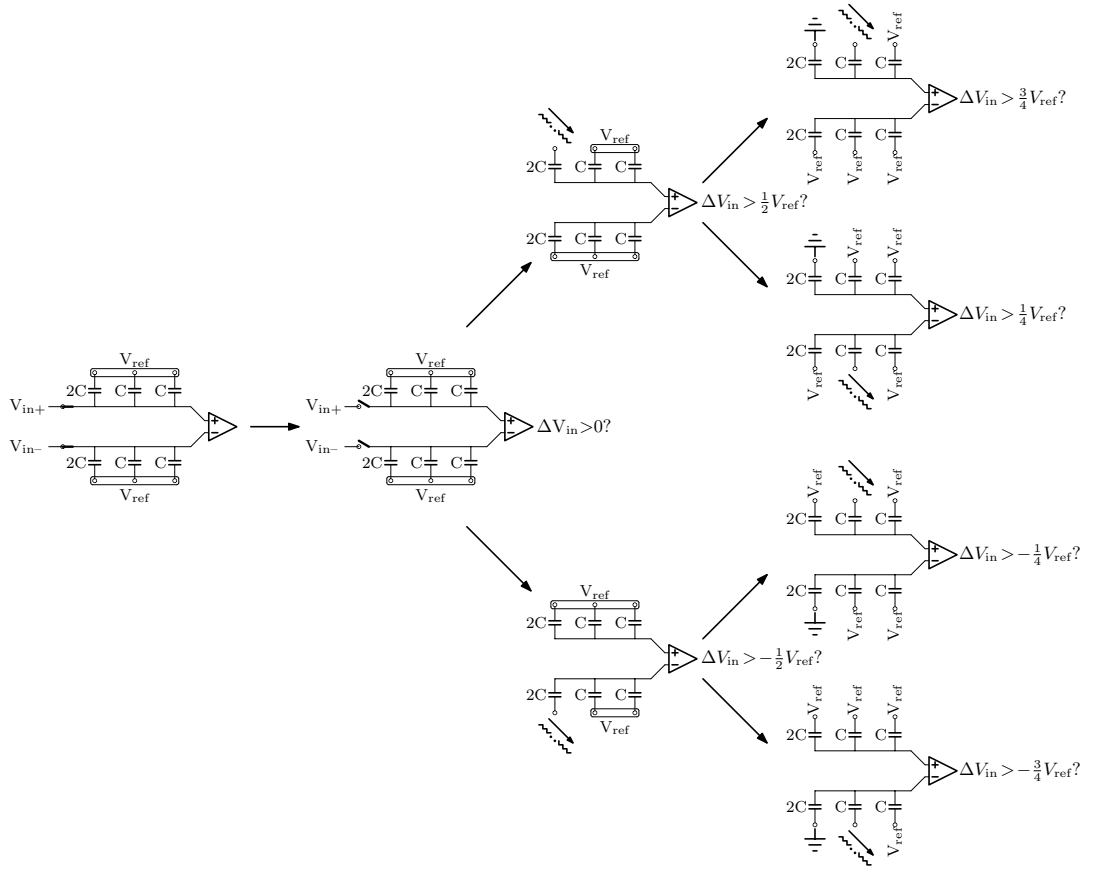


Figure 4.6.: 3-bit monotonic switching scheme conversion tree with applied stepwise charging

The monotonic switching scheme modified with the stepwise charging is shown in Fig. 4.6. Every active downward switching is replaced with a series of smaller voltage steps discharging the capacitor bottom plate from V_{ref} to Gnd. The DAC output waveform therefore becomes as shown in Fig. 4.7. The number of steps is the same for each conversion cycle and the voltage steps are equidistant. The exact step voltage is a fraction of the binary weight voltage equivalent that is being subtracted during a given conversion cycle. Thus, as the weights are consequently reducing during the conversion, so are the output voltage steps.

The energy consumption of the DAC in the case of the monotonic switching scheme for various numbers of charging steps was calculated using MATLAB. The script is presented in the Appendix A.3. The family of plots in Fig. 4.8 shows how the codewise energy consumption reduces with increasing the number of charging

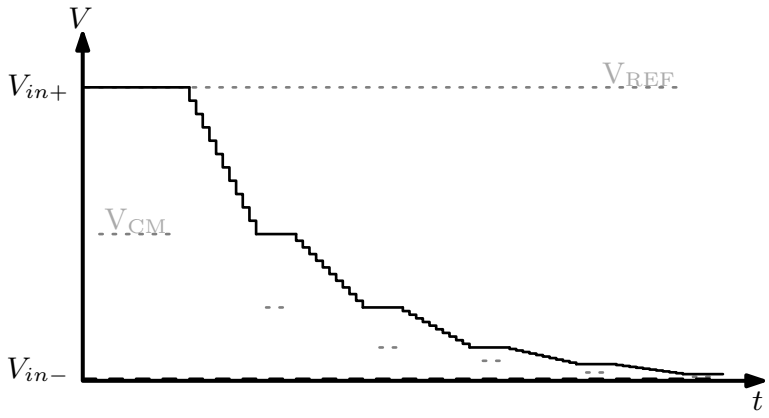


Figure 4.7.: Monotonic switching DAC output voltage with applied stepwise charging

steps used in the 10-bit monotonic SAR ADC. The average energy consumption for every stepwise charging configuration is then plotted in Fig. 4.9.

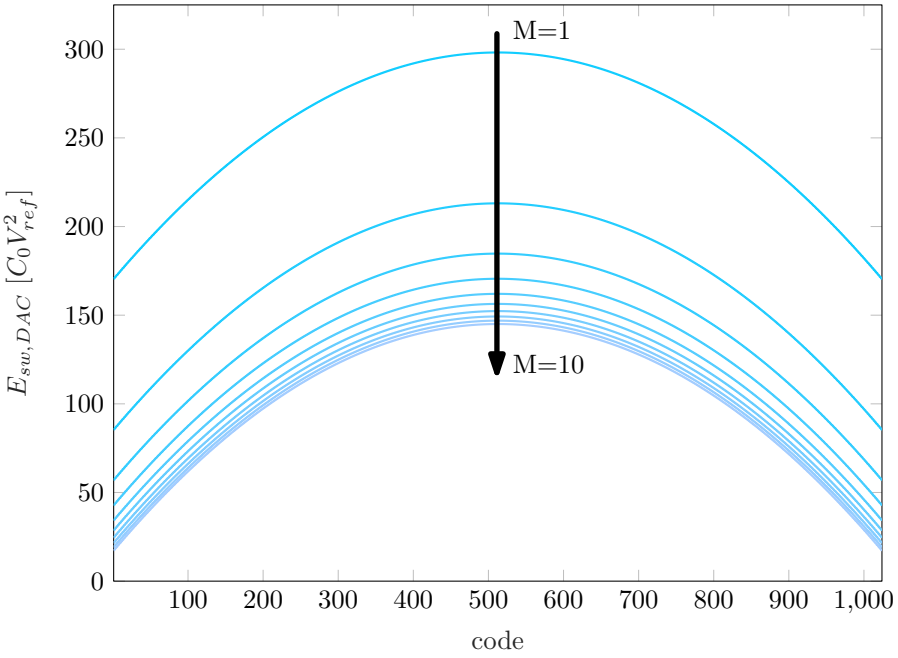


Figure 4.8.: 10-bit monotonic ADC's DAC switching energy vs. output code for stepwise charging with various numbers of steps M

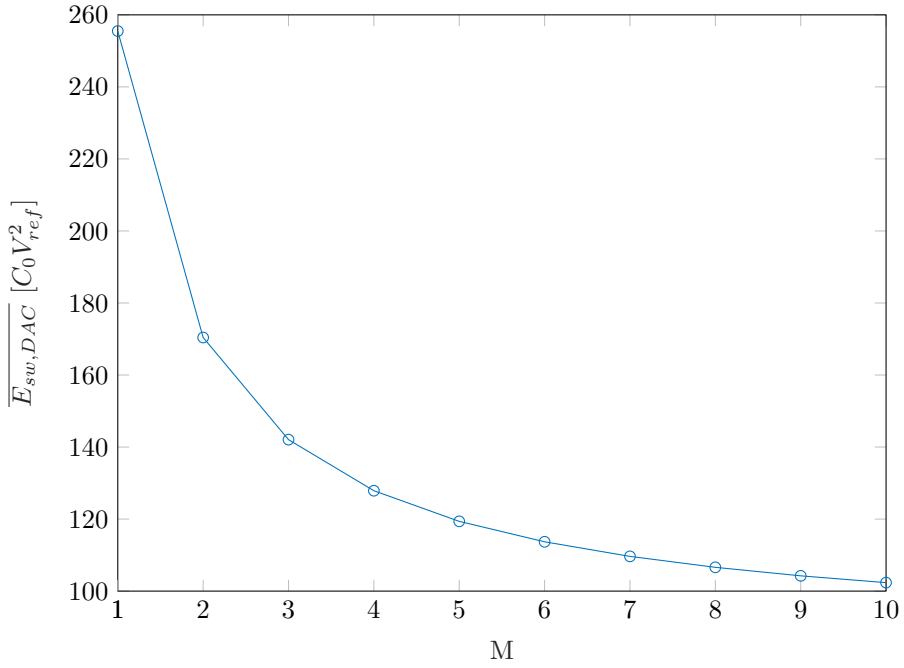


Figure 4.9.: Average DAC switching energy for 10-bit resolution for stepwise charging with various numbers of steps M

4.1.2. Intermediate voltage generator

An important aspect of the implementation of the stepwise charging DAC is taking the intermediate voltage sources into account. The number of charging steps can be large and therefore the usability and efficiency of the approach should be considered in conjunction with the intermediate voltage sources.

The requirements for such a source are mainly related to its efficiency. The initial and the final step voltages in the charging sequence are responsible for the accuracy of the conversion since only they are connected during the comparison. The intermediate voltage sources are therefore only used to provide the charging efficiency improvement.

The choice of the voltage converter to use for such purpose includes LDO, switched-inductor, and switched-capacitor topologies. The use of multiple LDOs is excessive in regard to power consumption, and the stability of the output voltage that LDO can provide is not required for stepwise charging. The switched-inductor converter can be ruled out as inductors are difficult to implement on-chip due to their generally large area and extra process options required to produce an on-chip inductor. The switched-capacitor DC-DC converter circuits are among the most efficient converters that can occupy smaller areas than switched-inductor-based ones. The output voltage ripple being the main disadvantage of this topology does not create a major issue for the stepwise charging application since the accuracy will not be affected by intermediate voltage ripple. It is also easier to implement

on-chip since no extra process options are required on top of the capacitor-related options that are already necessary for the SC-DAC.

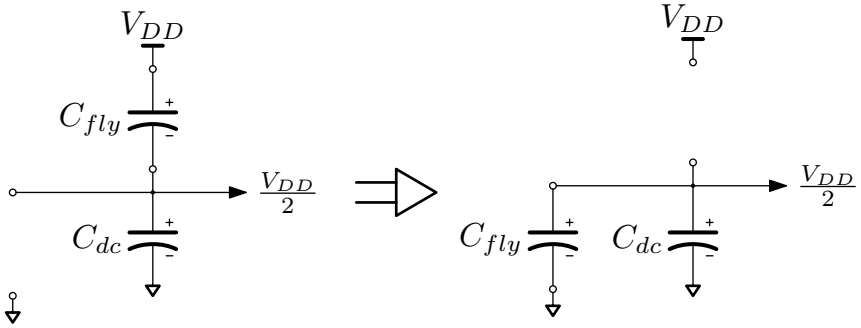


Figure 4.10.: Step-down DC-DC voltage converter

Figure 4.10 shows the principle of operation of the step-down switched-capacitor DC-DC converter. In this topology, two capacitors are being switched between series and parallel connections dividing the supply voltage by a factor of two. The topology in Fig. 4.12 uses an additional flying capacitor during the opposite clock phase to reduce the output voltage ripple.

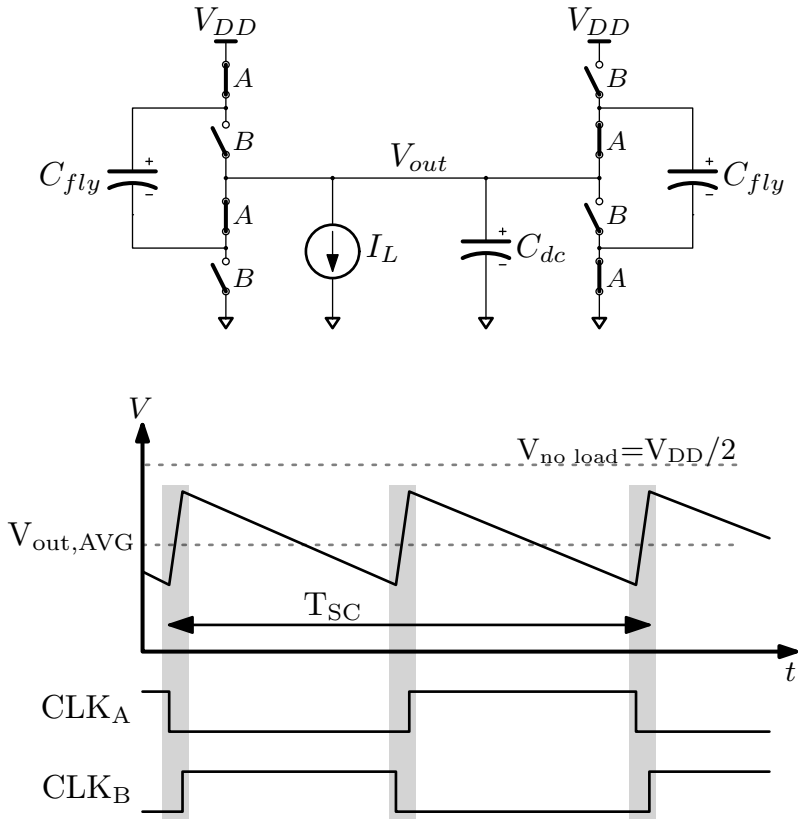


Figure 4.11.: Two-phase 2:1 DC-DC voltage converter (Top), the output voltage ripple waveform (Bottom). Image from [BSC+16]

According to [BSC+16] in a multi-phase converter when the load current source

I_L is connected to the output, the ripple voltage of this circuit will depend on the switching period T_{SC}, the number of phases N_{PH} and the total storing capacitance of the converter C_{tank}=C_{dc}+C_{fly}. The voltage can be expressed as:

$$V_{ripple} = \frac{I_L T_{SC}}{N_{PH} C_{tank}} \tag{4.1}$$

If the converter is used to supply a switched-capacitor circuit, there is no DC load current I_L apart from the leakage to provide a linear output voltage slope. Instead, the output voltage changes upon the connection due to the charge redistribution. If the converter is capable of injecting the withdrawn charge within one cycle, the output voltage can be restored in the next phase.

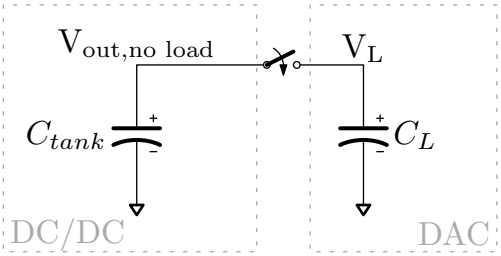


Figure 4.12.: Simplified circuit showing the charging of a capacitor using an SC converter

Figure 4.12 shows the simplified circuit used to estimate the resulting output voltage drop when the capacitive load is connected to the converter's output. Assuming the load is a DAC capacitor undergoing the stepwise charging procedure, the load capacitor can have a certain initial voltage as a residue from a previous charging step. The initial load voltage is marked in the figure as V_L. The resulting voltage V_{res} is derived assuming that the sum of the charges of the two capacitors will stay the same after the commutation due to the charge conservation principle, yielding:

$$Q_{tank,ini} + Q_{L,ini} = Q_{res} \tag{4.2}$$

$$C_{tank} V_{out,n.l.} + C_L V_L = (C_{tank} + C_L) V_{res} \tag{4.3}$$

The resulting voltage can be derived from (4.3) as:

$$V_{res} = V_{out,n.l.} \frac{C_{tank}}{C_{tank} + C_L} + V_L \left(1 - \frac{C_{tank}}{C_{tank} + C_L}\right) \tag{4.4}$$

During the AD conversion, the load capacitance varies every conversion cycle: depending on which capacitor is currently being switched, the effective load capacitance is represented by the series connection of the active capacitor with the rest

of the capacitors in the DAC. Therefore, the charge redistribution is the largest during the MSB decision and becomes smaller further down the conversion since the effective load capacitance reduces. Figure 4.13 shows an example of the stepwise discharging of MSB capacitor using 4 steps. SC voltage converters generating intermediate voltages are represented as their tank capacitances C_{tank}=C. During the stepwise discharging process, the voltage on each tank rises upon commutation and stays as is until SC converter restores it, returning the energy back to the voltage source. The residual voltages according to (4.4) are shown at the bottom of Figure 4.13.

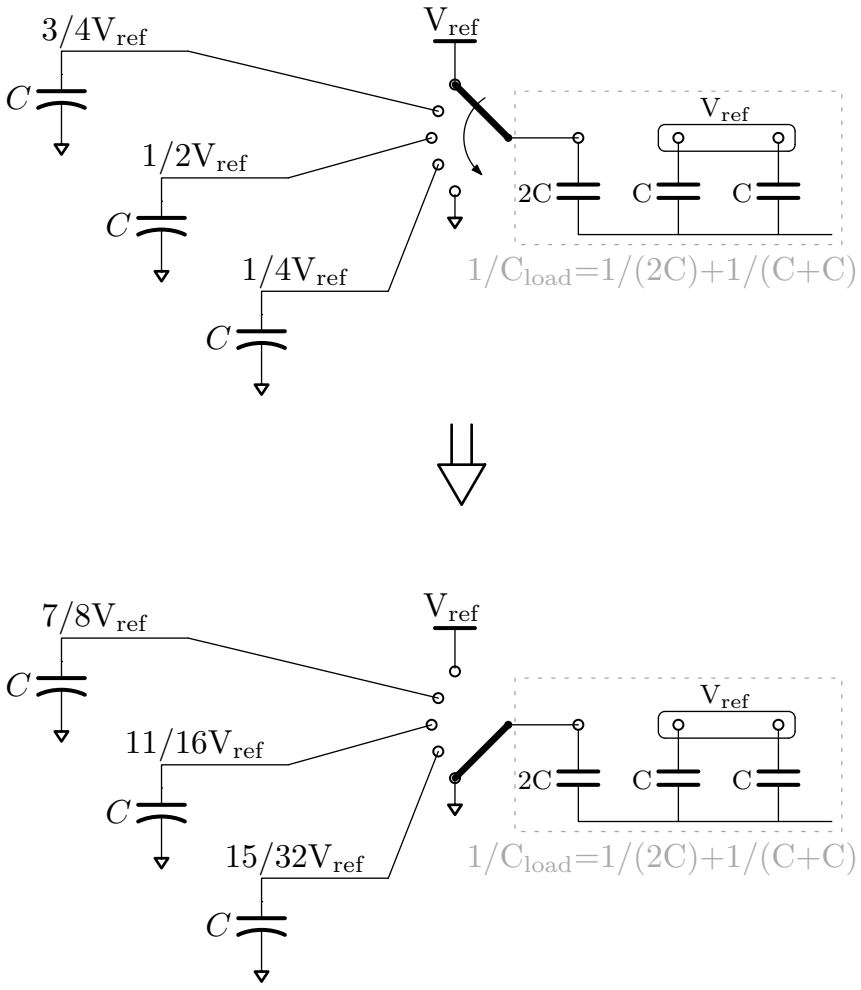


Figure 4.13.: MSB switching using 4-step charging via capacitor tanks

If instead of capacitor tanks, voltage sources had been used, the energy consumption from each source would have been expressed similarly to how it was described in Chapter 3.4.1 in the equation (3.24). For the case of stepwise charging via capacitor tanks, this approach can not be applied directly since there is no voltage source. The energy consumption can be found by comparing residual energy stored in a capacitor tank with its initial energy. The energy stored in a capacitor

C, if it is charged to a voltage V, equals to $\frac{CV^2}{2}$. The difference in stored energy in the capacitor tank prior to and after the commutation can therefore be derived as:

$$E = \frac{C_{tank}V_{out,n.l.}^2}{2} - \frac{C_{tank}V_{res}^2}{2} \tag{4.5}$$

Applied to each capacitor tank, (4.5) gives the energy withdrawn from each SC converter.

If the converter is considered to be ideal, the same energy would be required to restore the voltage at the SC converters back to the idle state. However, due to the non-100% efficiency of capacitor charging, the energy required to restore the voltage will be higher than the withdrawn energy. The efficiency of the charging process in the case of SC converter is not 50% as it would have been in the case of charging a capacitor from 0 to VDD with 1 voltage step (see chapter 3.1). Since the capacitor tank is not drained out completely, the residual voltage improves the efficiency of topping up the charge in the tank. This can be illustrated by the example of a 1-phase 2:1 step-down converter (same as in Fig. 4.10) with equal sizes of C_{fly} and C_{dc}. C_{tank} in that case is represented by the sum of the two capacitors, and therefore each of them represents half of C_{tank}. The energy transfer between the load and the converter is shown in Figure 4.14.

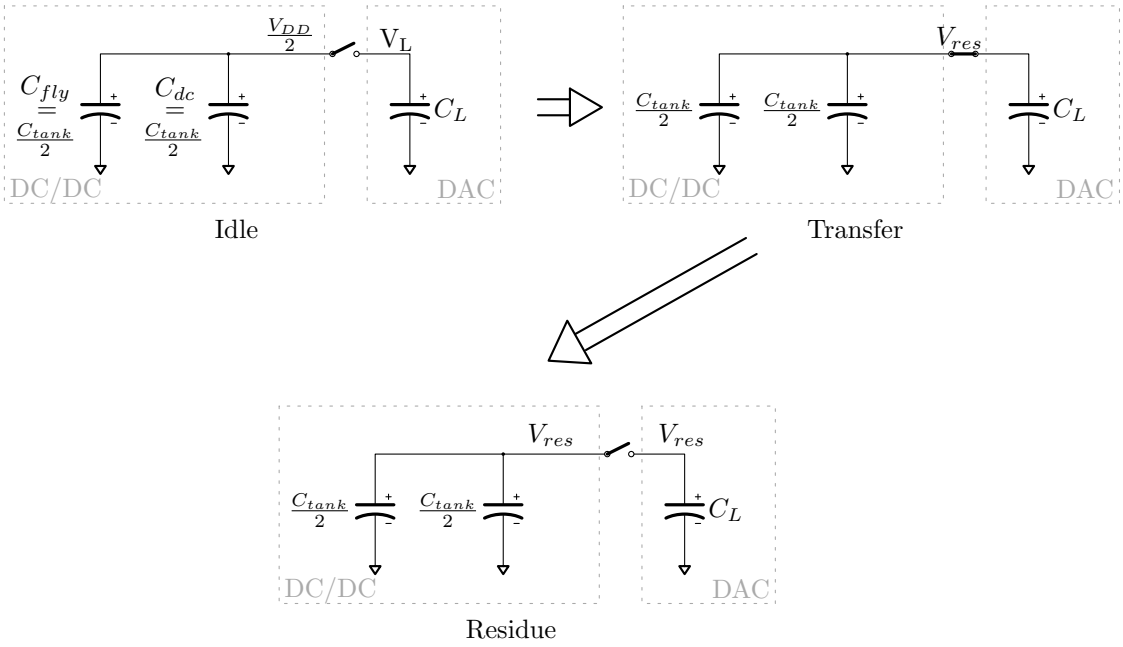


Figure 4.14.: The energy transfer between the DC-DC converter and the load capacitance represented by DAC

The difference in stored energy between the idle (E_{idle}) and residual (E_{res}) states

is the withdrawn energy E_{wthd}. This is the same energy that was described by (4.5), which gives:

$$E_{wthd} = E_{idle} - E_{res} = \frac{C_{tank}(0{,}5V_{DD})^2}{2} - \frac{C_{tank}V_{res}^2}{2} \tag{4.6}$$

To restore the voltage at the output, the converter's capacitors are reconfigured to the series connection and charged to VDD as shown in Fig. 4.15. Each capacitor has the same voltage across the plates, therefore the voltage of the stack is doubled.

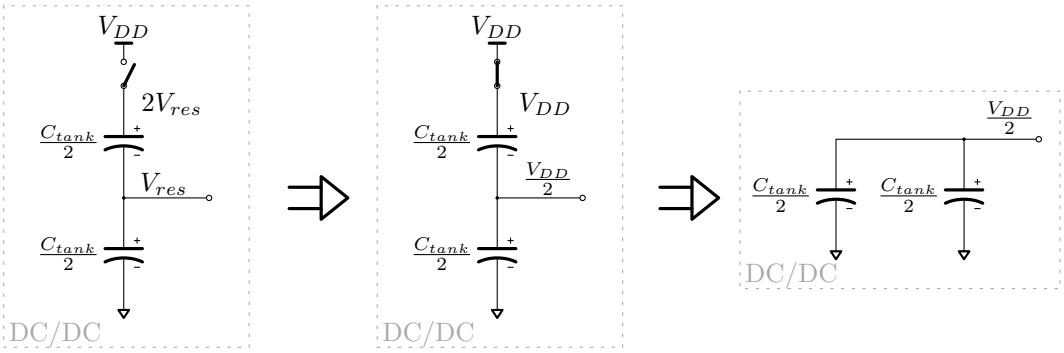


Figure 4.15.: DC-DC converter restoring the charge

The effective capacitance being charged is the series connection of the two, equals $\frac{C_{tank}}{4}$. Charging this capacitor from $2V_{res}$ to VDD requires the energy E_{ch} of:

$$E_{ch} = \frac{C_{tank}}{4}V_{DD}(V_{DD} - 2V_{res}) \tag{4.7}$$

The ratio between the withdrawn energy and the energy required to charge the SC converter back to the idle state can therefore be derived as a ratio between (4.6) and (4.7) which gives:

$$\eta = \frac{E_{wthd}}{E_{ch}} = \frac{1}{2} + \frac{V_{res}}{V_{DD}} \tag{4.8}$$

If the load capacitor's initial voltage V_L is lower than the idle voltage of the converter $\frac{V_{DD}}{2}$, the voltage upon commutation will drop, so that V_{res} is lower than $\frac{V_{DD}}{2}$, resulting in the efficiency less than 1. It indicates that the energy E_{ch} required to restore the withdrawn charge is more than the withdrawn energy.
If V_L is higher than $\frac{V_{DD}}{2}$, the voltage upon commutation rises, meaning that the energy is transferred to the converter's capacitor tank and not withdrawn from it. This results in the negative value in (4.6) and η larger than 1 since the energy was delivered to the converter's output. In terms of the energy consumption that indicates that less energy was transferred back to the voltage source VDD

upon voltage restoration than it was delivered to the converter's output from the load. This can be further illustrated using the previously mentioned example of discharging the MSB capacitor of the DAC matrix with 4 steps (Fig. 4.13). The middle capacitor tank with the initial voltage of $\frac{V_{ref}}{2}$ has a capacitance value of C. This tank can be represented by the 2:1 step-down SC converter with C_{tank}=C. This converter has an idle voltage of $\frac{V_{ref}}{2}$. The initial voltage at the load capacitor prior to commutation equals the residual voltage from the previous charging step: $V_L = \frac{7V_{ref}}{8}$. That voltage is larger than the idle voltage of the converter and therefore the energy will be transferred to the converter's output and the resulting voltage from the converter's perspective will rise. Residual voltage upon commutation can then be found using expression (4.4) which gives $V_{res} = \frac{11V_{ref}}{16}$. Substituting this value into (4.6) and deriving the E_{ch} from (4.8) gives:

$$E_{ch} = \frac{E_{wthd}}{\eta} = \frac{-0{,}111CV_{ref}^2}{1{,}1875} = -0{,}09CV_{ref}^2 \tag{4.9}$$

In the case of transferring energy to the SC converter's output, the result of (4.9) indicates that $0{,}09CV_{ref}^2$ Joules was delivered to the voltage source, which is less than $0{,}111CV_{ref}^2$ Joules that was delivered from DAC to the converter's tank.
The efficiency of the energy transfer η (4.8) is different for other converter's architectures and conversion ratios. For the different ratios between C_{fly} and C_{dc}, different numbers of charging phases, and charging the converter with multiple steps, the restored energy (4.7) will be expressed differently. However, the overall trend of the efficiency dependency on the voltage drop is presented in the switched-capacitor voltage converters in general.
To estimate the influence of stepwise charging via SC converters, the Matlab model (A.4) of the stepwise monotonic switching SAR ADC has been designed to include the energy transfer and charge redistribution depending on the size of the capacitor tanks. In this model, the energy transfer was calculated as (4.5), omitting η, so the model is independent of the topologies of various converters that might be used to generate the intermediate voltages. Since the SC converter's performance improves with the tank size, the downside to it is the occupied area. The tank's capacitance was therefore expressed as a value related to the unit capacitance to tie the tank size to the capacitance of the DAC. Then, the sum of all the capacitor tanks in the SC converters required for a given number of charging steps can be used as a limiting parameter. For the number of steps M

that requires M-1 intermediate voltage steps and gives the tank capacitance value for each converter:

$$C_{tank,1...M} = \frac{\text{Total converters' capacitance}}{M-1} \tag{4.10}$$

The total capacitance does not translate to the on-chip area the same way for the SC converters as for the DAC matrix. Due to the common centroid placement that is usually applied to the DAC unit capacitors' to improve matching, DAC represents an array of the unit capacitors placed within a certain distance of each other to comply with the minimal spacing allowed by the PDK manufacturer and to leave space for the routing. For the equivalent total capacitance value, a DAC occupies a significantly larger area on the chip compared to an SC converter, where the fly- and dc- capacitors don't require common centroid placement. Nevertheless, limiting the area dedicated to the SC converters allows to derive the area-limited curves for comparison between different configurations. The excess area can be set for each curve, whereas the number of charging steps can vary. An example of such a family of curves for 10-bit monotonic SAR ADC is shown in Figure 4.16. The dashed line shows the energy consumption without charge redistribution, and the 4 other solid lines show the DAC average switching energy for the limited excess areas dedicated to the SC converters' placement. From the closest to the no-redistribution limit to the farthest, the areas are $4096C_0$, $2048C_0$, $1024C_0$ and $512C_0$.

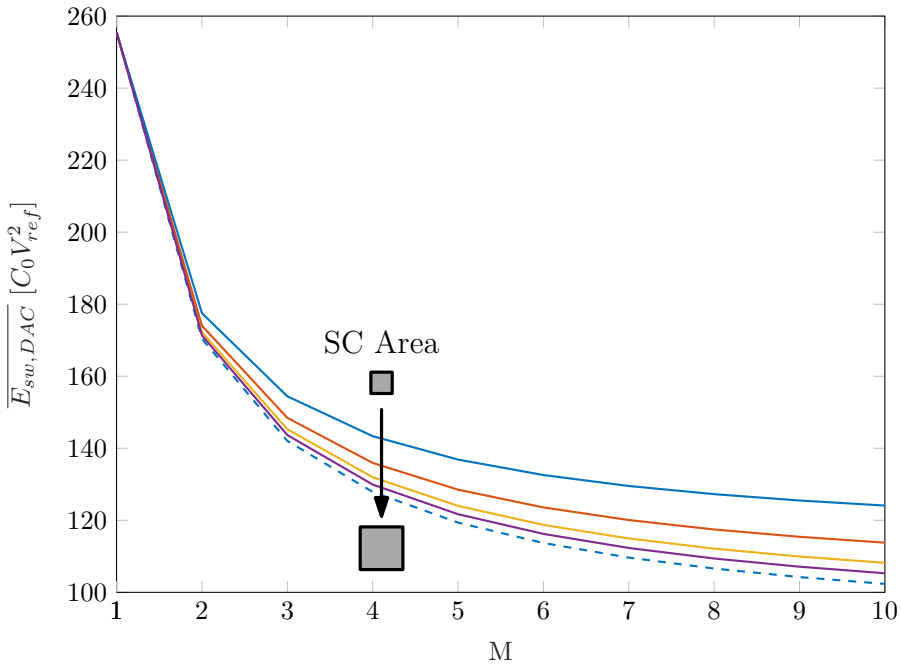


Figure 4.16.: Area limited average DAC switching energy for 10-bit resolution vs number of steps M. SC areas: 512,1024,2048,4096

If SC converters are considered to have MOSFET switches, the parasitic capacitances introduce additional energy losses. Assuming a simplified case with equal losses for each converter, the overall loss due to the parasitics will grow linearly with the number of steps. Applied to the ADC, this increasing influence overpowers the decreasing trend of the energy consumption causing it to grow with the number of steps after a certain point creating a minimum for each curve. Applied to the 10-bit ADC from Fig. 4.16, assuming that each converter after being connected to the DAC always restores its voltage with energy loss $E_{loss}=0.5C_0V^2_{ref}$ (Variable Loss=0.5 in A.4), that gives the results shown in Figure 4.17. The energy consumption shows high sensitivity to the losses as they grow linearly with the number of steps. In practice, it can be adjusted by applying the stepwise charging to only those capacitors in the DAC, where energy benefits overweight the penalty caused by the losses. Alternatively, the charge in the converters can be restored less often, relying on larger capacitor tanks to limit the charge redistribution.

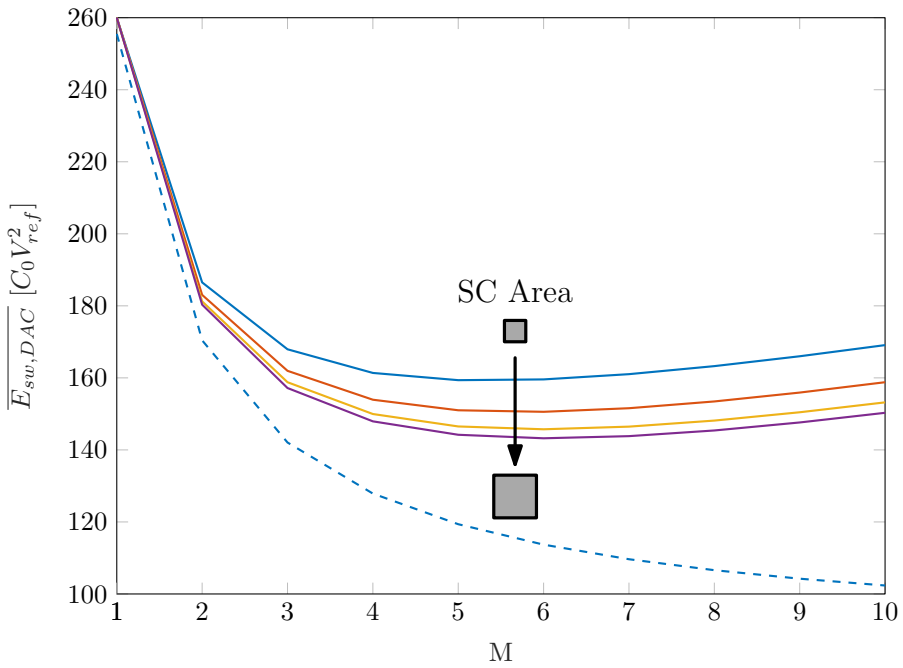


Figure 4.17.: Area limited average DAC switching energy for 10-bit resolution vs number of steps M, including losses in SC converter parasitic capacitances. SC areas: 512,1024,2048,4096. $E_{loss}=0.5C_0V^2_{ref}$

The SC DC-DC converters for the ADC prototype were designed using the 2:1 step-down approach applied in stages to divide the voltage further. The initial step-down converter divides the reference voltage by 2. The next stage has 2 converters with the same topology: one divides the voltage between the output of the previous stage and the ground, and the other does the same between the output and the reference voltage. Applying this approach further allows to

generate the voltage division in 2^n fashion where n is the number of stages. The 4-step stepwise charging requires 5 voltage levels, two of which are ground and the reference voltage. The 3 intermediate voltage levels can then be generated using the 2-stage step-down converter as shown in Figure 4.18. The disadvantage of this approach is decreased efficiency of the energy transfer for further stages as they recharge through the previous ones.

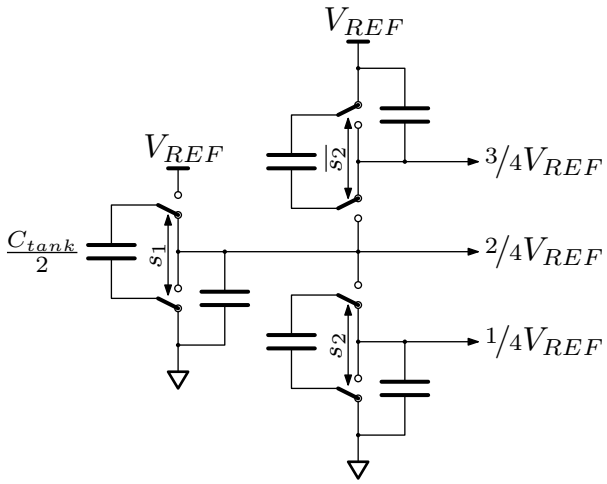


Figure 4.18.: 2-stage step-down SC converter for 4-step capacitor charging

Starting from the 3rd stage the architecture begins to produce outputs with reduced effective tank capacitance. This can be demonstrated using an example of the SC converter for 8-step charging. In Figure 4.19 these outputs are $^3/_8V_{ref}$ and $^5/_8V_{ref}$. These outputs are generated by the step-down converters that are connected between the two outputs of the previous stages. When the capacitors producing $^3/_8$ and $^5/_8V_{ref}$ are connected in parallel, they are not connected to the voltage source or the ground voltage as all the rest, but instead, they are connected to the previous stage. Effectively that results in a series connection of the two thank capacitors, reducing the overall storing capacitance for these outputs by two.

The energy consumption of the monotonic SAR ADC in conjunction with SC DC-DC converters using the staged 2:1 step-down architecture was simulated using SPICE using the UMC 65nm process, and reported in [1]. The simulation naturally includes the converter's charging efficiency η, and to include the charging losses the switches in the converters were implemented using MOSFETs. To restore the charge, all the stages were switched between the series and parallel connection upon every commutation with the DAC at every charging step. The overall capacitance dedicated to the SC converters was decided to be $2048C_0$, which is 2x total DAC capacitance for the 10-bit resolution. The DAC was designed using MIM capacitors of minimum size - 51.16fF. The DAC switches were implemented

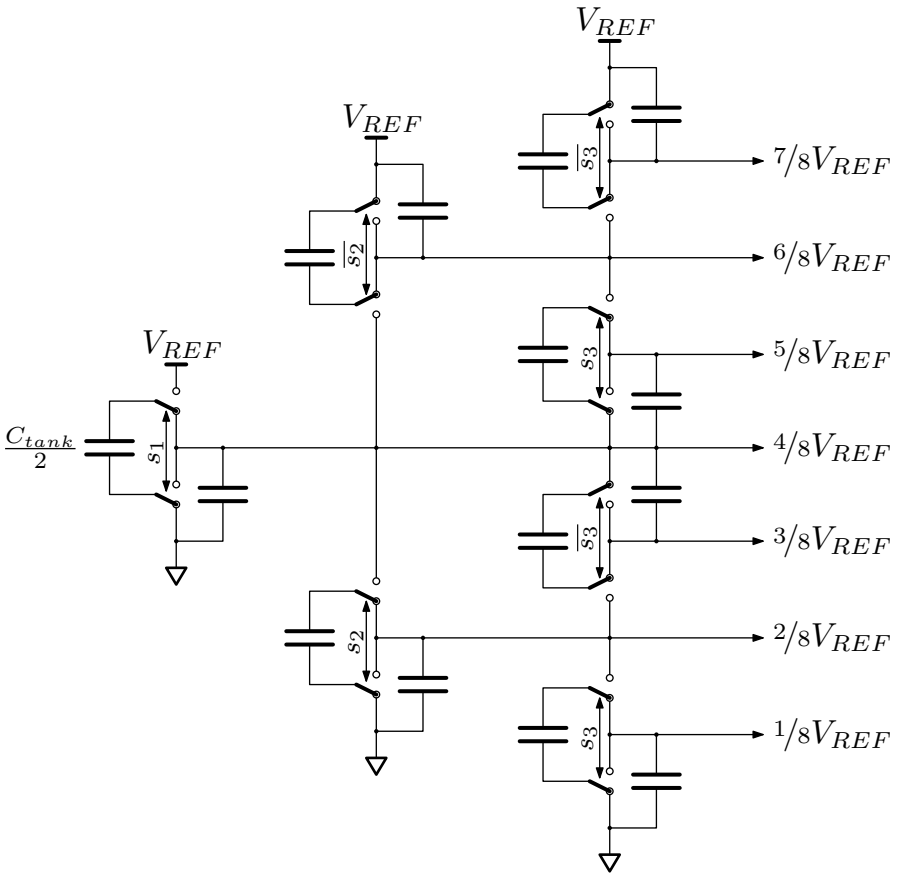


Figure 4.19.: 3-stage step-down SC converter for 8-step capacitor charging

on the transistor level as well. The rest of the ADC was implemented using ideal elements and Verilog-A modules. The simulation was made by applying the full-scale differential voltage ramp that was then converted with a 100kS/s sampling rate. The energy consumed at each conversion was captured using a Verilog-A module and then exported to MATLAB to plot the results.
In total, 4 ADC architectures have been simulated: the control, 1-step charging monotonic SAR ADC, and 2-, 4-, and 8-step charging ADCs with the SC converters designed accordingly for each architecture keeping the total SC converter capacitance same in each case. The code-wise switching energy for each case is shown in Figure 4.20. The average energy consumption in the case of 1-step charging amounted to 259.7 $C_0V_{ref}^2$, for 2-step - 180.7 $C_0V_{ref}^2$, for 4-step - 146.8 $C_0V_{ref}^2$ and for 8-step - 150.3 $C_0V_{ref}^2$. The results show that for the 8-step charging configuration, the energy losses and SC converters' efficiency overpowered the benefits compared to the 4-step charging configuration. Therefore, based on these results, the further development of the proof-of-concept prototype was selected to feature the 4-step charging.

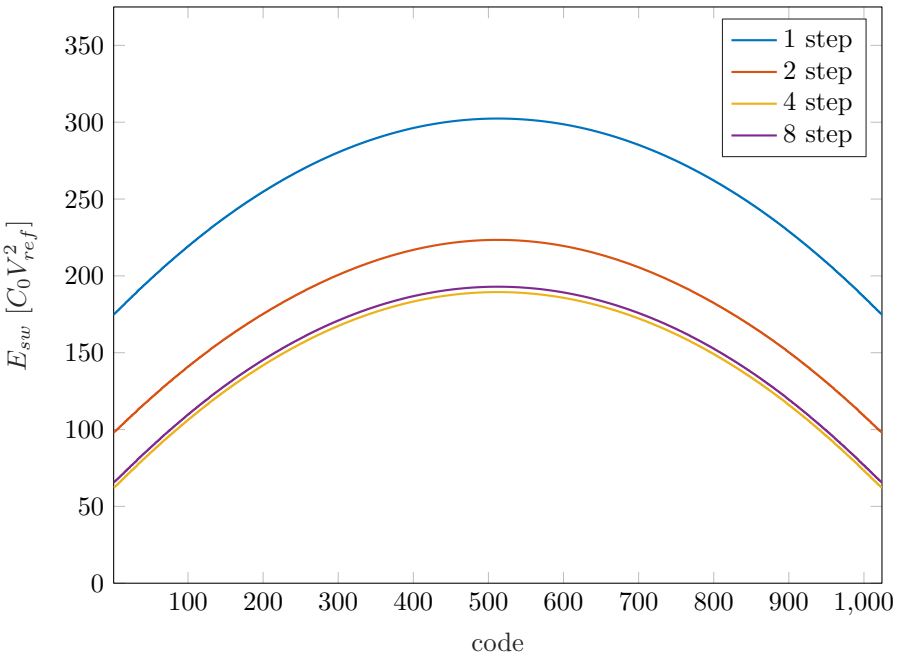


Figure 4.20.: Simulated code-wise switching energy of 4 10-bit monotonic SAR ADCs using 1-, 2-, 4-, and 8-step charging [1].

4.2. Adiabatic charging SAR ADC prototype

4.2.1. Block diagram of the ADC

The resulting block diagram of the 10-bit 4-step charging monotonic switching SAR ADC prototype is shown in Figure 4.21. The ADC operates asynchronously and generates an internal clock signal using the comparator's outputs and delay chain. The 90-degree phase-shifted clock is taken from the middle of the delay chain in order to generate and synchronize the 4 distinct cycles for the 4-step charging procedure. These clock signals are connected to the switch controllers, marked on the block diagram as CTRL. In addition, each switch controller receives an according control signal from the SAR register: "swp" for the positive DAC and "swn" for the negative. Control signals initiate the switching of each particular bit in the matrix, and after receiving this signal, the required switch controller manipulates the 5-way CMOS switch relying on the 2 clock signals.

The switch controllers are designed to be separate independent building blocks in order to keep the SAR register's logic intact. Since the SAR control register contains the logic responsible for the switching scheme, the extra circuitry required for the adiabatic switching becomes independent from the specific switching scheme. That way the architecture becomes a more versatile add-on compatible with other switching schemes rather than being only applicable to a particular one. The intermediate voltages required for the adiabatic charging are taken from the switched-capacitor DC-DC step-down converter that also utilizes both clock signals to recharge.

The overall operation of the ADC is organized in the following sequence: in the idle state the sampling switches are open and the logic is reset. The DAC capacitors are connected to the reference voltage and ADC is tracking the input signal. When the SAR register and input sampling switches receive the start-of-conversion "soc" signal, that invokes the conversion procedure. The sampling switches open, the control register reset releases and the first comparison takes place. Then, depending on the result of the comparison, either swp[8] or swn[8] makes the according switch controller perform the 4-step discharging sequence within the timing set by the clk and clk_{90°. The same clock signals are also used to recharge the SC DC/DC converter. The delayed clock then comes to the comparator and the cycle continues for the evaluation of the rest of the bits. The evaluation of the LSB interrupts the clock feedback loop, sets the end-of-conversion "eoc" signal, and the resulting code appears at the outputs where it is stored until it is refreshed with the next conversion result.

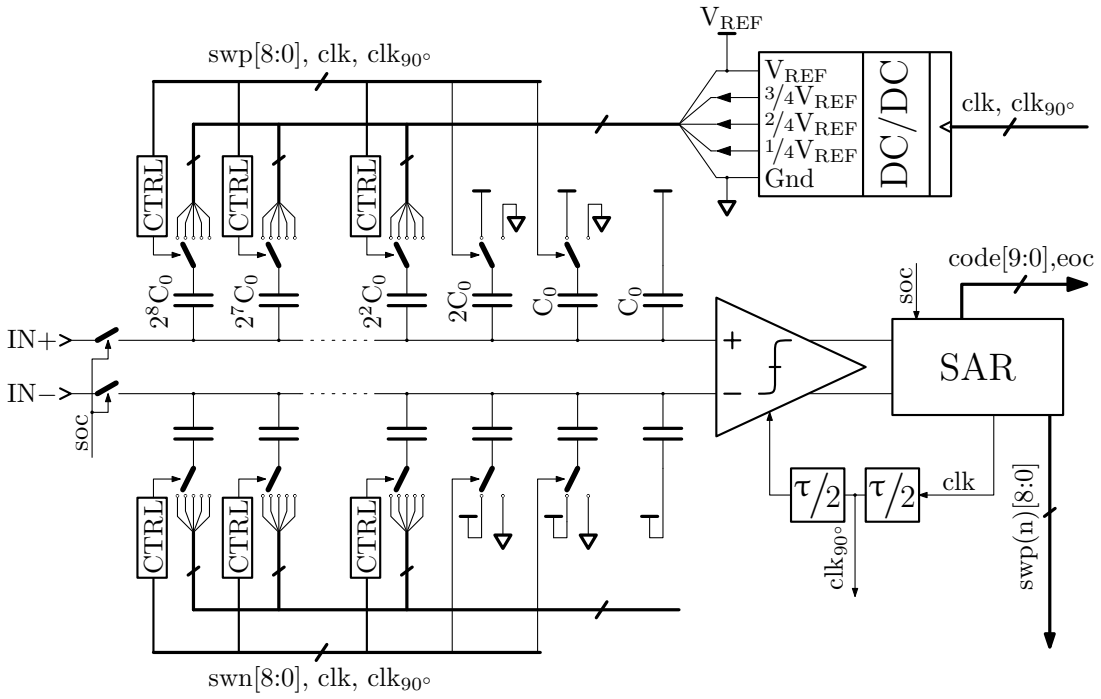


Figure 4.21.: Block diagram of the ADC

4.2.2. Input switch

Compared to the conventional SAR ADC switching scheme with bottom-plate sampling against Vcm, where the common mode voltage source can be switched off first, thus keeping the charge injection constant across the input voltage range, the monotonic switching scheme lacks that sampling procedure and instead samples the voltage onto the DAC top plates. In each DAC, sampling is done by disconnecting only one sampling switch between the matrix and the input voltage source. In these circumstances, a simple MOSFET switch would inject the amount of charge that is dependent on the input voltage, thus introducing non-linearities in the sampled voltage.

The bootstrapped sampling switch can provide suitable performance in regards to the charge injection for the ADC resolution of 8-12 bit. The benefits of this type of switch over the others were discussed in the Chapter 2.2.

The topology of the switch is shown in the Figure 4.22. The circuit is using a well-known design described in [Raz15a].

When the control signal S/H is high, it opens the PMOS switch P2, and closes the NMOS switches N3 and N2. When N2 closes, it connects the node X to the ground, which in turn closes the P1 PMOS switch. As a result, the capacitor C1 is being connected between VDD through P1 and GND through the N3. The pass-transistor N5 and switch N4 are open due to node X being tied to GND.

When the S/H signal is low, and capacitor C1 is charged, the switches N3 and N2

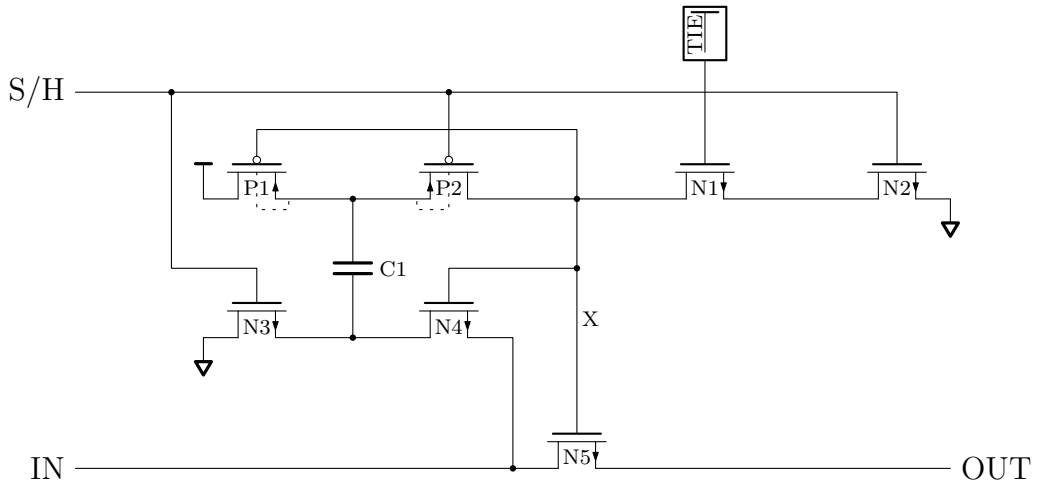


Figure 4.22.: Bootstrapped switch topology

are open and the P2 is closed, passing the high voltage from the capacitor to the node X, thus opening the P1 and closing the N4, which results in the capacitor being connected between the input and the gate of the pass-transistor N5. Since during the previous step C1 was charged to VDD, connecting it between input and node X provides the gate voltage of the N5 being higher than the input voltage by VDD.
The bootstrapped switch takes the full-swing range of input voltage and therefore the voltage at node X can reach 2 times the VDD. Transistor N1 protects N2 from high voltage damage improving longevity [Raz15a]. As it was done in [WZSR14], the substrate terminals of PMOS transistors P1 and P2 are connected to the top plate of C1 to avoid forward biasing of the p-n junction between substrate and source.

4.2.3. Comparator

The monotonic switching scheme utilizes the conversion using only the downward switching of either positive or the negative DAC and thus the common-mode voltage at the comparator's inputs varies during the conversion: at the MSB decision it reflects the input common-mode voltage equals $0.5V_{ref}$. Throughout the conversion, it decreases and approaches the LSB value during the LSB decision at the end of the conversion. As was discussed in Chapter 2.5, such operating conditions can introduce variation in the comparator's gain which then subsequently leads to the input-referred offset changing its value throughout the conversion, introducing non-linearities into the ADC transfer function.
To limit the influence of the common-mode voltage on the gain value, the biased comparator with the topology reported in [LCHL10] was used for the input stage.

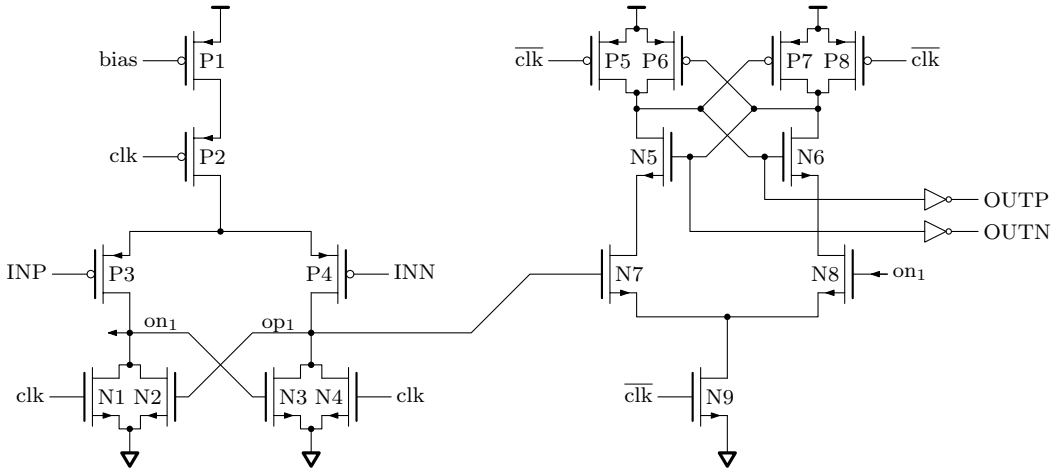


Figure 4.23.: Comparator topology

The output stage is represented by the StrongARM latch with inverters placed at its outputs to eliminate the offset that could be caused by the load capacitance mismatch. The resulting comparator circuit is shown in Figure 4.23.
The bias transistor P1 limits the tail current of the differential pair. When the clock signal is low, this current is allowed to pass through the switch P2. The reset switches N1 and N4 are open allowing the output signal to rise on the cross-coupled load represented by N2 and N3. During the amplification phase (Fig 4.24), when on1 and op1 both start to rise from Gnd to $V_{\text{th-N2,3}}$, the cross-coupled pair N2 and N3 is turned off. The time constant during that phase is defined by the bias current and the parasitic capacitances at the output nodes being charged. Therefore, fixing the bias current makes it independent from the input common-mode voltage if the output resistance of the current source P1 is not taken into account.
As the op1 and on1 approach the threshold voltage of N2 and N3, the cross-coupled latch turns on. The small-signal model of this phase is shown in Figure 4.25
The sum of the currents for each output node yields:

$$\Delta I - C_{on1}\frac{dV_{on1}}{dt} - g_{m2}V_{op1} = 0 \tag{4.11}$$

$$-\Delta I - C_{op1}\frac{dV_{op1}}{dt} - g_{m3}V_{on1} = 0 \tag{4.12}$$

Subtraction of (4.12) from (4.11) gives:

$$-\frac{C_{on(p)1}}{g_{m2,3}}\frac{d(V_{op1} - V_{on1})}{dt} + (V_{op1} - V_{on1}) = \frac{2\Delta I}{g_{m2,3}} \tag{4.13}$$

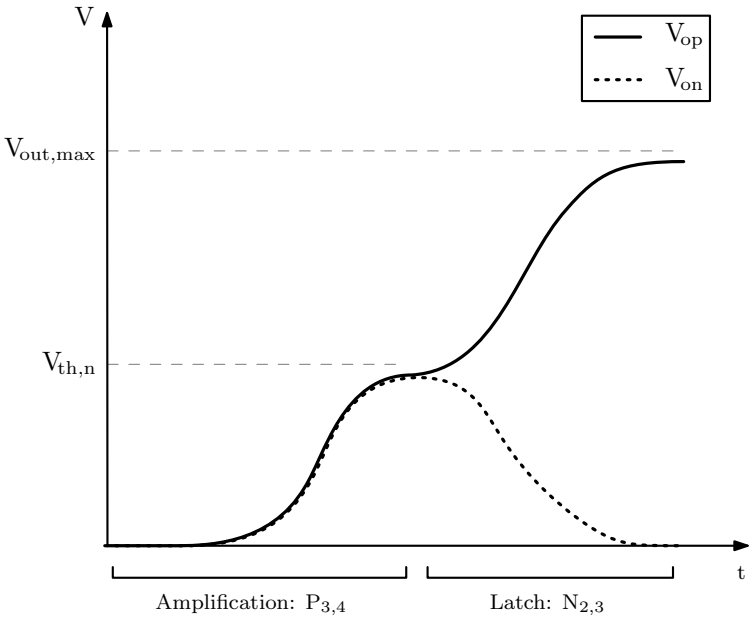


Figure 4.24.: Operation phases of the input stage

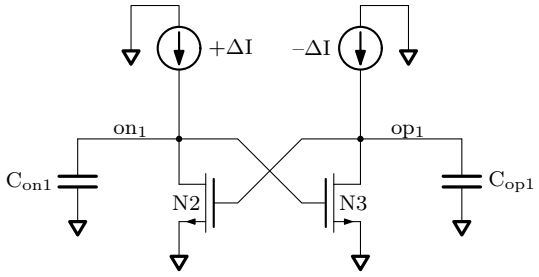


Figure 4.25.: Equivalent circuit of the 1-st stage cross-coupled load turned-on

The result is the first-order ODE model of the system with positive feedback and RHP pole. The output differential voltage grows exponentially and therefore the time constant τ is negative:

$$\tau = -\frac{C_{on(p)1}}{g_{m2,3}} \tag{4.14}$$

The bias current set by P1 keeps $g_{m2,3}$ of the cross-coupled load the same across the range of input common-mode voltage values, thus keeping the time constant (4.14) independent from the input common-mode voltage as well.
As the differential output voltage at the first stage grows, in the large-signal domain one of the two cross-coupled transistors N2 or N3 closes the channel due to its gate voltage connected to the output of the opposite branch reaching Gnd. That makes all bias current flow through the opposite branch with the open load whereas the branch with the load closed reaches its maximum output voltage. This voltage marked as $V_{out,max}$ in Figure 4.24 cannot reach VDD and also varies

with $V_{cm,in}$.

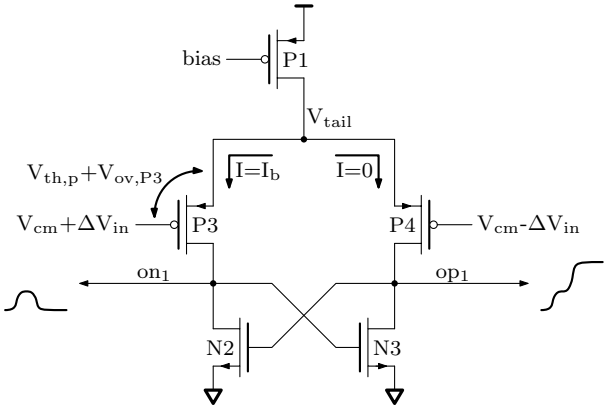


Figure 4.26.: Input stage's output voltage swing limitation

The mechanism describing this behaviour is depicted in Figure 4.26 with closed switches P2, N1, and N2 omitted for simplicity. Transistor N3 has the gate-source voltage $V_{gs,N3}$=0, and its channel is closed. With no current through the right branch, the output voltage V_{op1} approaches V_{tail}. This voltage is defined by the gate-source voltage of P3. Assuming it is in saturation and strong inversion, for the bias current to flow through P3 it has to have $V_{gs,P3}$=$V_{th,p}$+$V_{ov,P3}$. Therefore, V_{tail} is larger than the gate voltage of P3 by that amount. For the small values of $V_{cm,in}$ and small input differential voltages, the tail voltage can be lower than 0.5VDD, making this stage unreliable without a level shifter restoring the output voltage to the level appropriate for the digital circuitry. The StrongARM latch is therefore acting as a level shifter.

The cross-coupled latch in the input stage turns on when both outputs reach $V_{th\text{-}N}$. After that, the differential output voltage starts to grow. The output common-mode voltage $V_{cm,out1}$ is constant and close to $V_{th\text{-}N}$ until one output reaches Gnd and the other continues to grow to V_{tail}. Therefore, $V_{th\text{-}N}$ can be considered as the operating point at the inputs of the second stage defining the parameters in the small-signal domain. This value does not depend on the common mode voltage at the DAC outputs. The differential voltage span during the phase when the $V_{cm,out1}$ is constant is sufficient for the output stage to turn on, therefore further growth of one of the outputs causing the shift in $V_{cm,out1}$ has only limited impact on the second stage dependence on the $V_{cm,in}$. The overall comparator dependence on the input common-mode voltage is mainly defined by the finite output resistance of the current source P1 and its capability to maintain constant bias current when V_{tail} varies with $V_{cm,in}$.

4.2.4. Successive approximation register

The successive approximation register operates the clock loop and contains the necessary digital circuitry to provide DAC with control signals to follow the monotonic switching scheme. The circuit also has the output parallel shift register for the conversion result. Since the architecture of a prototype was decided to have separate parts responsible for the switching scheme and adiabatic charging to maintain versatility, the structure of the SAR control logic resembles the one originally reported in the [LCHL10]. The schematic of the resulting control logic is shown in Figure 4.27.

The start-of-conversion signal (SOC) acts as a reset signal. During the reset phase with SOC at logic low (0), the clock signal is held at logic high (1) and both comparator's outputs are held at 0. Upon the start of conversion on the negative edge of SOC, the clock switches to 0 and reaches the comparator through the delay, initiating the first comparison. The XOR gate is used to differentiate whether the outputs of the comparator are valid. Upon receiving the valid signal, the serial shift register made using D flip-flops uses the valid signal as a clock to feed the 1 from the tied input of the first flip-flop further down the chain. The last clock cycle, when the 1 reaches the output of the last flip-flop, enables the stop signal connected to the 3OR gate, disabling the clock loop until reset.

During the conversion, the series register described above generates signals labeled as sw-clk[0:8] at its parallel outputs. These signals are used as clock signals for the two arrays of D flip-flops taking the comparator's decision at a given conversion step and using this decision to switch the according DAC capacitor. These control signals are labeled as swp[8:0] and swn[8:0] for the positive and negative DAC switches accordingly.

Since the swp(n) signals are taken from the comparator outputs, they resemble the bit decisions and are used as the output code. For the code at the output of the ADC to always stay valid and refresh only upon the end of conversion, the EOC signal is used to clock the parallel-in, parallel-out register that keeps the results of the previous conversion until the end of the current one. The LSB decision is taken directly from the comparator output and does not require further switching of the DAC. Hence, the LSB decision does not require an according swp flip-flop and is directly forwarded to the output code parallel register.

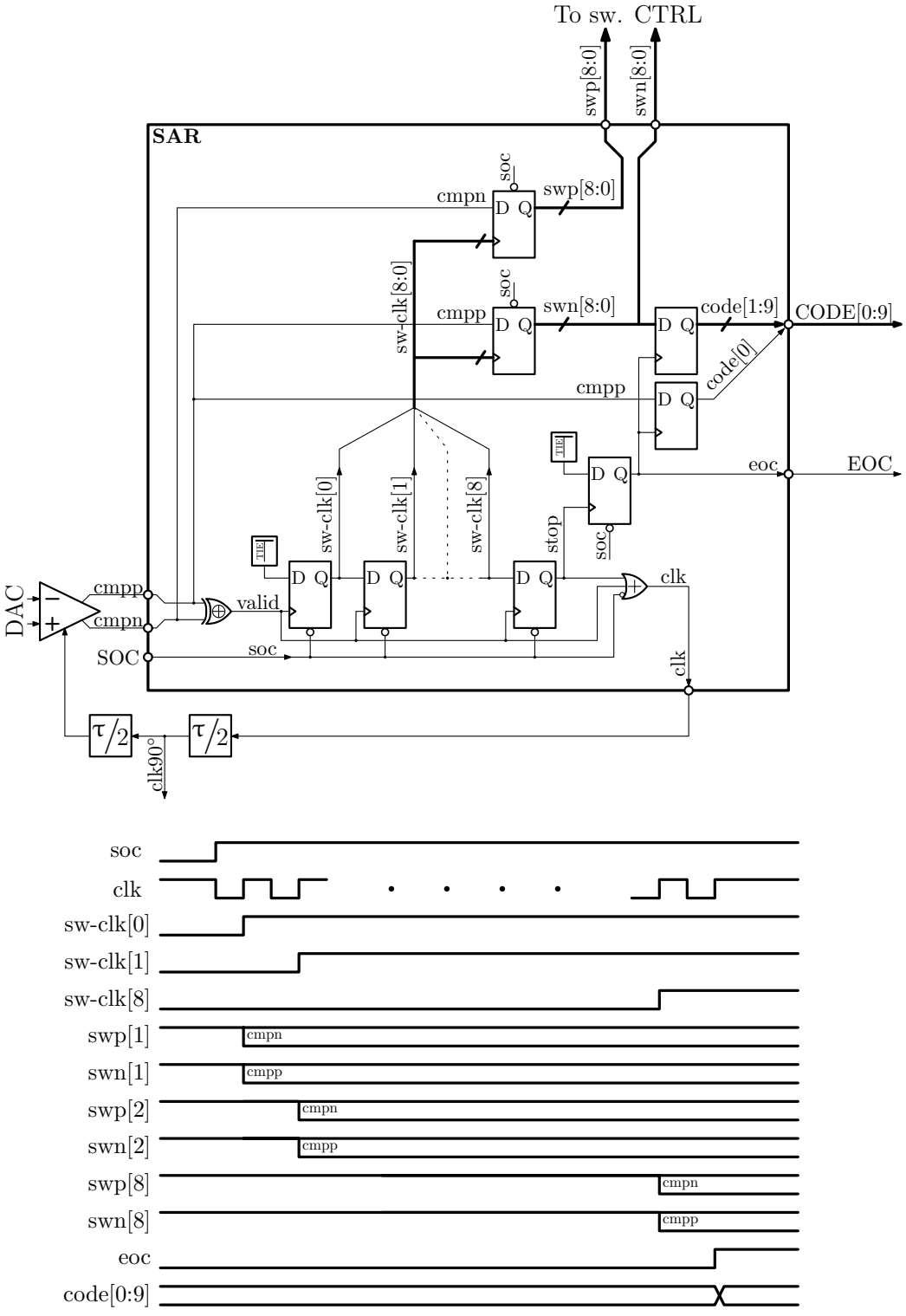


Figure 4.27.: Successive Approximation Register logic

4.2.5. Delay chain: 90˚phase shift

The delay element in the clock feedback loop sets the conversion speed and ensures proper settling of the DAC output voltage. To generate 4 distinct steps during 1 conversion step, the extra output signal was taken from the middle of the delay chain. Conceptually, that provides an additional clock signal shifted to approximately 90 degrees. Combined, clk and clk_{90° provide four distinct states during every conversion step: 00,01,11,01.
The delay chain (Fig. 4.28) is combined from self-supply modulation delay elements [OLP20]. Next inverter's supply voltage is connected to the output of the previous inverter. The number of stages connected in series using this principle was chosen to be 4. The four chains of four inverters create one $\tau/2$ delay element.
The implemented design uses the clock shifted by 270 degrees rather than 90. It is done by taking the output clock signal 1 inverter away from the middle of the delay chain, effectively providing the inversion of the 90-degree phase-shifted clock and introducing an extra 180-degree phase shift.

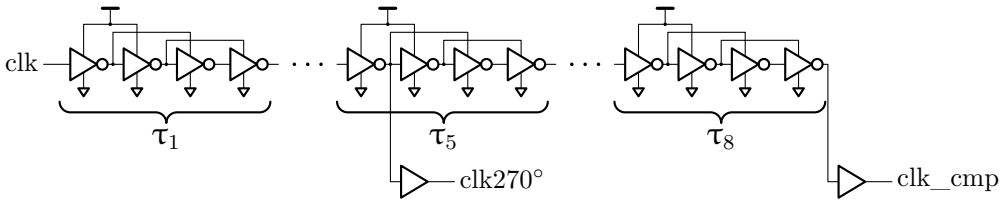


Figure 4.28.: 270-degree phase clock generation

Comparator latency being a part of the clock loop fluctuates the phase shift. In some designs that may affect the settling before the comparison. The inconsistency of charging steps before the last one only impairs energy efficiency, whereas the last charging step is important for maintaining the accuracy of the conversion. Therefore, in designs where the comparator contribution to the overall delay is large, the phase shift adjustment can be done by taking the extra clock signal earlier in the delay chain to preserve the time for the last step. In the implemented design comparator's contribution to the overall delay was not significant and the phase shift adjustment was not necessary.

4.2.6. Additional switch controllers

To generate separate switching signals for 5-way CMOS switches, switch controllers were designed. The conceptual circuit diagram of the controller is shown in Fig. 4.29. In the figure, the output signals are brought up to the same polarity for clarity of demonstration. The circuit utilizes 4 states provided by clk and clk_{270° to generate 4 charging steps for each DAC capacitor. Swp(n)[i] initiates the sequence

and disconnects the capacitor from the Vref node. Hence, this signal is directly transferred to the output as $sw[i]_0$.

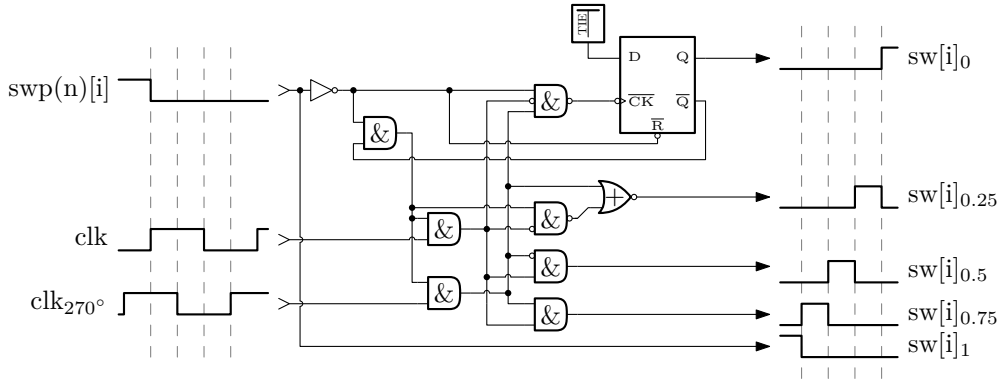


Figure 4.29.: Switch controller

Since clk and $clk_{270°}$ are running continuously and each controller has to only engage once during the conversion, it requires gating the rest of the controller's outputs from the clock signals. The first column of the AND gates creates a stage that together with the flip-flop acts as a gate system that enables the switch controller on the negative edge of swp(n)[i] and then disables the controller while holding its outputs after the last charging step signal $sw[i]_0$ has been switched. The second stage of inverters extracts the necessary signals from the clk and $clk_{270°}$ using AND gates with direct and inverted inputs and a NOR gate.
At the last phase, when clk is 0 and $clk_{270°}$ is 1, the 3NAND gate generates the clock for the D flip-flop which switches its positive output to 1. The inverting flip-flop output then switches AND gate to 0, thus disabling the two other AND gates making the controller insensitive to the clock signals.
In the implemented switch controller, the resulting 5 output control signals are brought to the appropriate polarity to operate the 5-way CMOS switches connecting the DAC capacitors to the according voltages. The switches use NMOS transistors for the connection to Gnd and $^1/_4V_{REF}$ while the rest of the switches are PMOS. Therefore, to maintain the appropriate polarity for the PMOS switches, in the implemented circuit the signal $sw[i]_1$ was taken from the output of the inverter ranter than being transferred directly to the output, and to generate the signals $sw[i]_{0.75}$ and $sw[i]_{0.5}$ the according gates with the inverting outputs were used.

4.2.7. DC-DC converter

The DC-DC converter is implemented using a 2-stage step-down switched capacitor topology. The first stage divides the supply voltage by two through serial-parallel commutation of the capacitors C1 and C2 using switches P2 and N2-N4.

The output voltage of the first stage is being further converted by the second stage through a downward conversion on capacitors C5-C6 and switches N6-N9, and upward conversion on capacitors C3-C4 and switches P3-P5 and N5.

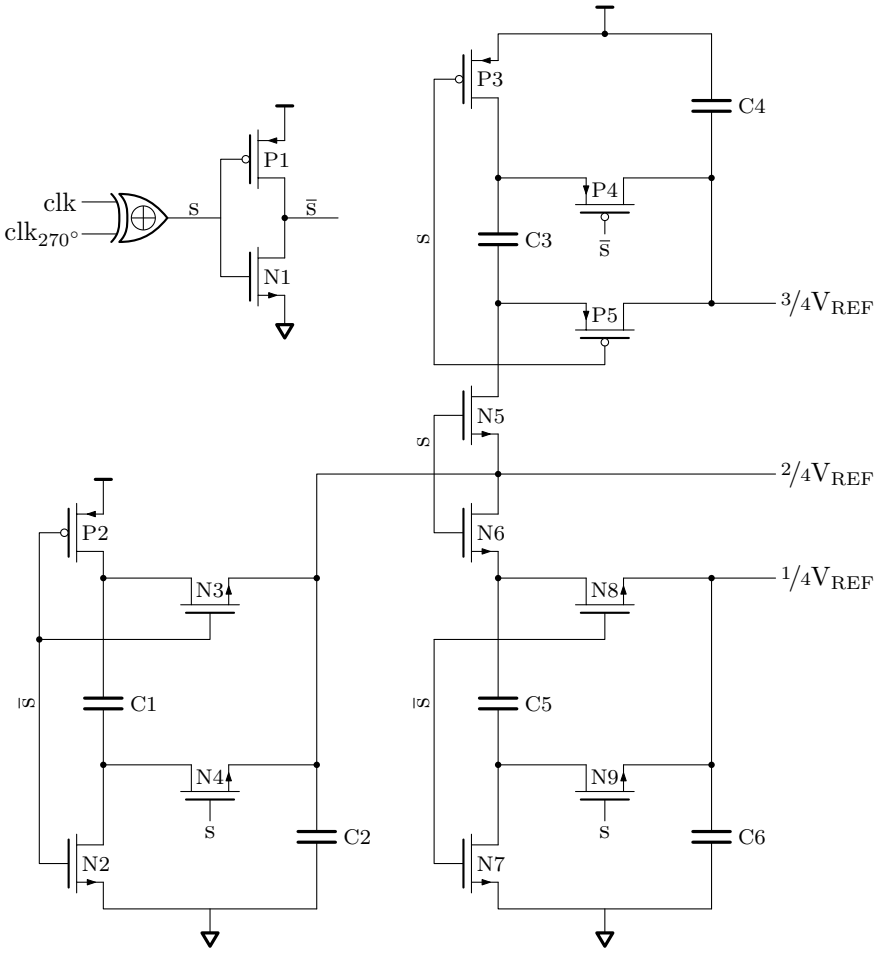


Figure 4.30.: 2-stage step-down SC voltage converter topology

All six capacitors are of equal size. The total capacitance of the converter in regards to the DAC unit capacitor was targeted to be approximately $2048C_0$, which for the 51fF unit capacitor resulted in a value of 17.5pF for each capacitor in the DC-DC converter.

To restore the charge, the circuit multiplies the clock frequency using XOR gate, then the resulting signal marked as "s" is inverted to generate the charging signal of the opposite polarity for the PMOS switches. Overall this results in the converter restoring the charge twice during the DAC stepwise discharging sequence at every bit decision. Due to the two LSBs not using the stepwise charging and therefore not withdrawing the charge from the converter, the clock cycles during these steps provide redundancy to ensure a complete charge restoration of the DC-DC converter while the last two bits undergo the conversion.

4.2.8. DAC Layout: diagonal weighted common centroid, shielding

The placement of the DAC capacitors for one of the DACs is shown in Figure 4.31. The common centroid placement reduces the systematic mismatch caused by the first-order process gradient. The placement method used for the implementation was introduced by [LZCL14]. It is optimized for the binary-weighted DAC matrices and uses the diagonal-weighted common centroid approach and homogenization to minimize oxide gradient-induced mismatch. Dummy capacitors shown in grey are placed to reduce the proximity effects.

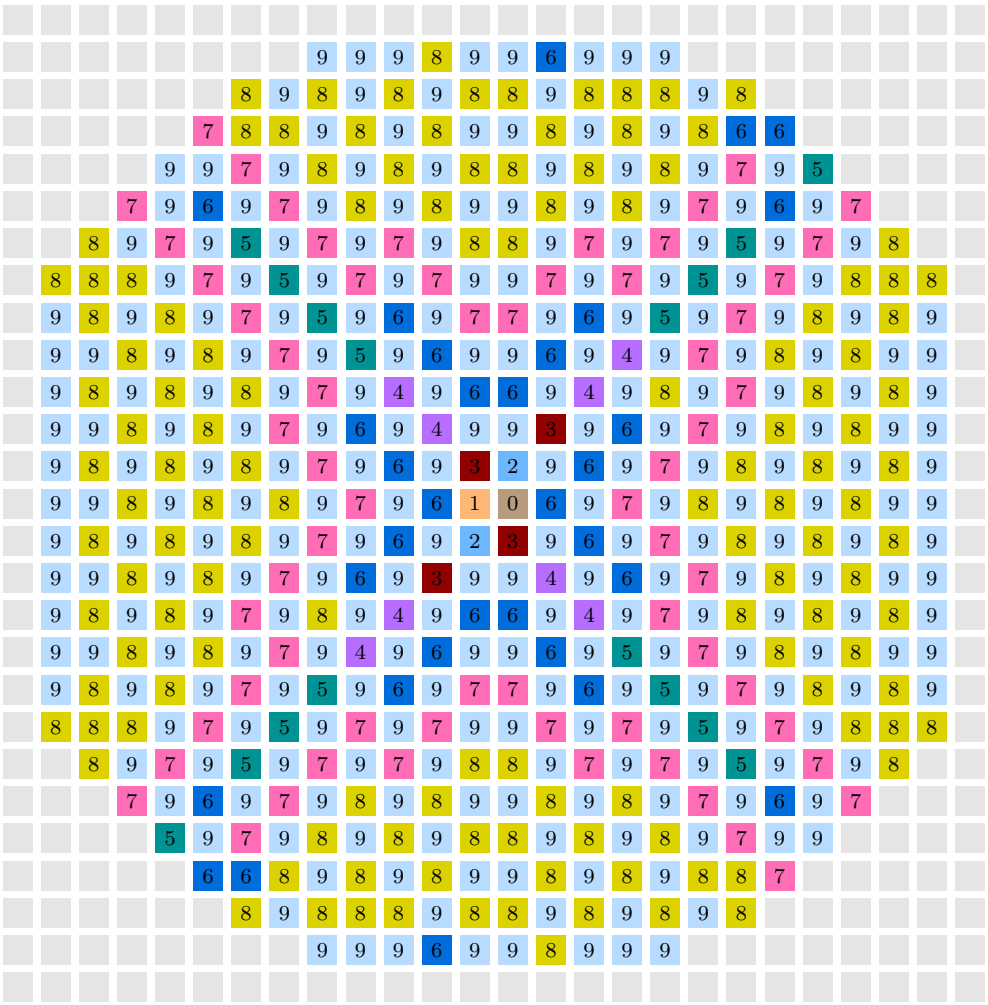


Figure 4.31.: DAC placement. Recreated image from [LZCL14]

For the routing of the signal wires it is important that the parasitic capacitances do not influence the binary-weighted ratios in the DAC matrix. This is achieved by the shielding technique used for routing. The concept of shielding is shown in Figure 4.32. A layer of metal connected to the reference voltage or ground placed in between the routing wires splits the coupling parasitic capacitance between top

and bottom plate of the unit capacitor, thus preserving the capacitance value.

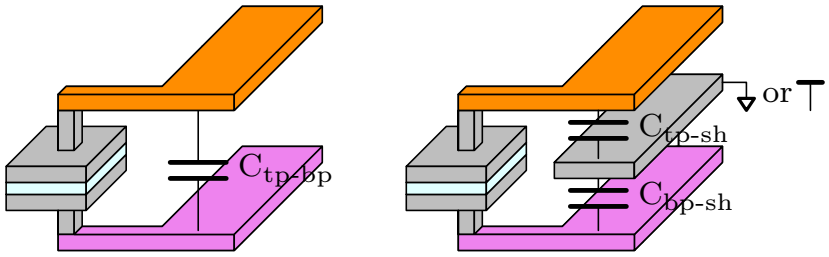


Figure 4.32.: Shielding of the DAC capacitors routing

In the DAC matrix, the top plates of all the unit capacitors are wired together and routed above the shield. The routing from the bottom plates of the unit capacitors to the DAC switches is placed below the shield. This keeps the binary-weighted ratios unaffected by the routing. The downside of this method compared to no-shielding is that the extra coupling capacitance from the top plates routing to the shield introduces a larger DAC gain error, which results in a reduction of the ADC full-scale voltage.

4.2.9. Chip design

The layout of the produced prototype is shown in Figure 4.33. The prototype is designed using UMC 65nm process with MIM process option. The chip contains 4 ADCs with multiplexed outputs. The ADC described in the chapter 4.2 is placed in the top-left corner and labeled ADC_A. The other ADCs named counterclockwise as ADC_B, ADC_C, and ADC_D. The ADCs B and C are test structures not relevant to this research. The ADC_D is a modified version of ADC_A. The difference between ADC_A and ADC_D will be described further in this chapter. The chip features separate supply domains for each ADC. On the chip top-level, the top two ADCs have their own digital supply called VDD_A and VDD_D, with digital ground VSS which is a common digital ground for the overall chip. Similarly, the analog supply VDDANAC_A and VDDANAC_D are the separate analog supply voltages of the two top ADCs, whereas VSSANAC is a common analog ground of the whole chip. ADCs at the bottom have their analog and digital supply combined and connected to pins VDDANAC_B and VDDANAC_C.
The pad ring is powered with low-voltage 1.2V digital supply VDD(also used for the output multiplexer), and I/O 2.5V digital supply VDDIO.
Overall, the chip has 3 ground nodes: VSSANAC, VSS, and VSSIO. The triple-well layout has not been used, therefore grounds are electrically connected through the P-substrate, which introduces a resistive path between the ground wires making them not completely separated. However, since only one ADC is supposed to

be measured at any given time, and the PCB is not supposed to have extended digital circuitry onboard, the ground wires separation was considered sufficient despite the resistive coupling.

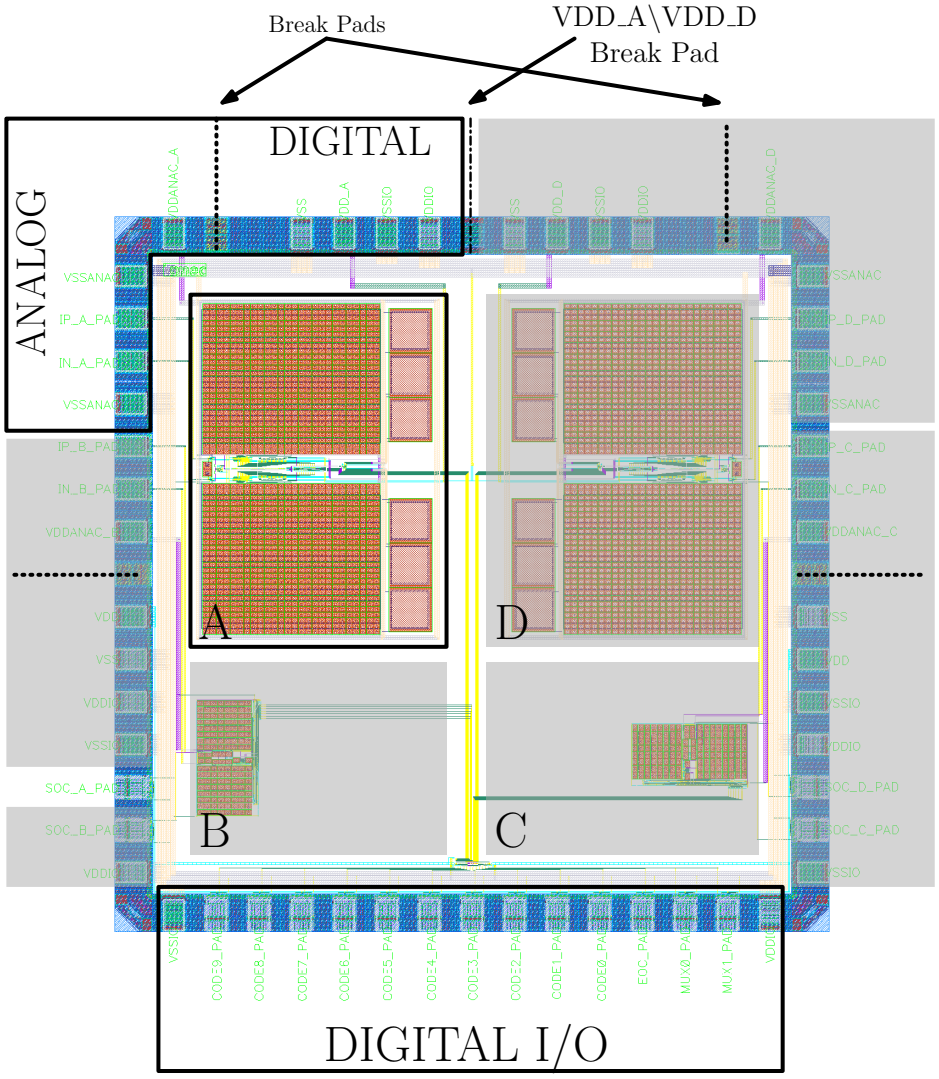


Figure 4.33.: Produced IC layout

Overall, the pad ring features two analog domains in the top-left and top-right corners, in the top-middle it has two digital domains with separated digital supplies VDD_A and VDD_D. The digital domain on the bottom has digital I/O pads for the four SOC signals, multiplexed EOC and output bus, and the MUX control inputs. The description of the pins is given in the Table 4.2.

As mentioned above, the produced chip contains 4 ADCs, two of which (B and C) are not relevant to this research. The ADC_A was described in the chapter 4.2. The ADC_D is a modified version of the ADC_A and differs from it in terms of speed and unit-capacitor size.

The ADC_A has a 51fF unit capacitor which is a minimum size allowed by the

Pin	Description
VDDANAC_A(D)	Analog supply of the ADC_A(D)
VDD_A(D)	Digital supply of the ADC_A(D)
VDDANAC_B	Combined supply of the ADC_B
VDDANAC_C	Combined supply of the ADC_C
VDD	General purpose digital supply for pads and mux
VSSANAC	Common analog ground
VSS	Common digital ground
VDDIO	2.5V I\O supply
VSSIO	I\O ground
SOC_A(B,C,D)	Start of conversion inputs for ADC_A(B,C,D)
MUX[1:0]	Multiplexer input selection bits
CODE[9:0]	Output code of the selected ADC
EOC	End of conversion signal of the selected ADC

Table 4.2.: IC pin description.

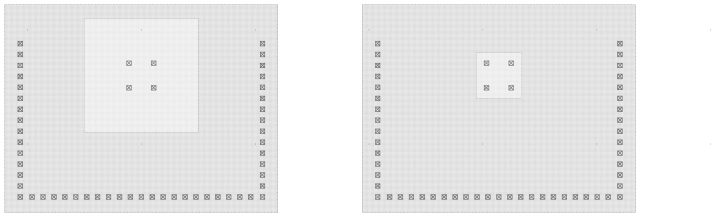


Figure 4.34.: Original (left) and modified DRC limited (right) Pcell layouts

provided library pcell. The pcell was modified to reduce the value further down to 8.5fF while still keeping it free of DRC errors. The original pcell used in ADC_A is shown in Figure 4.34(left). The modified capacitor layout with the size limited by DRC is used in ADC_D and is shown in Figure 4.34(right). To keep routing between the two DACs close, the reduced capacitor has the same via placement. That allows for a simple replacement of the capacitor's layout view in the original DAC to produce a second version.

Another difference between the ADC_D compared to ADC_A is the higher conversion speed. The delay chain of the ADC_A (described in Chapter 4.2.5) was modified to increase the clock frequency. Instead of using 8 self-supply modulated delay elements, the delay chain of the ADC_D was shortened resulting in 4 delay elements in total. The length of the transistors in the modified delay was also reduced. The phase-shifted clock signal was taken from the middle of the modified delay chain in the same manner. The resulting clock feedback loop provides a conversion speed of 1MS/s compared to 165kS/s for the ADC_A.

The photo of an unpackaged sample of the produced chip is shown in Figure 4.35. Both ADCs occupy an equal area due to the reduction of the unit capacitor size by shrinking only one of two plates. Although the total capacitance of the DC/DC converter in ADC_A is $2048C_0$ and the sum of capacitances of positive and negative DACs is $1024C_0$, the area occupied by the DC/DC converter is 2x101x313um and for 2xCDAC it is 2x416x354um. Therefore, the DC/DC converter occupied area is approximately 4.7 times smaller than that of the DAC.

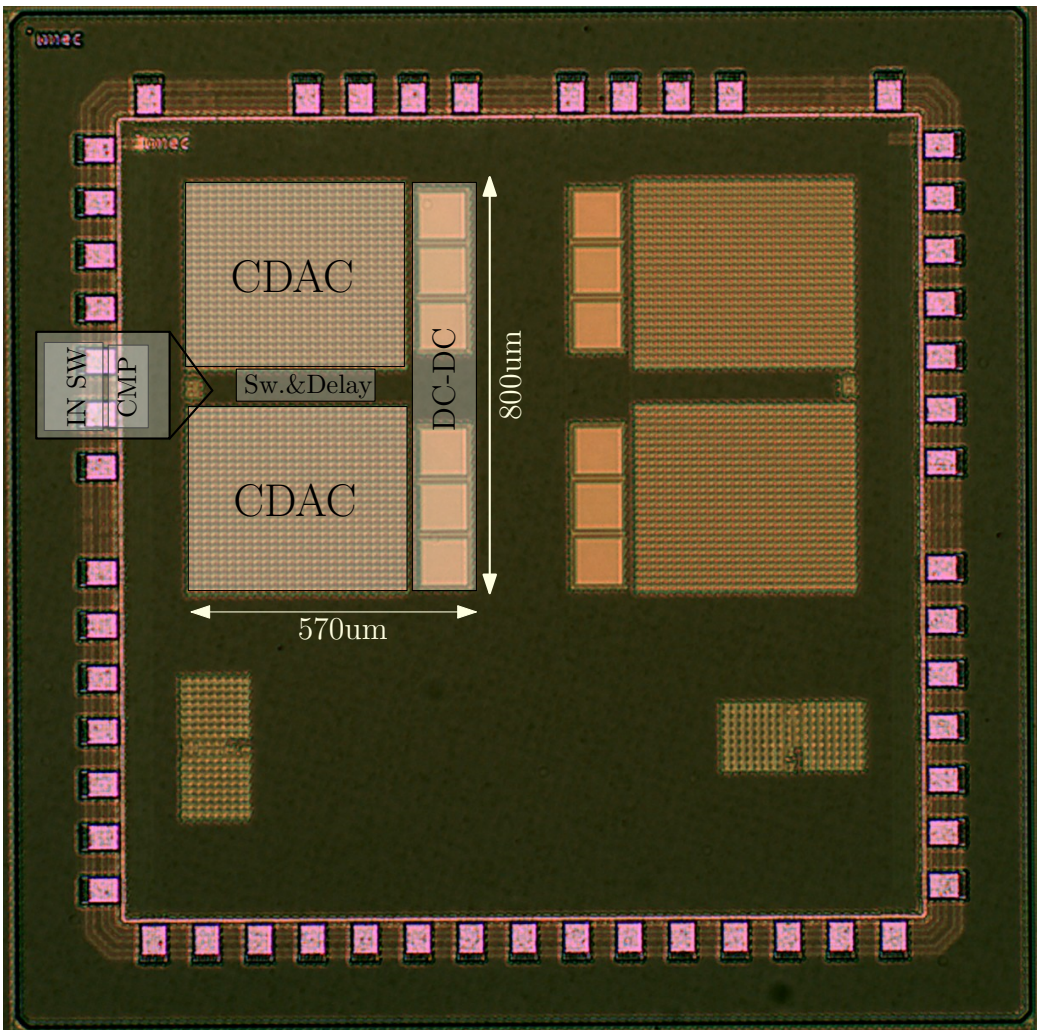


Figure 4.35.: Die photo of a non-packaged produced IC

5 Measurements

5.1. PCB Design

The PCB used for the ADC evaluation is shown in Figure 5.1. The board features a selectable supply for each ADC that can either be taken from the onboard 1.2V LDO or an external DC voltage source, connected to one of the terminals A, B, C, or D. The switching between external and onboard supply is implemented using 3 pins for each ADC. Each central pin is connected to the ADC supply, the right-side pin is connected to the onboard 1.2V supply, and the left-side pin is routed to the SMA connector dedicated to the external voltage source. Selection is therefore done with a jumper. For ADCs A and D which feature separate digital and analog supplies, the nodes were connected so the overall ADC power consumption can be measured from one channel of the external DC voltage supply.

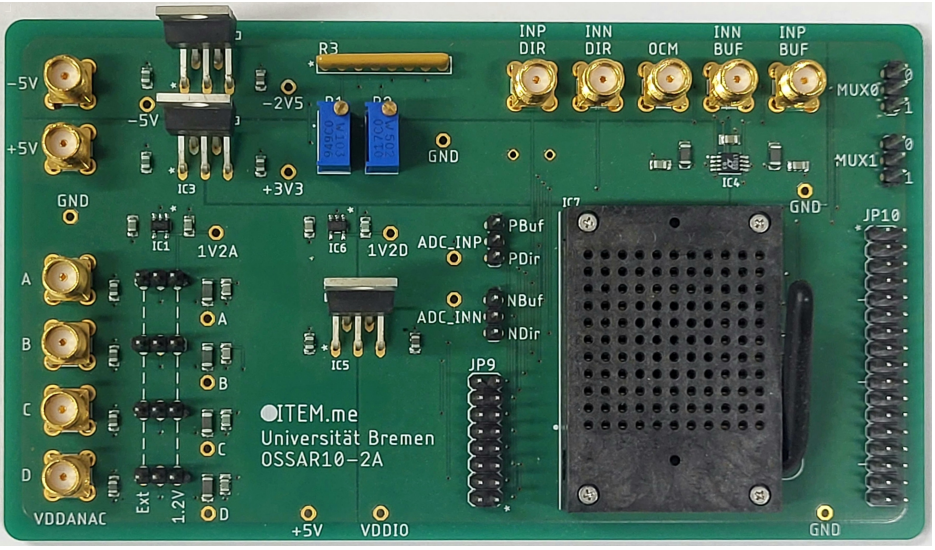


Figure 5.1.: PCB used for the measurements

The input signal conditioning is done using the LTC6363-1 differential amplifier. If the OCM input is not driven, the amplifier's output common mode voltage

is in the middle of the supply voltage span of the amplifier. To adjust it to the required 0.6V the amplifier is connected to the +3.3V positive supply and -2.5V negative supply, which can be further adjusted using coarse and fine trim resistors R1 and R2 to achieve 0.6V. Alternatively, the OCM SMA-input can be used to directly set the output common mode to a desired value.
Similarly to the ADC supply voltage selection, the ADC input signals can also be taken directly from the voltage source skipping the onboard driver using jumpers on the P(N)Buf-P(N)Dir group of pins. The selected configuration then provides the input voltage transfer to the nodes ADC_INP(N).
To transfer this voltage further to the differential inputs of 1 of the 4 ADCs, the group of connectors JP9 is routed in a way that interchanging ADC_INP and ADC_INN are routed to the left column from top to bottom, and differential inputs of the 4 ADCs routed to the right column. Therefore, to connect the input voltage to the desired ADC inputs, it requires 2 jumpers connecting the left- and right sides of the JP9, thus connecting the ADC_INP(N) to the according inputs of the desired ADC.
On the right-hand side of the PCB the pins MUX0 and MUX1 are used to control the on-chip output multiplexer selecting the outputs of one of the four ADCs to be transferred to the output of the chip. The group of pins JP10 is routed to the output code bus, end-of-conversion signal as well as four start-of-conversion signals.
For the measurements, the PCB was set up as follows: +/-5V supply voltage was taken from the Agilent E3647A Dual Output DC power supply, the ADC supply was taken from the Keysight B2962A power source, the clock signal and single-ended input voltage was taken from the Rigol DG4062 function generator. The input voltage from the generator was connected to the INP-BUF input of the PCB while the INN-BUF input was connected to the ground node. The single-ended to differential conversion was done onboard by the differential amplifier. The digital readout was done using the Tektronix TLA 5202B logic analyzer. The recorded data was then processed in MATLAB.

5.2. Measurement results and Discussion

5.2.1. Dynamic characteristics

To measure the dynamic characteristics of the ADCs, sine waves with a near full-scale peak-to-peak amplitude and various frequencies were applied to the inputs. A 32768 points FFT spectra were then plotted and evaluated in MATLAB to find SNDR, SFDR, SNR, and THD. SNDR was then used to calculate the resulting ENOB.
The dynamic performance was measured in three regions using 3 frequencies for each ADC: high frequency, mid-bandwidth, and low frequency. To avoid spectrum leakage, the input frequencies for each range were calculated using a ratio with a prime number as:

$$F_{in} = \frac{N_{prime}}{No.\ of\ samples} \cdot F_s \tag{5.1}$$

For each region, this resulted in:

$$F_{in,H} = \frac{14593}{32768} \cdot F_s \tag{5.2}$$

$$F_{in,M} = \frac{7603}{32768} \cdot F_s \tag{5.3}$$

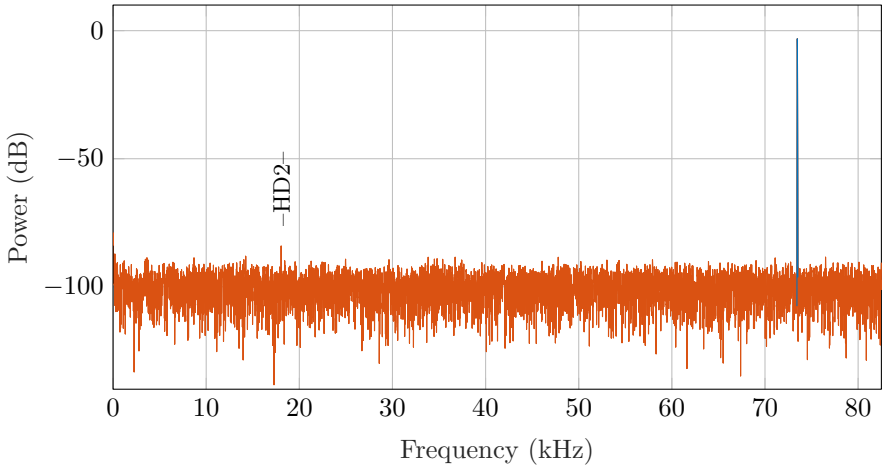
$$F_{in,L} = \frac{311}{32768} \cdot F_s \tag{5.4}$$

This gives 3 tones for the ADC-A with 165 kS/s sampling rate and 3 tones for the ADC-D with a sampling rate of 1MS/s. Both ADCs use the SOC signal with a 90% duty-cycle. The 32768 points FFT spectra for ADC-A and ADC-D are shown in Figures 5.2 and 5.3. The results are summarized in Table 5.1.

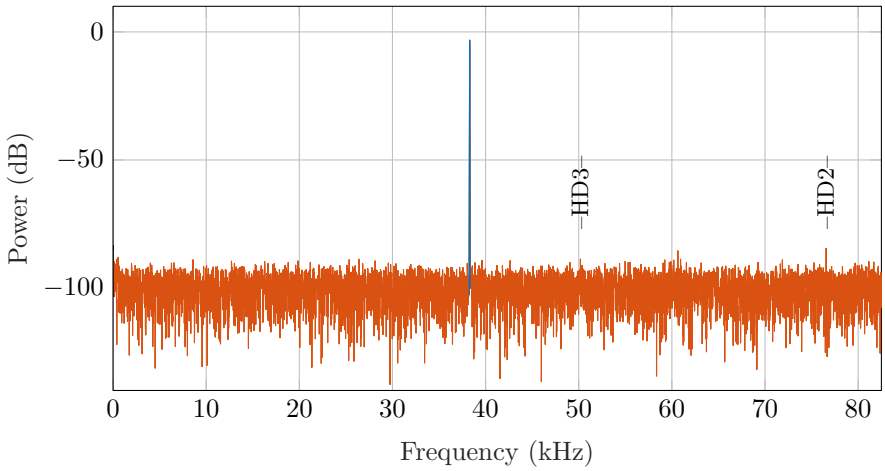
	ADC-A, 165 kS/s			**ADC-D, 1 MS/s**		
	H	M	L	H	M	L
F_{in} (kHz)	73.47	38.28	1.57	445.34	232.03	9.49
SNDR (dB)	57.63	57.73	57.77	56.52	56.80	56.77
SFDR (dB)	75.83	80.66	81.72	72.55	77.62	82.99
SNR (dB)	57.66	57.75	57.8	56.73	56.85	56.78
THD (dB)	79.1	80.67	78.4	69.43	75.32	81.61
ENOB (Bit)	9.28	9.3	9.3	9.1	9.14	9.14

Table 5.1.: Dynamic performance

$SNDR_{dB}$ 57.63, $SFDR_{dB}$ 75.83, SNR_{dB} 57.66, THD_{dB} 79.1, ENOB: 9.28



$SNDR_{dB}$ 57.73; $SFDR_{dB}$ 80.66, SNR_{dB} 57.75, THD_{dB} 80.67, ENOB 9.3



$SNDR_{dB}$: 57.77, $SFDR_{dB}$ 81.72, SNR_{dB} 57.8, THD_{dB} 78.4, ENOB 9.3

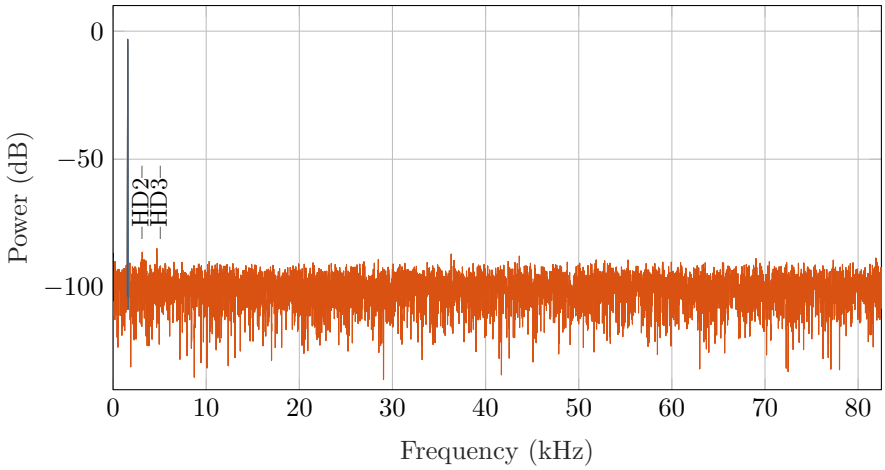
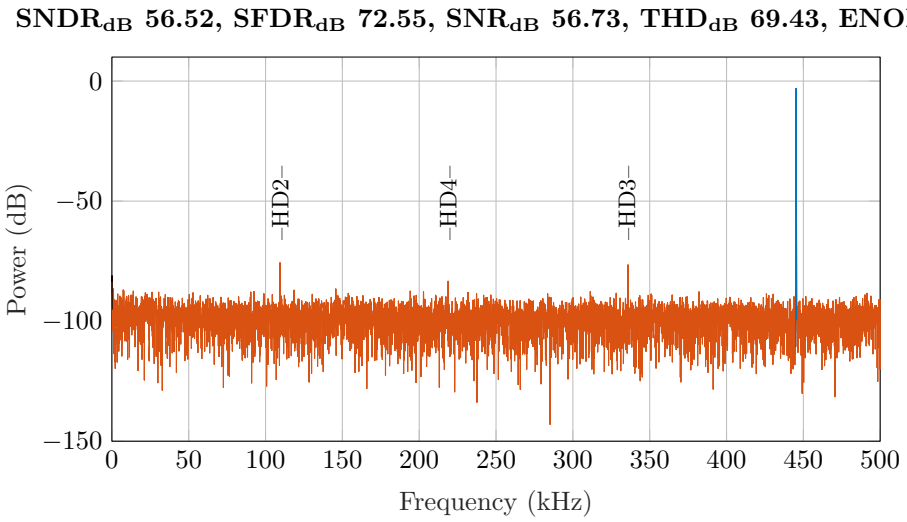
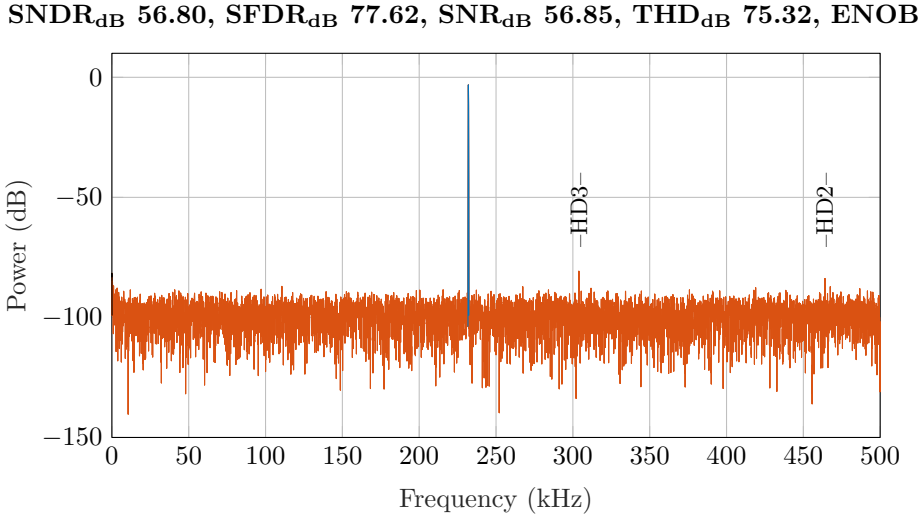


Figure 5.2.: ADC-A output 32768 points FFT spectra for 3 input frequencies





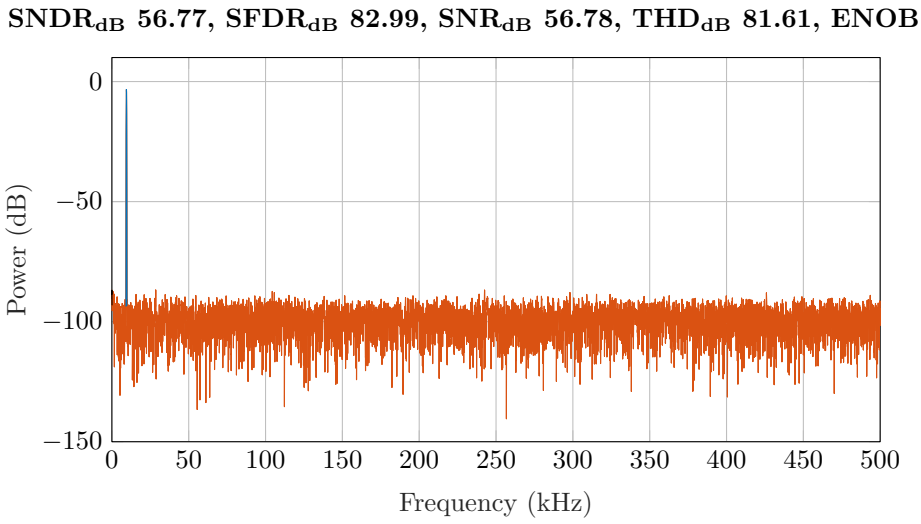


Figure 5.3.: ADC-D output 32768 points FFT spectra for 3 input frequencies

5.2.2. Static characteristics

The linearity tests have been performed using the histogram method. Sine wave input signals with frequencies of 1.57 kHz for the ADC-A and 9.49 kHz for the ADC-D were applied to ADCs inputs. The magnitude of the input signal is required to be sufficient to clip the ADC at the ends of the code range. The resulting data was then collected and the output code histogram was evaluated and compared against the ideal sine wave probability density function. The method and the MATLAB script used are described in [MI].
The required data record size to test a 10-bit ADC with a DNL error resolution of 0.1 LSB and a confidence level of 99% is 1070678 [MI]. For a 95% confidence level, the required record size is 617920. The Tektronix TLA 5202B logic analyzer has a maximum data record size of 1048576. Thus, the confidence level of the measured results approaches but does not reach 99%.
The resulting DNL/INL plots and histograms for ADC-A and ADC-D are presented in Figures 5.4 and 5.5. The measurement results are summarized in the Table 5.2.

	ADC-A, 165 kS/s	**ADC-D, 1 MS/s**
DNL (LSB)	+0.87/-0.79	+1.07/-0.90
INL (LSB)	+0.94/-0.28	+1.19/-0.77

Table 5.2.: Linearity performance

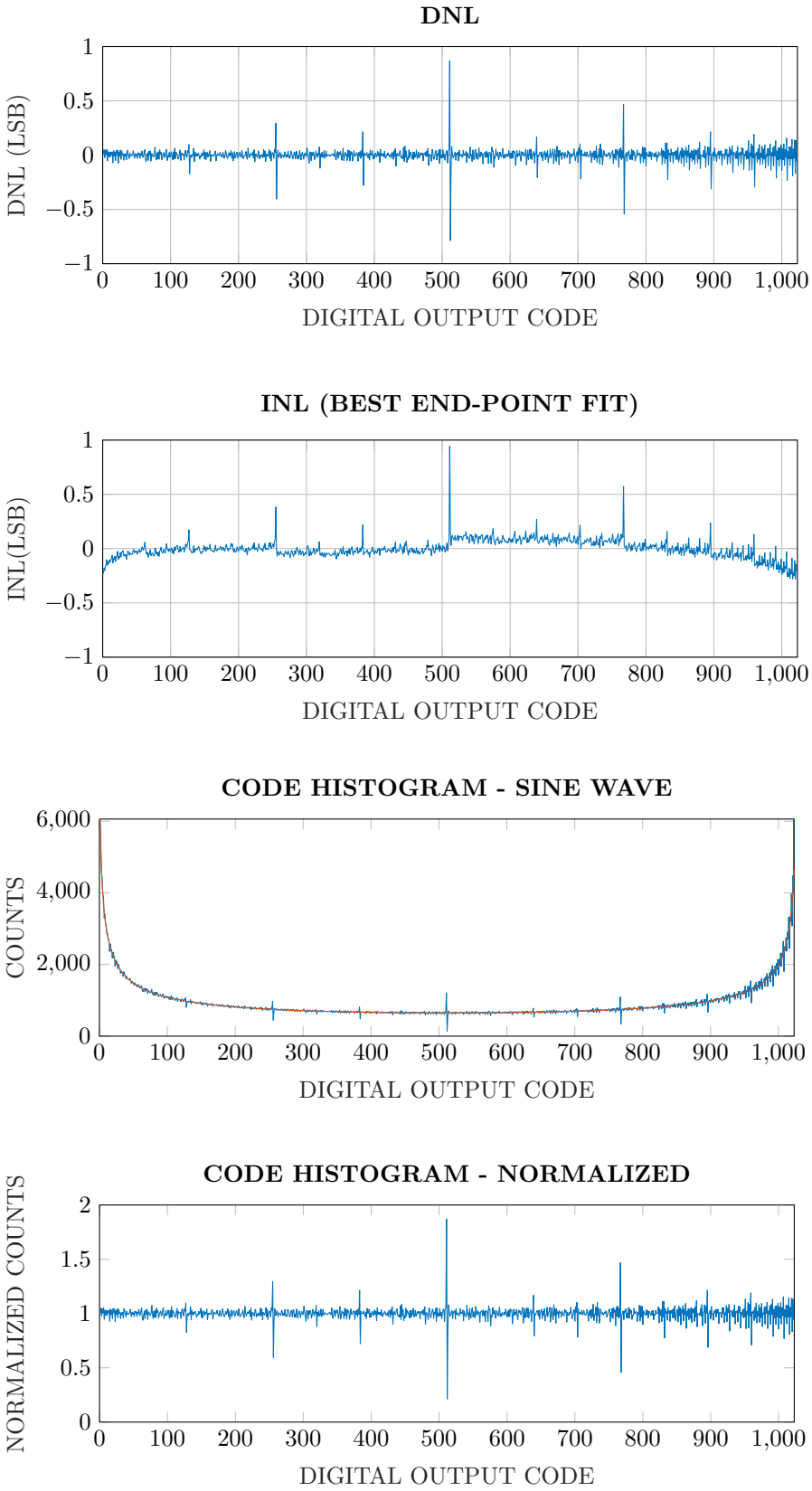


Figure 5.4.: Measured ADC-A static performance

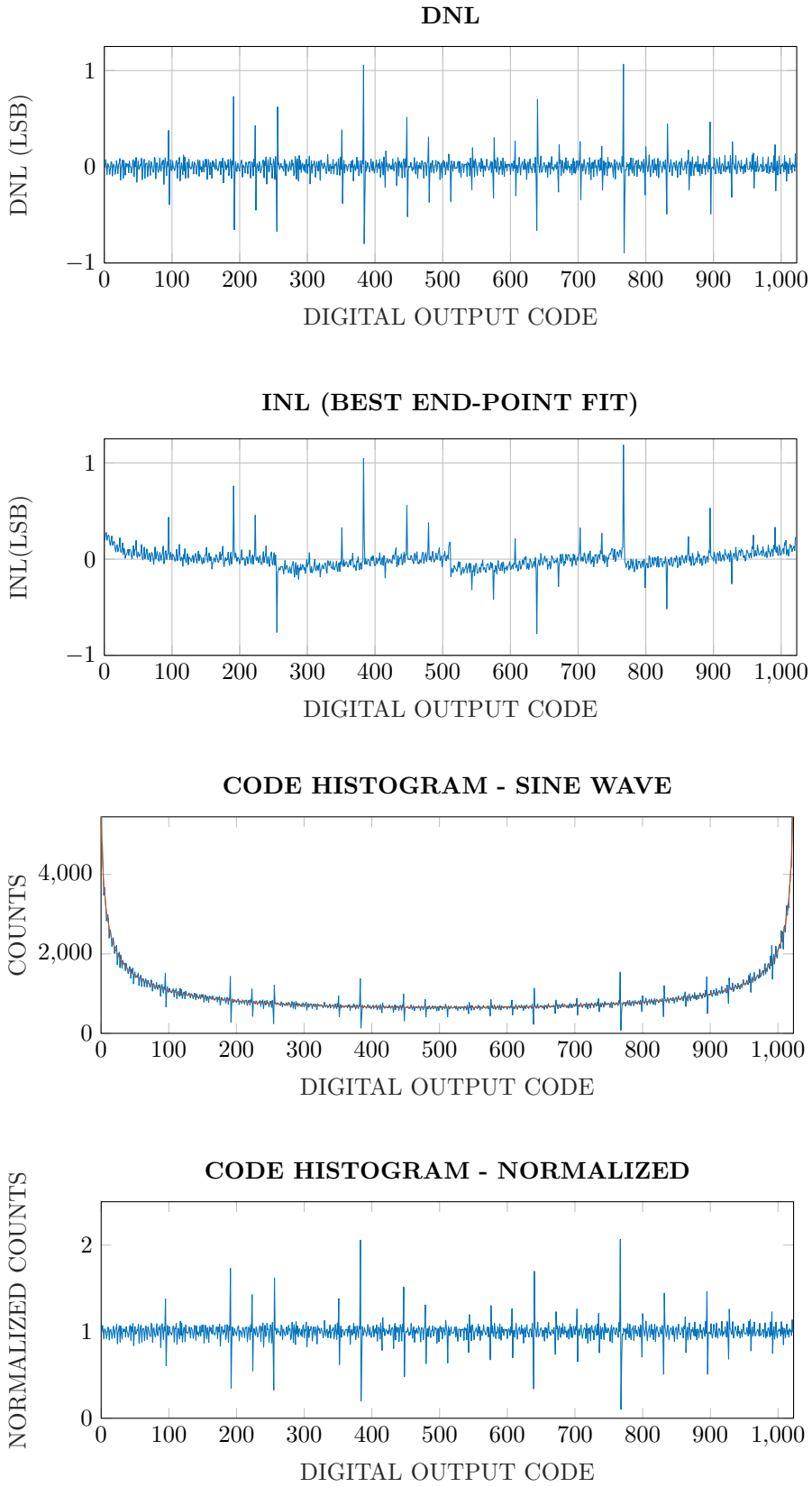


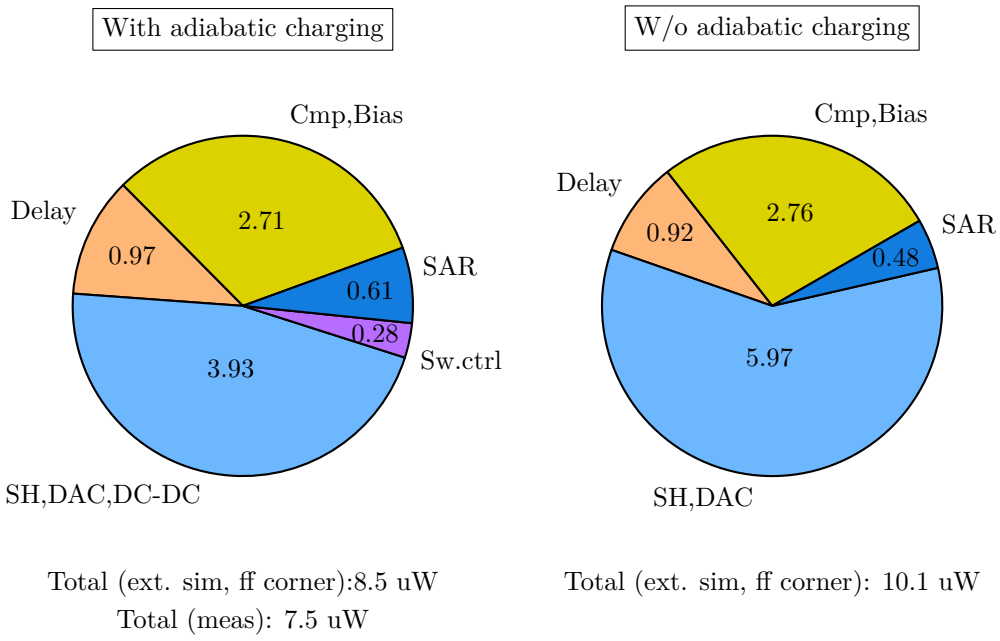
Figure 5.5.: Measured ADC-D static performance

5.2.3. Power consumption

The power consumption of the ADCs was taken from a power source for 10 codes equally distributed throughout the code range and averaged. The resulting power consumption of the ADC-A amounted to 7.5 uW and that of ADC-D to 19.6 uW. To further analyze the power consumption, the simulation of the extracted circuit was done over the process corners to estimate the corner of the received prototype based on the conversion speed achieved during measurements. The simulation results closest to the measured parameters were achieved in the fast-fast corner. Therefore, the simulation results provided further were taken from the ff-corner simulations.

The power consumption of the ADCs' building blocks was taken from the simulation of the hierarchically extracted layout. The top level of the ADC was simulated as is with all the subcircuits being represented by their extracted cell views. Most of the routing between switches and DAC bottom plates, as well as the top plates routing, was a part of the DAC cell layout and thus included in the extraction. Therefore, only the minimal routing parasitics between the blocks on the top level of the ADC hierarchy were left out of the simulation.

Pie-charts of the extracted simulations for ADC-A and ADC-D are presented in the left parts of Figures 5.6 and 5.7.



Total (ext. sim, ff corner):8.5 uW
Total (meas): 7.5 uW

Total (ext. sim, ff corner): 10.1 uW

Figure 5.6.: ADC-A power consumption pie chart

To analyze the adiabatic charging approach's influence on the ADCs power consumption, two more ADC circuits were created by removing the parts responsible for the 4-step charging from ADCs' schematics and layouts, to create 1-step charg-

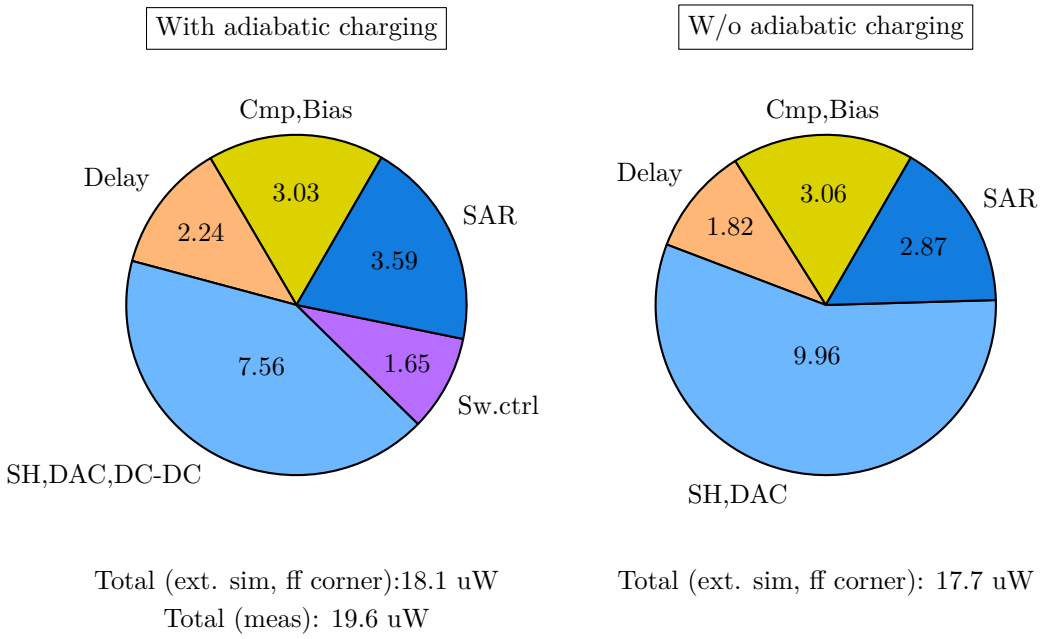


Figure 5.7.: ADC-D power consumption pie chart

ing ADCs from ADC-A and ADC-D. The DC-DC converters and switch controllers were removed, and the 5-way switches were replaced with 2-way switches. Delay circuits were left as is, with phase-shifted clock outputs being not used and left open.
The resulting 1 charging step versions of the produced ADCs allow for a fair comparison between the ADC-A in configuration with- and without the adiabatic charging and the same comparison for the ADC-D. The power consumption pie charts of the ADC-A and ADC-D without adiabatic charging are shown in the right parts of Figures 5.6 and 5.7.

Adiabatic switching in ADC-A:
Implemented adiabatic charging in ADC-A has reduced DAC power consumption by 2.04uW (34%) That value includes the DC-DC conversion losses, but does not include additional losses caused by the additional circuitry. The switch controllers required for the adiabatic charging procedure consume 280nW of extra power. Furthermore, the delay circuit in the case of adiabatic charging is used not only to delay the clock for the comparator but also to operate the switch controllers. The extra load capacitance there causes an increase in the delay chain power consumption. Additionally, the overall crosstalk caused by the phase-shifted circuitry increases the power consumption of the SAR control logic in the adiabatic counterpart, despite the block being identical in both circuits. The waveform demonstrating this effect is shown in Figure 5.8. This effect is only present in

circuits that feature adiabatic charging.
If all the extra power consumption is taken into account, the adiabatic charging circuitry in ADC-A consumes 3.93+0.28+0.05+0.13=4.39uW, reducing the non-adiabatic charging DAC power consumption by 26%.

Adiabatic switching in ADC-D:
The ADC-D sampling speed is 1MS/s versus 165kS/s for the ADC-A, which results in the power consumption of the digital circuits such as SAR and switch controllers increased by approximately 6 times despite the energy consumed by them per conversion cycle being the same as in the ADC-A. The delay element in ADC-D was modified to accommodate the faster conversion speed, therefore its power consumption is scaled up differently.
The adiabatic charging in the ADC-D has reduced the power consumption of the DAC by 2.4uW, which is 24% less than without the adiabatic charging if only the DAC and DC-DC are considered. The reduction is 10% less compared to the 34% in the case of ADC-A. The DC-DC converter in ADC-A is identical to one in the ADC-D, hence it has the same tank capacitance, however, the DAC unit capacitance value used in the ADC-D is only 8.5fF versus 51fF in ADC-A. On one hand it makes the efficiency of the power transfer higher due to the lower charge redistribution between the DC-DC and the load, however on the other hand it makes the switching losses in the DC-DC converter larger related to the power delivered to the load. This behaviour was covered in more detail in chapter 4.1.2. The switching losses in the DC-DC converter value can be expressed in $C_0V_{ref}^2$, where C_0 is the DAC unit capacitance. The switching losses in the DC-DC converter as small as $0.5C_0V_{ref}^2$ can significantly decrease the overall efficiency (Ch. 4.1.2, Fig. 4.17). In the case of ADC-D, the same DC-DC switching losses as in the ADC-A became the dominant source of overall conversion losses compared to small load capacitance minimizing the charge-redistribution. In such a scenario, where the load capacitance is significantly smaller than the DC-DC tank capacitance, the efficiency could be improved by reducing the DC-DC converter's charging frequency by removing the XOR clock multiplier. That would significantly reduce the switching losses while introducing only slightly more charge redistribution losses that represent less of an issue in the case of a small DAC capacitance.
Additional circuitry power consumption in the adiabatic charging ADC-D is of the same structure as in the ADC-A: switch controllers power consumption, higher power consumption of the delay chain due to it being connected to the extra load of the switch controllers and a cross-talk induced increased power consumption of the SAR control register together amounted to 2.79uW. Together with the DAC and DC-DC power consumption it gives 2.79+7.56=10.35 uW, which is

larger than 9.96uW consumed by the DAC without the adiabatic charging applied. Compared to ADC-A, the smaller unit capacitance in ADC-D reduced the portion of the energy consumed by the DAC, while the digital circuitry was consuming the same energy. This resulted in the power consumption of the additional digital circuitry becoming more significant and overpowering the savings provided by adiabatic charging.

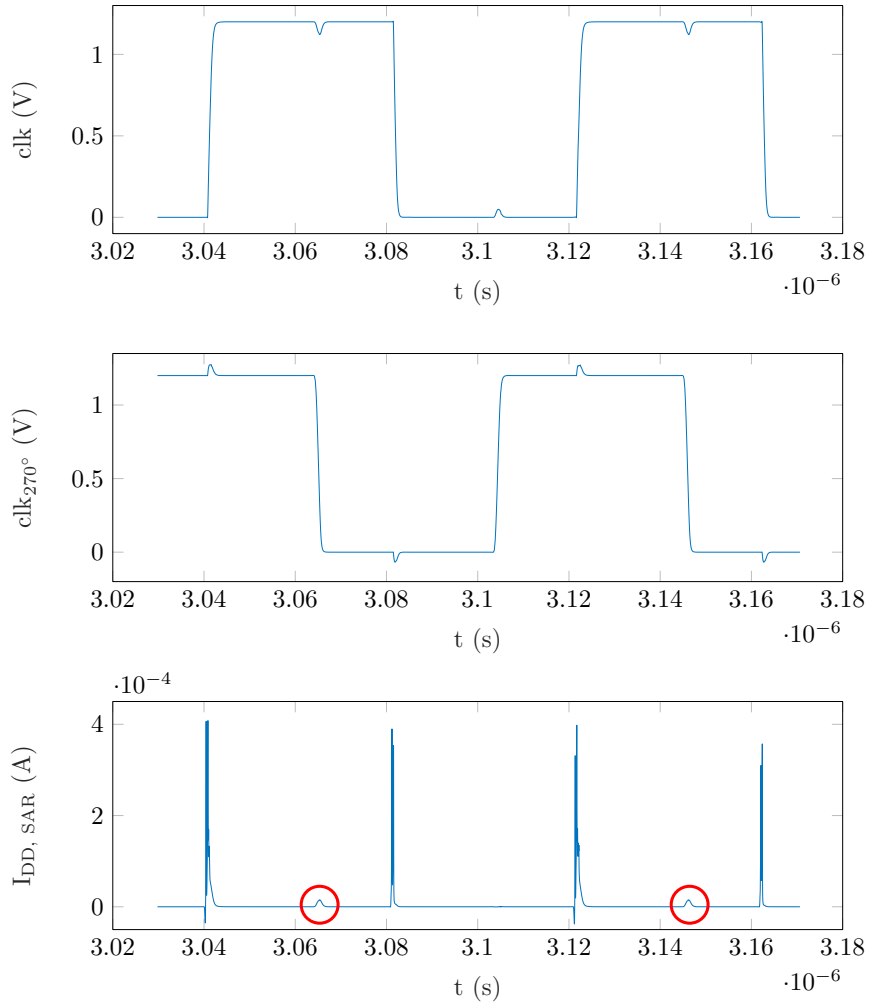


Figure 5.8.: Phase-shifted circuitry induced crosstalk influence on SAR controller power consumption

The case of the ADC-D highlights the limitation of the adiabatic charging approach applied to SAR ADC. The applicability of the approach is significantly dependent on the additional control logic power consumption and its relation to the DAC switching energy savings. Therefore, the approach is less suitable in the lower-resolution ADCs due to their smaller DAC capacitance. The approach is also less suitable in medium-resolution ADCs designed using small unit capacitor values such as ADC-D. In such designs, the reduction of the DAC capacitance can go as low as the minimum value complying with kT/C noise limits, which allows

for lower DAC power consumption but requires further calibration to compensate for the increased mismatch errors. Adiabatic charging savings in such circuits can be overpowered by the additional control logic. In order to better estimate the benefits of the adiabatic charging in a particular case, the switch controller energy consumption can be added to the DC-DC converter switching losses and entered in the model A.4 described in Chapter 4.1.2.
With an increase of SAR ADC resolution the control logic power consumption would increase linearly, whereas the binary-weighted DAC power consumption will grow by a factor of 2 with each bit if bridge-capacitor DACs are not considered. Moreover, the top-plate sampling ADCs such as the implemented Monotonic SAR rely on the bootstrapped input switch that can be more difficult to design with small enough nonlinearities to be used in designs above 12 Bit. For example, to use a bootstrapped input switch in a 16-bit ADC, it is required to use dynamically driven deep-nwell to control the pass-transistor back-bias [Pel22, BSK+11]. The limitations of the top-plate sampling make the bottom-plate sampling and conventional switching scheme more attractive for the resolution above 12-bit. Such architectures can benefit from adiabatic charging due to the significantly higher power consumption of the conventional DAC switching scheme.

5.2.4. Summarized performance

Table 5.3 shows the summarized performance of both ADCs.

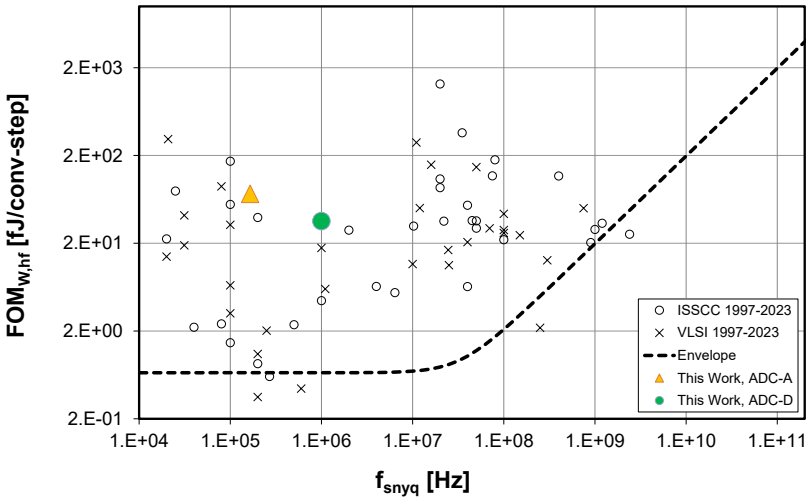
	ADC-A	**ADC-D**
Process (nm)	65	
Supply (V)	1.2	
Area(mm^2)	0.456	
F_S (kS/s)	165	1000
DNL (LSB)	+0.87/-0.79	+1.07/-0.90
INL (LSB)	+0.94/-0.28	+1.19/-0.77
SNDR (dB)	57.63	56.52
SFDR (dB)	75.83	72.55
SNR (dB)	57.66	56.73
THD (dB)	78.4	69.43
ENOB (Bit)	9.28	9.1
Power (uW)	7.5	19.6
FoMW (fJ/c.st.)	73.1	35.7
FoMS (dB)	158	160.6

Table 5.3.: Summarized performance

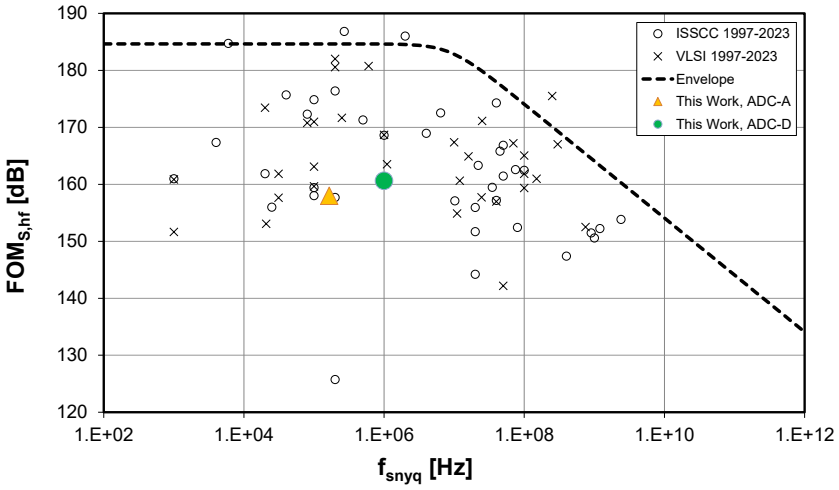
Schreier and Walden Figures-of-Merit were calculated and placed against the Nyquist-rate SAR ADCs from the VLSI Symposium and ISSCC conference collected over the years in the ADC survey [Mur]. Figures 5.9a and 5.9b show the

comparison.

The comparison against the state-of-the-art ADCs shows acceptable performance, although the produced prototypes do not outperform the competitors. With the prototypes aimed to prove the savings in DAC switching energy by stepwise charging (covered in detail in Section 5.2.3), the design approach to the surrounding circuitry was biased towards conservative methods. Together with the chips being fabricated in the fast-fast corner it led to only satisfactory overall power consumption of the proof-of-concept ADC prototypes.



(a) Walden figure of merit



(b) Schreier figure of merit

Figure 5.9.: Comparison of the produced ADC with the state of the art [Mur]

6 Summary

The work presents a study of the adiabatic charging approach applied to SAR ADCs. The adiabatic charging was applied to the switched-capacitor DAC in the ADC in the form of charging the DAC capacitors with a series of equidistant voltage steps. The concept of adiabatic charging is not new: it is a known way to maximize the efficiency of capacitors' charging in circuits such as switched-capacitor DC-DC converters. However, when applied to DAC, little published data was available regarding that.

The thesis starts with an estimation of the benefits of stepwise charging applied to a conventional SAR ADC. The average DAC switching energy was derived as a function of resolution and the number of charging steps. The calculations were verified in MATLAB.

Further development required the design of an ADC prototype. First, a switching scheme had to be chosen. Besides the conventional switching scheme that was evaluated for adiabatic charging, numerous other switching schemes were reported over the years, varying in system-level demands and often trading certain shortcomings for energy consumption benefits. Once the switching scheme was selected, the other aspects of the stepwise charging implementation with the chosen monotonic switching scheme were put into consideration. The reference voltage generator's influence on energy savings, depending on the configuration, was estimated in MATLAB. Based on that, the optimum number of charging steps was selected for future development.

As a result, two 10-bit ADC prototypes were developed. The prototypes use different DAC unit capacitor sizes and operate at different speeds. The architectures of the prototypes were designed in a way to keep additional control circuitry outside of the SAR control logic register to keep the approach independent from the DAC switching scheme and keep the possibility of using it with the other schemes with minimal modification. This also allowed for better distinguishing the stepwise charging system-level trade-offs when it comes to control logic complexity.

The prototypes were fabricated in a 65nm CMOS process and measured. Two

different configurations of the same architecture showed different results in terms of the overall reduction in power consumption. To better highlight the power savings, detailed power consumption charts were made based on the extracted simulation. Additionally, the adiabatic charging circuitry was removed from the layouts of the produced prototypes, thus creating a non-adiabatic version of each produced ADC. That allowed for the side-by-side comparison of each ADC with its non-adiabatic counterpart to evaluate the benefits of the adiabatic charging approach in each case.
The results of the work presented the case of an ADC with a larger DAC capacitance, where the overall DAC switching power savings (including all the additional circuitry) amounted to 26%, as well as the case of a smaller DAC capacitance configuration of the second prototype, showcasing the limitations of the approach, where the power savings of adiabatic charging were overpowered by the additional control logic and DC-DC converter switching losses.
Overall, the obtained results demonstrate that adiabatic charging can help reduce power consumption in SAR ADCs. In designs with small DAC unit capacitors, extra care is required in order to gain the benefits. The presented design approach and MATLAB models allow a designer to estimate and include the losses to determine whether adiabatic charging will be effective within a particular ADC configuration and process.

Future work:
A conservative design approach to the proof-of-concept prototypes resulted in only a satisfactory figure of merit when compared to the state-of-the-art designs. There is an opportunity to re-optimize subcircuits such as the comparator and delay line, which will allow for a significant reduction of the overall power consumption. Reducing the complexity of the control logic in both, the SAR register and the switch controllers as well as the integration between both will reduce the digital penalty of the adiabatic charging approach thus allowing it to be used with smaller DAC capacitance. Increasing the resolution to 12-bit will further improve the ratio between the energy savings and control logic penalty due to the DAC capacitance growing with resolution at a faster rate than the control logic which is only required to provide two additional conversion steps. Additionally, applying adiabatic charging to a number of MSB capacitors in the DAC matrix instead of a complete DAC will further reduce the control logic penalty and better balance the efficiency improvement in the designs with the smaller unit capacitors.

A Appendix

A.1. Average switching energy of an n-th conversion step of a stepwise conventional SAR ADC

The detailed derivation of the average switching energy during an n-th conversion step of a conventional SAR ADC with M-step stepwise charging applied (Chapter 3.4.3, Equation (3.42))

$$\overline{E_n} = \frac{\sum_{m=1}^{M} E_{n,m,up} + \sum_{m=1}^{M} E_{n,m,down}}{2} \tag{A.1}$$

$$= \frac{1}{2}\Bigg[\sum_{m=1}^{M} \Big[2^{N-n} C_0 V_{REF} \left(0 - \frac{1}{M}\frac{V_{REF}}{2^{n+1}}\right) \cdots \tag{A.2}$$

$$+ 2^{N-1-n} C_0 \frac{m}{M} V_{REF} \left(\frac{1}{M} V_{REF} - \frac{1}{M}\frac{V_{REF}}{2^{n+1}}\right) \Big] \cdots$$

$$+ \sum_{m=1}^{M} \Big[2^{N-n} C_0 \frac{M-m}{M} V_{REF} \left(-\frac{1}{M} V_{REF} - (-\frac{1}{M}\frac{V_{REF}}{2^{n+1}})\right) \cdots$$

$$+ 2^{N-1-n} C_0 \frac{m}{M} V_{REF} \left(\frac{1}{M} V_{REF} - (-\frac{1}{M}\frac{V_{REF}}{2^{n+1}})\right) \Big] \Bigg]$$

$$= \frac{1}{2} C_0 V_{REF}^2 \sum_{m=1}^{M} \Bigg[2^{N-n} \left(-\frac{1}{M}\frac{1}{2^{n+1}}\right) + 2^{N-1-n}\frac{m}{M}\left(\frac{1}{M} - \frac{1}{M}\frac{1}{2^{n+1}}\right) \cdots \tag{A.3}$$

$$+ 2^{N-n}\frac{M-m}{M}\left(-\frac{1}{M} + \frac{1}{M}\frac{1}{2^{n+1}}\right) + 2^{N-1-n}\frac{m}{M}\left(\frac{1}{M} + \frac{1}{M}\frac{1}{2^{n+1}}\right) \Bigg]$$

$$= \frac{1}{2} C_0 V_{REF}^2 \sum_{m=1}^{M} \Bigg[-2^{N-n}\frac{1}{M}\frac{1}{2^{n+1}} + 2^{N-n}\left(1 - \frac{m}{M}\right)\left(-\frac{1}{M} + \frac{1}{M}\frac{1}{2^{n+1}}\right) \cdots \tag{A.4}$$

$$+ 2^{N-1-n}\frac{m}{M}\left(\frac{1}{M} - \frac{1}{M}\frac{1}{2^{n+1}} + \frac{1}{M} + \frac{1}{M}\frac{1}{2^{n+1}}\right) \Bigg]$$

$$= \frac{1}{2} C_0 V_{REF}^2 \sum_{m=1}^{M} \Bigg[-2^{N-n}\frac{1}{M}\frac{1}{2^{n+1}} + 2^{N-n}\left(-\frac{1}{M} + \frac{1}{M}\frac{1}{2^{n+1}}\right) \cdots \tag{A.5}$$

$$
\begin{aligned}
&- 2^{N-n}\frac{m}{M}\left(-\frac{1}{M}+\frac{1}{M}\frac{1}{2^{n+1}}\right)+2^{N-1-n}\frac{m}{M}\frac{2}{M}\Bigg] \\
&= \frac{1}{2}C_0V_{REF}^2\sum_{m=1}^{M}\Bigg[-2^{N-n}\frac{1}{M}-2^{N-n}\frac{m}{M}\left(-\frac{1}{M}+\frac{1}{M}\frac{1}{2^{n+1}}\right)\cdots \qquad \text{(A.6)} \\
&\quad + 2^{N-1-n+1}\frac{m}{M}\frac{1}{M}\Bigg] \\
&= \frac{1}{2}C_0V_{REF}^2\sum_{m=1}^{M}\left[-2^{N-n}\frac{1}{M}-2^{N-n}\frac{m}{M}\left(-\frac{1}{M}+\frac{1}{M}\frac{1}{2^{n+1}}-\frac{1}{M}\right)\right] \qquad \text{(A.7)} \\
&= \frac{1}{2}C_0V_{REF}^2 2^{N-n}\sum_{m=1}^{M}\left[-\frac{1}{M}+\frac{m}{M^2}\left(2-\frac{1}{2^{n+1}}\right)\right] \qquad \text{(A.8)} \\
&= \frac{1}{2}C_0V_{REF}^2 2^{N-n}\left[\frac{1}{M^2}\left(2-\frac{1}{2^{n+1}}\right)\sum_{m=1}^{M}m-\frac{1}{M}\sum_{m=1}^{M}1\right] \qquad \text{(A.9)} \\
&= \frac{1}{2}C_0V_{REF}^2 2^{N-n}\left[\frac{1}{M^2}\left(2-\frac{1}{2^{n+1}}\right)\frac{M(M+1)}{2}-1\right] \qquad \text{(A.10)} \\
&= \frac{1}{2}2^{N-n}C_0V_{REF}^2\left[\left(1-\frac{1}{2^{n+2}}\right)\frac{M+1}{M}-1\right] \qquad \text{(A.11)}
\end{aligned}
$$

A.2. Switching energy of a stepwise conventional SAR ADC (Matlab)

The MATLAB model of a conventional SAR ADC with applied stepwise charging used in Chapter 3.4.3 to validate the derived average switching energy (Eq. (3.43)) against "avg_en" model output and calculate codewise switching energy "en" for various configurations shown in Figure 3.16. The model has variable resolution "res" and variable number of stepwise charging steps "steps".

```
function [avg_en,en]=conv_sar_sw_en_multistep(res,steps
    )

en(1:2^res)=0;

for v_in=1:2^res
 en(v_in)=conv_sar_sw_en_multistep_core(v_in,res,steps)
    *2; % x2 to mimic the differential architecture.
    Since the negative dac energy is the same as
    positive
end
avg_en=mean(en);


function [sw_en]=conv_sar_sw_en_multistep_core(v_in,res
    ,steps)
vref=2^res;
v_dac(1:res+1)=0;      %Dac voltage
v_sw(1:res+1,1:res+1)=0;       %Voltage at swithces
dac_w(1:res+1)=0; %DAC weights
E(1:res)=0;
cursor=0;

%DAC assembly
for i=1:res
 dac_w(i)=1/2^(i); %ratios of every capacitor to the
    total dac capacitance, e.g. 1/2, 1/4, ..
 dac_c(i)=2^(res-i); %size of every capacitor in the
    matrix, e.g. 256, 128, ...
end
```

```
dac_w(res+1)=1/2^(res);
dac_c(res+1)=2^(0);

%sample
v_sw(1,1:res+1)=v_in;
v_dac(1)=0;
cursor=cursor+1;

%hold
v_sw(2,1:res+1)=0;
v_dac(2)=v_dac(1)-v_in;
cursor=cursor+1;

%shift the sampled voltage (necessary step for the
   conventional sar)
for s=1:steps
v_sw(2+s,1:res+1)=v_sw(2+(s-1),1:res+1);          %
   transfer the switch voltages from the previous step
   (previous row in the array)
v_sw(2+s,1)=vref*(s/steps);                        %
   switch the MSB cap
v_dac(2+s)=v_dac(2+(s-1))+(v_sw(2+s,1)-v_sw(2+(s-1),1))
   *dac_w(1);    %dV of the MSB switch multiplied to
   the ratio
  for k=1:(res+1)
    E(1)=E(1)+dac_c(k)*v_sw(2+s,k)*((v_sw(2+s,k)-v_sw
       (2+(s-1),k))-(v_dac(2+s)-v_dac(2+(s-1)))); %
       energy summed for every cap in "dac matrix" as E
       (k)=C(k)*V_sw(k)*(dV_sw(k)-dV_dac)
  end
cursor=cursor+1;
end
E_norm(1)=E(1)/(vref^2);

%conversion
for n=1:(res-1)
if v_dac(cursor)<0
    for s=1:steps
        v_sw(cursor+1,1:res+1)=v_sw(cursor,1:res+1);
```

```
54          v_sw(cursor+1,n+1)=vref*(s/steps);      %add
               the bit at trial
55          v_dac(cursor+1)=v_dac(cursor)+(v_sw(cursor+1,n
               +1)-v_sw(cursor,n+1))*dac_w(n+1); %dV of the
                current switch multiplied to the ratio
56          for k=1:(res+1)
57               E(n+1)=E(n+1)+dac_c(k)*v_sw(cursor+1,k)*((
                    v_sw(cursor+1,k)-v_sw(cursor,k))-(v_dac
                    (cursor+1)-v_dac(cursor))); %energy
                    summed for every cap in "dac matrix" as
                     E(k)=C(k)*V_sw(k)*(dV_sw(k)-dV_dac)
58          end
59          cursor=cursor+1;
60          E_norm(n+1)=E(n+1)/(vref^2);
61      end
62  else
63      for s=1:steps
64          v_sw(cursor+1,1:res+1)=v_sw(cursor,1:res+1);
65          v_sw(cursor+1,n)=vref*(1-s/steps);      %
               subtract the previous bit
66          v_sw(cursor+1,n+1)=vref*(s/steps);  %add the
               bit at trial
67          v_dac(cursor+1)=v_dac(cursor)+(v_sw(cursor+1,n)
               -v_sw(cursor,n))*dac_w(n)+(v_sw(cursor+1,n
               +1)-v_sw(cursor,n+1))*dac_w(n+1); %dV of the
                switches multiplied by the ratios
68          for k=1:(res+1)
69              E(n+1)=E(n+1)+dac_c(k)*v_sw(cursor+1,k)*((
                    v_sw(cursor+1,k)-v_sw(cursor,k))-(v_dac(
                    cursor+1)-v_dac(cursor))); %energy
                    summed for every cap in "dac matrix" as
                    E(k)=C(k)*V_sw(k)*(dV_sw(k)-dV_dac)
70          end
71          cursor=cursor+1;
72          E_norm(n+1)=E(n+1)/(vref^2);
73      end
74  end
75  sw_en=sum(E_norm);
76  end
```

A.3. Switching energy of a stepwise monotonic SAR ADC (Matlab)

The MATLAB model of a monotonic SAR ADC with applied stepwise charging that was used in Chapter 4.1.1 to calculate codewise switching energy that was shown in Figure 4.8. The model takes ADC resolution N and the number of charging steps m and calculates the average switching energy stored in the variable "Energy" and the codewise switching energy for every code stored in the variable "SwEn".

```
function [Energy,SwEn]= SwEnMonotNsteps(N,m)
N=N-1; % correction for the 1-bit less DAC resolution
   in monotonic switching scheme
Vin=-2^N+0.5;
for k=1:2^(N+1)
Vref=2^N;
coden(1:N)=1;
codep(1:N)=1;
i=1;
j=1;
l=1;
Vxp(1)=Vref/2+Vin/2;
Vxp(2:N+1)=0;
Vxn(1)=Vref/2-Vin/2;
Vxn(2:N+1)=0;
dVxp(1:N)=0;
dVxn(1:N)=0;
Enp=0;
Enn=0;
CMP(1:N)=0;

    for i=1:N
    CMP(i)=Vxp(i)-Vxn(i);
    if (CMP(i)>=0)
        codep(i)=0;
        for l=1:m
        Vxp(i+1)=Vxp(i)-(2^(N-i)/m);
        Vxn(i+1)=Vxn(i);
        dVxp(i)=Vxp(i+1)-Vxp(i);
```

```
29          Vxp(i)=Vxp(i+1);
30          for j=1:N
31              if (codep(j)==1)
32                  Enp=Enp+(2^(N-j))*(-1*dVxp(i)/Vref);
33              end
34          end
35          Enp=Enp+(2^0)*(-1*dVxp(i)/Vref)+((m-l)/m)*(2^(N
               -i)*((-1/m)-1*dVxp(i)/Vref));
36          end
37      else
38          coden(i)=0;
39          for l=1:m
40          Vxn(i+1)=Vxn(i)-(2^(N-i)/m);
41          Vxp(i+1)=Vxp(i);
42          dVxn(i)=Vxn(i+1)-Vxn(i);
43          Vxn(i)=Vxn(i+1);
44          for j=1:N
45              if (coden(j)==1)
46                  Enn=Enn+(2^(N-j))*(-1*dVxn(i)/Vref);
47              end
48          end
49          Enn=Enn+(2^0)*(-1*dVxn(i)/Vref)+((m-l)/m)*(2^(N
               -i)*((-1/m)-1*dVxn(i)/Vref));
50          end
51      end
52      end
53      SwEn(k)=Enn+Enp;
54      Vin=Vin+1;
55  end
56  Energy=mean(SwEn);
57  end
```

A.4. Switching energy of a stepwise monotonic SAR ADC incl. charge redistribution (Matlab)

The MATLAB model of a monotonic SAR ADC with applied stepwise charging that was used in Chapter 4.1.2 to calculate average DAC switching energy that was shown in Figures 4.16 and 4.17. The model emulates the stepwise charging procedure with intermediate step voltage sources represented with capacitor tanks. The capacitance of a single tank is defined by the input parameter "storecap". The model also takes ADC resolution N and the number of charging steps m and calculates the average DAC switching energy stored in the output variable "Energy". The variable "Loss" in line 23 can be set to include the energy losses at a single charging step, e.g. energy lost to charge parasitic capacitances in MOSFET switches of the DC-DC converter. These losses require to be expressed in $C_0 V_{ref}^2$.

```
1  function [Energy]=
       SwEnMonotNsteps_Charge_Redistr_Q_withdrawn(N,m,
       storecap)
2  %in this model the charge redistribution energy is
       calculated as energy
3  %withdrawn from the capacitor tank: using the
       difference between energy
4  %that was stored initially and the resulting residual
       energy in the tank
5  N=N-1; % correction for the 1-bit less DAC resolution
       in monotonic switching scheme
6  Vin=-2^N+0.5;
7  for k=1:2^(N+1)
8  Vref=2^N;
9  coden(1:N)=1;
10 codep(1:N)=1;
11 i=1;
12 j=1;
13 l=1;
14 Vxp(1)=Vref/2+Vin/2;
15 Vxp(2:N+1)=0;
16 Vxn(1)=Vref/2-Vin/2;
17 Vxn(2:N+1)=0;
```

```
dVxp(1:N)=0;
dVxn(1:N)=0;
Enp=0;
Enn=0;
CMP(1:N)=0;
Loss=0;
    for i=1:N
    CMP(i)=Vxp(i)-Vxn(i);
    Vxp1st=Vxp(i);%Saved Vx before applying any steps
    Vxn1st=Vxn(i);%Saved Vx before applying any steps
    Vswp(1:m)=Vref;
    Vswn(1:m)=Vref;
    Cload=1/(1/(2^(N-i))+1/(2^N-2^(N-i)));
    r=storecap/(Cload+storecap);
    if (CMP(i)>=0)
        codep(i)=0;
        for l=1:m
        if (l<m)
        Vswp(l+1)=((m-l)/m)*Vref*r+Vswp(l)*(1-r); %
           voltage at the switch at a given charging
           step incl. redistr. dep. on the prev.
           voltage and ratio "r".
        dVswp(l)=Vswp(l+1)-Vswp(l); %switches down -
           will be a negative value
        Vxp(i+1)=Vxp(i)+dVswp(l)*(2^(N-i)/2^(N)); %
           subtract dV at the switch corrected by the
           relative weight
        else
        Vswp(l+1)=0; % Last step - ground
        dVswp(l)=Vswp(l+1)-Vswp(l);
        Vxp(i+1)=Vxp1st-2^(N-i);
        end
        Vxn(i+1)=Vxn(i);
        dVxp(i)=Vxp(i+1)-Vxp(i);
        Vxp(i)=Vxp(i+1);
        Vswp(l)=Vswp(l+1);
        for j=1:N
            if (codep(j)==1)
                Enp=Enp+(2^(N-j))*(-1*dVxp(i)/Vref);
```

```
51              end
52          end
53          Enp=Enp+(2^0)*(-1*dVxp(i)/Vref)+(1/2)*storecap
               *(((m-l)/m)^2-(Vswp(l)/Vref)^2)+Loss;
54          end
55      else
56          coden(i)=0;
57          for l=1:m
58          if (l<m)
59          Vswn(l+1)=((m-l)/m)*Vref*r+Vswn(l)*(1-r); %
               voltage at the switch at a given charging
               step incl. redistr. dep. on the prev.
               voltage and ratio "r".
60          dVswn(l)=Vswn(l+1)-Vswn(l); %switches down -
               will be a negative value
61          Vxn(i+1)=Vxn(i)+dVswn(l)*(2^(N-i)/2^(N)); %
               subtract dV at the switch corrected by the
               relative weight
62          else
63          Vswn(l+1)=0; % Last step is ground
64          dVswn(l)=Vswn(l+1)-Vswn(l);
65          Vxn(i+1)=Vxn1st-2^(N-i);
66          end
67          Vxp(i+1)=Vxp(i);
68          dVxn(i)=Vxn(i+1)-Vxn(i);
69          Vxn(i)=Vxn(i+1);
70          Vswn(l)=Vswn(l+1);
71          for j=1:N
72              if (coden(j)==1)
73                  Enn=Enn+(2^(N-j))*(-1*dVxn(i)/Vref);
74              end
75          end
76          Enn=Enn+(2^0)*(-1*dVxn(i)/Vref)+(1/2)*storecap
               *(((m-l)/m)^2-(Vswn(l)/Vref)^2)+Loss;
77          end
78      end
79      end
80      SwEn(k)=Enn+Enp;
81      Vin=Vin+1;
```

```
82 end
83 Energy=mean(SwEn);
84 end
```

A.5. Transistor dimensions

Device name	Width (um)	Length (um)
P1-2	0.08	0.06
N1-4	0.08	0.06
N5	1	0.06

Table A.1.: Input switch (Fig. 4.22) transistor dimensions

Device name	Width (um)	Length (um)
P1	3	0.2
P2	0.08	0.06
P3-4	0.16	0.08
P5-8	0.08	0.06
N1-4	0.5	0.06
N5-6	1	0.06
N7-8	1	0.06
N9	1	0.06

Table A.2.: Comparator (Fig. 4.23) transistor dimensions

Device name	Width (um)	Length (um)
P1	0.21	0.06
P2-5	1	0.06
N1	0.15	0.06
N2-9	0.75	0.06

Table A.3.: DC-DC converter (Fig. 4.30) transistor dimensions

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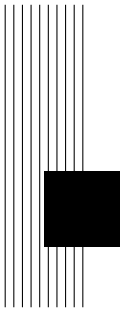

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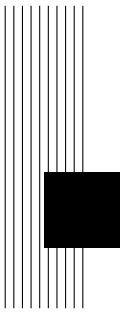

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