Ein Beitrag zur Herstellung und Charakterisierung von Galliumnitrid Trench MOSFETs auf nativen Substraten

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Fabrication and characterization of gallium nitride trench MOSFETs on native substrates

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Abstract

In recent time, an increase in electrification has been observed, and with fields like digitalization, e-mobility and renewable energy rapidly growing, this trend will continue in the years to come. The need for efficient and compact systems for electrical power conversion is more important than ever and the key technology to achieve this are semiconductor based converters and inverters. But silicon, the predominant semiconductor material in past and present, has reached its physical limits. As far as power semiconductor devices are concerned, highly complex device types are required to further increase performance. This jeopardizes processing speed, cost and reliability. Excellent resilience against high voltage and thermal stress make wide band gap semiconductors such as gallium nitride or silicon carbide a viable alternative, especially for power conversion applications. In this work, gallium nitride trench metal oxide semiconductor field effect transistors were fabricated on native substrates and were electrically characterized. The focus was on the metal oxide semiconductor inversion channel and the mobility of the carriers therein. A novel, chlorine-free plasma etching procedure was developed to fabricate the gate trenches. Subsequent wet etching in alkaline solution resulted in vertical trench sidewalls that are oriented along the gallium nitride crystal planes due to a high degree of anisotropy in the wet etch process. Compared to state of the art processing, the gate structure was fabricated completely metal free and is based on a gate electrode made from polycrystalline silicon. Gate dielectric and gate electrode were fabricated by means of low pressure chemical vapor deposition, a process that yields high quality layers with excellent homogeneity and conformal deposition. Gate structures with different dielectrics were characterized by using planar and trench metal oxide semiconductor capacitors. Dielectric breakdown field strength, leakage current density, hysteresis effects and bulk oxide trap generation were examined. A post deposition annealing of the dielectric layer, prior to the fabrication of the gate electrode, was found to improve thermal robustness and to reduce hysteresis effects in the case of a silicon dioxide layer. A generally superior performance in terms of thermal stability, dielectric breakdown field strength and hysteresis effects was observed for structures with the polycrystalline silicon compared to structures with a commonly used metal gate electrode. The combination of silicon dioxide as dielectric and polycrystalline silicon as gate electrode emerged as the best choice and was used for the fabrication of the transistors. The on-state performance of the fabricated transistors was comparable with state of the art devices with a high on to off current ratio of 10^{10} and an area-specific on-resistance of $\approx 10\,\mathrm{m\Omega\,cm^2}$. The inversion channel field effect mobility was 10 and $30\,\mathrm{cm^2/Vs}$ at a vertical and planar interface, respectively. The low values for threshold voltage and channel mobility suggest

high interface charge and defect density. Technology computer-aided design simulations support this assumption. This work shows, that chlorine- and metal-free trench gate structures are competitive to state of the art processing and can build the foundation for future work with the focus on the interface between oxide layer and semiconductor.

Kurzfassung

Die vergangenen Jahre waren von einer zunehmenden Elektrifizierung geprägt und mit den stark wachsenden Bereichen Digitalisierung, erneuerbare Energien und Elektromobilität wird sich dieser Trend in den kommenden Jahren fortsetzen. Effiziente und kompakte Systeme zur Umwandlung elektrischer Energie werden wichtiger denn je. Die Schlüsselkomponente, um solche Systeme zu realisieren, ist der halbleiterbasierte Konverter oder Inverter. Allerdings hat Silizium, das mit Abstand wichtigste und verbreitetste Halbleitermaterial, seine physikalischen Grenzen erreicht. Zumindest im Hinblick auf Leistungshalbleiterbauteile werden immer ausgefallenere und komplexere Lösungen benötigt, was sich wiederum in den Herstellungskosten und der Bauteilzuverlässigkeit niederschlägt. Hervorragende Robustheit bezüglich hoher elektrischer Spannung und thermischer Belastung machen Wide-Bandgap-Halbleiter wie Galliumnitrid oder Siliziumkarbid zu vielversprechenden Alternativen, speziell für Leistungsbauteile. In dieser Arbeit wurden Galliumnitrid basierte Trench Metall-Oxid-Halbleiter-Feldeffekttransistoren auf nativen Substraten hergestellt und vermessen. Der Fokus lag auf dem Metall-Oxid-Halbleiter-Inversionskanal und der Mobilität der Ladungsträger im Kanal. Ein neuartiger, chlorfreier Plasmaätzprozess wurde verwendet, um die Gatetrenches herzustellen. Anschließendes nasschemisches Nachbehandeln in einer alkalischen Lösung führte zu vertikalen Trenchseitenwänden die sich aufgrund der ausgeprägten Anisotropie der Nassätzung entlang der Facetten des Galliumnitridkristalls ausbildeten. Im Gegensatz zum üblichen Vorgehen wurde die Gatestruktur in dieser Arbeit vollständig metallfrei prozessiert und basiert auf einer Gateelektrode aus polykristallinem Silizium. Gatedielektrikum und Gateelektrode wurden mittels chemischer Gasphasenabscheidung bei niedrigem Druck hergestellt, einem Prozess der qualitativ hochwertige, homogene und konforme Schichten ergibt. Verschiedene Gatedielektrika wurden anhand von planaren und getrenchten Metall-Oxid-Halbleiter-Kondensatoren untersucht. Dielektrische Durchbruchfestigkeit, Leckstromdichte, Hystereseeffekte und die Entstehung von Traps wurden untersucht. Im Fall von Siliziumdioxid als Gatedielektrikum erhöhte eine der Abscheidung nachgelagerte Temperprozedur, vor der Deposition der Gateelektrode, die thermische Belastbarkeit und reduzierte Hystereseeffekte. Im Vergleich zu Strukturen mit einer metallenen Gateelektrode zeigten solche mit einer Gateelektrode aus polykristallinem Silizium eine generell bessere Performance hinsichtlich thermischer Stabilität, elektrischer Durchbruchfestigkeit und Hysterese. Die Kombination aus Siliziumdioxid als Gatedielektrikum und polykristallinem Silizium als Gateelektrode stellte sich als die beste Wahl heraus und bildete die Basis für die Herstellung der Transistoren. Die on-State Performance dieser Transistoren war vergleichbar mit State-of-the-Art Bauteilen. Das On-Off-Stromverhältnis lag

bei ca. 10^{10} und der flächenspezifische On-Widerstand betrug $\approx 10\,\mathrm{m\Omega\,cm^2}$. Die Ladungsträgermobilität im Inversionskanal war $10\,\mathrm{cm^2/Vs}$ für ein vertikales Interface und $30\,\mathrm{cm^2/Vs}$ für ein planares. Die niedrige Schwellspannung und die geringe Ladungsträgermobilität deutet auf eine hohe Dichte an Interfaceladung und Defekten hin. Diese Vermutung wurde durch computergestützte Simulationen untermauert. In dieser Arbeit wurde gezeigt, dass chlor- und metallfrei-prozessierte Trenchgatestrukturen kompetitive Resultate liefern und die Ergebnisse bilden die Basis für weiterführende Untersuchungen deren Fokus auf dem Interface zwischen Halbleiter und Gatedielektrikum liegen sollte.

Acronyms

2DEG	two dimensional electron gas
AFM	atomic force microscopy
ALD	atomic layer deposition
aSi	amorphous silicon
CV	capacitance voltage
CVD	chemical vapor deposition
EBI	etching barrier index
EDX	energy-dispersive X-ray spectroscopy
FN	Fowler-Nordheim
GaF_3	gallium trifluoride
GaN	gallium nitride
HEMT	high electron mobility transistor
ICP	inductively coupled plasma
IGBT	insulated gate bipolar transistor
IV	current voltage
KOH	potassium hydroxide
LPCVD	low pressure chemical vapor deposition
MIS	metal insulator semiconductor
MOCVD	metal organic chemical vapor deposition
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
PECVD	plasma enhanced chemical vapor deposition
poly Si	polycrystalline silicon
SEM	scanning electron microscopy
SiC	silicon carbide

TBOX	thick bottom oxide
TCAD	technology computer-aided design
TMAH	tetramethyl-ammonium hydroxide
VD-MOSFET	vertical double diffused metal oxide semiconductor field effect transistor
WBG	wide band gap

Symbols

A_{active}	Active chip area	cm^2
$BFOM_{\text{norm}}$	Baliga's figure of merit normalized to the value for silicon	-
$C^*_{\text{ox,diel}}$	Area specific capacitance of the oxide or dielectric layer	F/cm^2
C^*_{QS}	Area specific quasi static capacitance	F/cm^2
$D^{(-)}_{\text{Acc}}, D^{(+)}_{\text{Don}}$	Density of (ionized) acceptor or donor like defect states	$\text{cm}^{-2}\,\text{eV}^{-1}$
D_{Pad}	Pad distance at a transfer length module	µm
$\varepsilon_{\text{diel}}$	Dielectric constant of the dielectric	-
ε_{r}	Dielectric constant (in general)	-
ε_{S}	Dielectric constant of the semiconductor	-
$E_{\text{A,D}}$	Ionization energy of acceptors or donors	eV
EBI	Etching barrier index	$1/\mathring{A}^2$
E_{B}	Device breakdown field strength	MV/cm
E_{crit}	Critical electric field strength	MV/cm
E_{F}	Fermi energy	eV
E_{F_p}	Fermi energy in th p-type semiconductor	eV
E_{G}	Energy band gap	eV
E_{i}	Intrinsic Fermi energy	eV
$E_{\text{ox, diel}}$	Electric field strength in the oxide or dielectric layer	MV/cm
Φ_{B}	Band barrier height at the dielectric interface	V
Φ_{bi}	Built-in voltage	V
Φ_{bulk}	Semiconductor bulk potential	V
Φ_{surf}	Surface potential	V
Φ_{T}	Band barrier height of the traps in the dielectric	V
$g_{\text{A,D}}$	Degeneracy factor for acceptors or donors	-
g_{m}	Transconductance	$\Omega^{-1}\,\text{cm}^{-2}$
I_{D}	Drain current density	A/cm^2
I_{D_corr}	Drain current density corrected for serial resistance	A/cm^2
I_{e}	Electron current density	A/cm^2
I_{FN}	Fowler-Nordheim current density	A/cm^2
I_{G}	Gate current density	A/cm^2
I_{PF}	Pool-Frenkel current density	A/cm^2
λ	Thermal conductivity	W/mK
L_{ch}	Inversion channel length	µm
L_{T}	Transfer length	µm

m^*_{diel}	Effective electron mass in the dielectric	kg
μ_{b}	Bulk carrier mobility	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{c}	Carrier mobility term related to coulomb scattering	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{diel}	Electron mobility in the dielectric material	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{e}	Electron mobility	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{FE}	Field effect mobility	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{inv}	Inversion channel carrier mobility	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{sp}	Carrier mobility term related to surface phonon scattering	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{sr}	Carrier mobility term related to surface roughness	$\mathrm{cm}^2/\mathrm{Vs}$
μ_{tot}	Total inversion channel carrier mobility (modeled)	$\mathrm{cm}^2/\mathrm{Vs}$
N_{A}	Acceptor concentration	cm^{-3}
N^-_{A}	Concentration of active acceptors	cm^{-3}
N_{D}	Donor concentration	cm^{-3}
N^+_{D}	Concentration of active donors	cm^{-3}
n_{i}	Intrinsic carrier density	cm^{-3}
$N_{[\mathrm{Mg}]}$	Concentration of magnesium impurities	cm^{-3}
n_{N}	Number of dangling bonds per nitrogen atom	-
$N_{[\mathrm{Si}]}$	Concentration of silicon impurities	cm^{-3}
$N_{\mathrm{V,C}}$	Valence or conduction band effective density of states	cm^{-3}
p, n	Concentration of positive or negative carriers	cm^{-3}
P_{D}	Planar density of a crystal facet	atoms/$\mathring{A}^2$
q	Charge	C
Q_{G}	Gate charge density	$\mathrm{C/cm}^2$
Q_{it}	Interface charge density	$\mathrm{C/m}^2$
$q\Phi_{\mathrm{S,M}}$	Semiconductor or metal work function	eV
R_{ch}	Channel resistance	Ω
$R_{\mathrm{cont.}}$	Total contact resistance	Ω
$R_{\mathrm{cont.D}}$	Drain contact resistance	Ω
$R_{\mathrm{cont.Drift}}$	Drift layer resistance	Ω
$R_{\mathrm{cont.S}}$	Source contact resistance	Ω
R_{drift}	Drift layer resistance	Ω
$R_{\mathrm{DSon}}\,A$	Area specific on-resistance	$\mathrm{m}\Omega\,\mathrm{cm}^2$
R_{serial}	Sum of all MOSFET resistance components except for R_{ch}	Ω
R_{sh}	Sheet resistance	$\Omega_{\square}$
R_{source}	Feed resistance of the n^+-source layer	Ω
R_{spread}	Resistance contribution due tu current spreading	Ω
$R_{\mathrm{substr.}}$	Substrate resistance	Ω
R_{tot}	Total device resistance	Ω
ρ_{C}	Specific contact resistance	$\Omega\,\mathrm{cm}^2$
ρ_{ox}	Oxide charge density	cm^{-3}
$\rho_{\mathrm{substr.}}$	Substrate resistivity	$\Omega\,\mathrm{cm}$

T	Temperature	K
t_{drift}	Thickness of the drift layer	µm
t_{drift}	Thickness of the drift layer	µm
t_{inv}	Depth of the inversion channel	nm
$t_{\text{ox,diel}}$	Thickness of the oxide or dielectric layer	µm
t_{substr}	Thickness of the drift layer	µm
V_{B}	Breakdown voltage	V
V_{DS}	Drain-source voltage	V
V_{DSsat}	Drain-source saturation voltage	V
V_{FB}	Flat band voltage	V
V_{Gen}	Voltage output of the function generator	V
V_{GS}	Gate-source voltage	V
V_{max}	Maximum drain-source voltage for a specified dielectric field strength limit	V
V_{MOSFET}	Drain-source voltage drop across the MOSFET during the switching measurement	V
v_{sat}	Carrier saturation velocity	cm/s
V_{th}	threshold voltage	V
w_{cell}	Width of a transistor cell, also pitch size	µm
w_{ch}	Inversion channel width	µm
w_{depl}	Width of the depletion zone	cm
w_{trench}	Width of the trench	µm
χ	Electron affinity	V

Contents

1 Introduction

It is indisputable that climate change is one of the greatest challenges of the 21st century. The urgency for an essential change in the way humanity produces and consumes energy and resources has become strikingly clear in recent years. A more efficient and sustainable lifestyle is inevitable if demand for higher living standards has to be met in conjunction with a rapidly growing world population.

Today, the energy sector is responsible for three quarters of global CO_2 emissions as approximately 80 % of the energy is produced from fossil fuels [1]. Energy demand has increased by 40 % since the year 2000 and so have CO_2 emissions [2, 3]. During the same time span, electricity consumption nearly doubled [4, 5] with more than 60 % of it still originating from fossil fuels [6]. Electricity is predestined to be generated from renewable sources and a shift towards a sustainable concept is unarguably the most important step to meet the continuously rising demand. If electricity is generated from hydro-, wind and solar energy, the increasing degree of electrification can be advantageous and might even be necessary. Especially the transportation sector can benefit from such a development. Driven by legislation and advances in battery technology, the market for e-mobility and electric transportation in general, has been growing rapidly in the last years and will continue to do so. Today's number of approximately eight million electric vehicles is believed to increase to 140-240 million by 2030 [7]. However, a higher degree of electrification requires increased efficiency in power storage, distribution and conversion. Electric vehicles in particular, have special demands for power conversion units as conversion must be bidirectional between DC and AC, and between multiple voltage levels such as grid, battery, motor and miscellaneous devices. In addition, it must be compact and highly efficient since on-board energy storage is limited and expensive.

Since 1950, semiconductor devices based on silicon are used for power conversion [8]. Originally, the bipolar transistor was the device of choice but from 1970 on, the metal oxide semiconductor field effect transistor (MOSFET) was adopted and its transformation to the vertical double diffused metal oxide semiconductor field effect transistor (VD-MOSFET) and the trench MOSFET [9] marked the advent of vertical power devices. Today, the insulated gate bipolar transistor (IGBT), a hybrid of MOSFET and bipolar transistor, is a common power switch for medium and high voltage applications (>600 V) and is found in most electric vehicles. Eventually, requirements regarding efficiency, switching speed and module size, revealed the IGBT's limits [10] and those of the silicon technology in general. As a semiconductor, silicon offers a variety of advantages, including low cost, good processability and extensive understanding of the material in

general. It is therefore unchallenged in many fields of application for example solar cells and low power or logic switches. However, silicon is not the ideal candidate for power devices. So-called wide band gap (WBG) semiconductors such as gallium nitride (GaN) or silicon carbide (SiC) are much better suited for this task. Transistors based on these materials achieve a more favorable trade-off relationship between conduction losses and blocking voltage, which makes them especially useful for application at higher voltages, that is 600 V and above. Compared to the IGBT, they can operate at higher frequencies, which allows the power conversion system to be more compact. These benefits make them very attractive for use in the mobility sector and put them in direct competition to far more matured silicon devices, the IGBT chief among them. As of today, silicon carbide and gallium nitride are by far the most relevant representatives of wide band gap semiconductors. While silicon carbide based power MOSFET solutions up to kilovolt operating voltage are already available, gallium nitride is so far only represented in the low to medium voltage regime up to 600 V. The most common gallium nitride device type is the high electron mobility transistor (HEMT), with telecommunication, high-end radar and low voltage power supply units as focus applications.

An often demanded requirement for power switches is fail-safe operation. This means the default state of a voltage source inverter switch must be open in order to prevent short circuiting. Such behavior must either be achieved by external circuiting, or is inherent to the device type itself, as in the case of the MOSFET and the IGBT. The metal oxide semiconductor (MOS) concept can be adopted for wide band gap materials and is today the common approach for power devices. Intense research is on-going and various types of silicon carbide and gallium nitride based power devices have been demonstrated so far. Although the silicon IGBT still dominates the power conversion market between 600 and 3000 V, wide band gap semiconductors rise in significance and will be the favorable solutions for next generation power applications.

1.1 State of the art and related work

The concept of the MOSFET dates back to the 1920s when Julius Edgar Lilienfeld discovered the principle of the field effect. The first silicon-based MOSFET was demonstrated in 1960 by Kahng [11] and since then the MOSFET has come a long way and has been improved considerably.

Today, MOSFETs are used in a wide range of applications, from high voltage devices for power conversion to low voltage logic switches. Complementary MOS-technology (CMOS), where n- and p-type devices are combined in one circuit, are essential in CPUs and memory and the quasi loss less static operation of the MOSFET makes it an ideal candidate in this field of application. Its inherently normally-off behavior makes the MOSFET also suitable for power conversion devices. Furthermore, as a unipolar device, the MOSFET is capable of low-loss, high-frequency switching. The main difference

between a logic switch and a power switch is the requirement of the latter, to block a considerably higher voltage and carry more current. To cope with this demand, the IGBT was developed in 1979 [12] and is today widely used as power semiconductor device. Together with the 1974 developed trench MOSFET [9], the IGBT marks the advent of the vertical architecture. Compared to a planar design, the vertical one allows a scaling of operating voltage that is nearly independent from chip size and is today the standard approach for most power devices. Although the IGBT has relatively low conduction losses and can operate at high voltages, since it is a bipolar device, high frequencies lead to considerable switching losses, more than ten times higher than for a MOSFET [13], depending on the operation frequency and the actual voltage rating of the device. Other device concepts, such as the super junction MOSFET, which is based on the reduced surface field (RESURF) concept [14], have been developed to improve efficiency and competitiveness of silicon-based power devices. The logarithmic plot in figure 1.1 shows the area specific on-resistance of various silicon, SiC and GaN based devices as function of the breakdown voltage. Also depicted is the unipolar limit, defined as the trade-off relationship between the specific drift layer resistance and the breakdown voltage. The plot shows that the mentioned super junction device type achieves a lower on-resistance at a given breakdown voltage than devices with conventional junctions. Especially the IGBT, apart from the mentioned switching losses, shows excellent performance in high voltage applications.

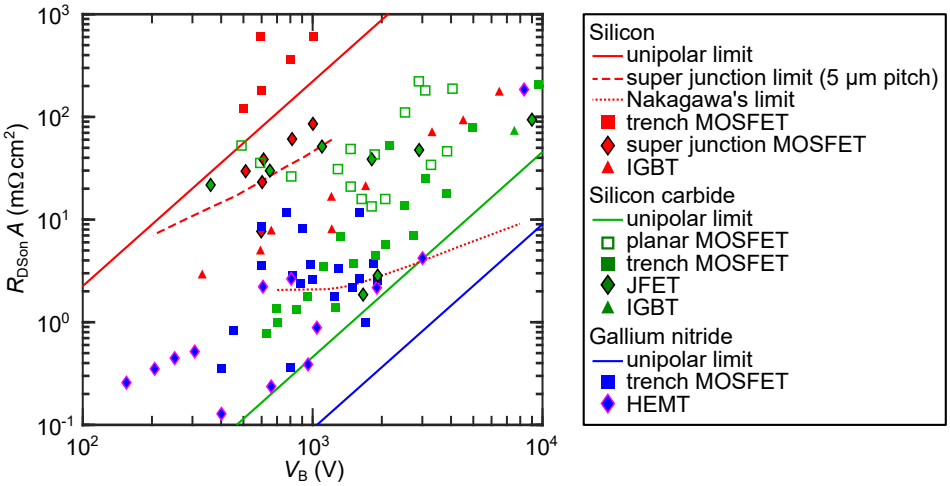

Figure 1.1: On-resistance vs blocking voltage of real devices in the context of the unipolar limits for silicon (red), SiC (green) and GaN (blue). Data from [15–31].

Silicon is by far the most prominent semiconductor and sound understanding of this material enables the fabrication of complex device concepts, without jeopardizing reliability and cost requirements. Therefore, silicon is still the material of choice for many applications despite the theoretical advantages of WBG materials. The main requirement for a power switch is low conduction loss in the on-state along with the capability to block high voltages in the off-state. Wide band gap semiconductors satisfy this requirement to

a greater degree than silicon. This can be seen from the plot in figure 1.1. The theoretical limits of these materials imply a much better performance compared to silicon devices and apart from the IGBT, there is no competition in the medium to high voltage regime. Apart from the on-state conduction loss, other capabilities such as thermal robustness and switching speed are relevant as well. Several important material parameters such as critical electric field strength E_{crit}, thermal conductivity λ or electron mobility μ_{e}, are presented in figure 1.2 a) for SiC, GaN and silicon. The comparison illustrates the advantage of WBG materials in various fields, which is the reason for their increasing adoption for power devices. Figure 1.2 b) illustrates the market share of SiC and GaN in comparison to silicon. Although the theoretical advantage of the WBG materials over silicon is significant, cost-related factors, material quality and a lack of sound understanding regarding processing technology and interface engineering are reasons why silicon still dominates the market. However, a clear trend is observable and the significance of WBG devices will increase in the near future.

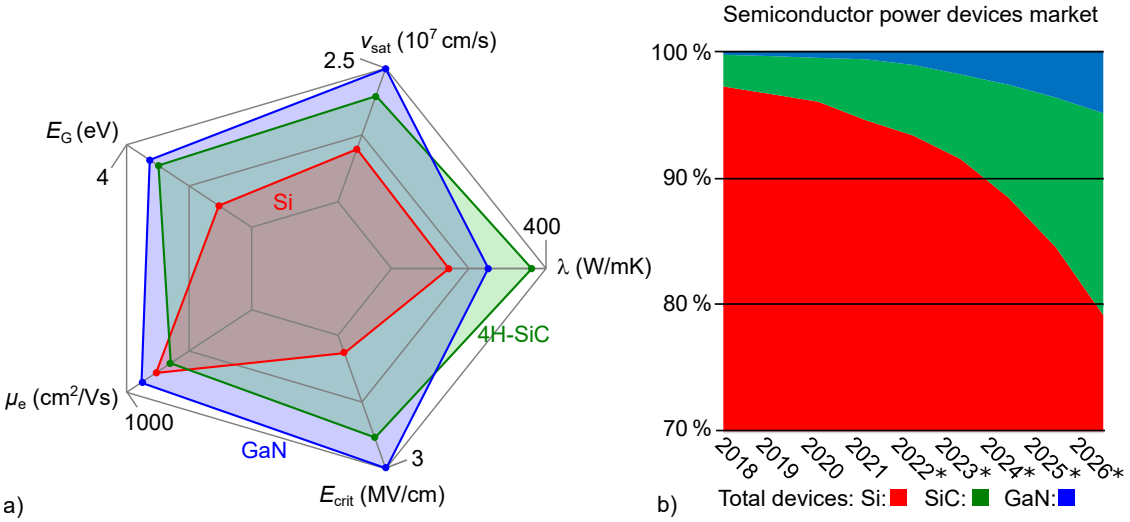

Figure 1.2: a) Crucial material parameters for silicon, SiC and GaN. All values correspond to a temperature of 300 K. The critical field strength refers to a doping concentration of $10^{16}\,\mathrm{cm}^{-3}$, the electron mobility to $10^{17}\,\mathrm{cm}^{-3}$. Both concentrations are typical for drift- and p-base layer, respectively, where the corresponding parameter is relevant. Source: [8]. b) Percentage market share of SiC and GaN devices compared to silicon. Years beyond 2021 show forecast values. Source: [32]

Various device concepts have been demonstrated for SiC and GaN including lateral and vertical architectures. The most common GaN device is the lateral HEMT, which based on a channel of two dimensional electron gas (2DEG), allows high frequency switching and low switching losses. The HEMT is a normally-on device and although methods have been developed to achieve normally-off behavior, in most cases threshold voltages are still too low for power applications [33, 34]. The lateral device architecture limits the contact area and thus the current that can be fed into the device. Furthermore, it restricts the HEMT mostly to the low to medium voltage regime, i.e. up to 600 V [35, 36]. Although

higher rated devices exist [37, 38], large safety margins and questionable reliability make them usually unattractive. Vertical alternatives to the lateral HEMT are the vertical HEMT [39] or the current aperture vertical electron transistor (CAVET) [40, 41]. Both are based on a 2DEG channel but are not commercialized so far. A commercialized SiC power device is the VD-MOSFET, today the most common WBG power switch and a direct competitor to the silicon IGBT. Note that the term VD-MOSFET is adopted from the corresponding silicon device. Due to low impurity diffusion in SiC and GaN, ion implantation is typically used. Gallium nitride VD-MOSFETs have been demonstrated as well [42, 43] but are yet to be commercialized. An evolution of the VD-MOSFET is the trench MOSFET, which further reduces device size. The trench MOSFET was originally developed on silicon as logic switch in integrated circuits [9]. Today the structure is widely adopted and transferred to SiC, GaN and other materials. The plot in figure 1.1 shows real devices of various types and from different materials in the context of their unipolar limit. In the case of silicon, the theoretical limit for super junction MOSFETs [31] and the limit for IGBTs proposed by Nakagawa [44], are displayed as well.

This work concerns the GaN trench MOSFET and the state of research for this device concept will be discussed in more detail. In 2007, Otake et al. [45] demonstrated the first GaN trench MOSFET. In 2014 [25] they presented a device with 1.2 kV blocking capability and 1.8 $\mathrm{m\Omega\,cm^2}$ specific on-resistance. Recent work on the GaN trench MOSFET was done by multiple groups, e.g. [46–48, 30, 49, 50] including devices fabricated on foreign substrates [51, 52]. In the following passage, the basic fabrication procedure and corresponding challenges are described along with references and notes regarding the current state of research.

The first step in device manufacturing is typically the fabrication of differently doped layers and regions in the semiconductor. To create n-type doped GaN, silicon atoms are incorporated during the epitaxial growth or via ion implantation. The low activation energy of the silicon donors, only about 20 meV, makes n-type doping relatively easy and a wide range of doping concentrations (10^{17}-$2{\cdot}10^{19}\,\mathrm{cm^{-3}}$) was achieved [53]. On the other hand, p-type doping is still not fully understood [54, 55] and mainly problematic due to the high ionization energy of approximately 220 meV for the magnesium acceptors. Regarding the fabrication process of the GaN trench MOSFET, the common way to etch the trench is chlorine based plasma etching [56–59]. However, work concerning photo assisted wet etching of GaN trenches has been published [60, 61]. Chlorine free plasma etching of GaN trenches has so far not been demonstrated successfully, although rudimentary approaches were presented [62]. The plasma etched trench is usually subjected to a post treatment in alkaline solution to optimize the geometry and interface [63–65, 26]. An interesting but so far open question concerns the orientation of the trenches along the two nonpolar vertical GaN crystal planes and the resulting effect on the carrier in the MOS inversion channel. Concerning the gate structure, published work is mostly limited to two types of gate dielectric namely atomic layer deposited aluminum oxide [42, 46, 48, 27] and silicon dioxide [25, 52] or a material stack of both [66]. The gate contact is based on

a variety of metals including but not limited to nickel [42], aluminum [25], chrome and gold [52] or titanium and gold [27].

Although the adaption of GaN in the market for power devices is behind that of SiC, better carrier mobility and the higher critical field strength, make it more attractive and devices fabricated from it, potentially smaller and more efficient. In addition, the lower growth temperature for GaN substrates compared to that for SiC and especially the option to grow epitaxial layers of GaN on low cost substrates for example silicon [67, 68], will reduce material cost in the future. Lastly, further development will benefit from synergy effects with the large LED and RF industry.

1.2 Motivation and research objective

Advances in the growth technology improved GaN crystal quality [67, 68], reduced bulk defect density and thus allowed the fabrication of vertical devices. Although device types such as the power FinFET [69] or the vertical HEMT [39] promise outstanding efficiency and switching speed, the fabrication process is complicated and concerns regarding normally-on behavior have yet to be dispelled. The VD- and trench MOSFET on the other hand, are inherently normally-off and can be fabricated without epitaxial regrowth, buried layers or the need for elaborated p-GaN gates on 2DEG channels. A close resemblance to their silicon based counterparts make the GaN VD- and trench MOSFETs the most promising candidates for the first generation of commercialized vertical GaN power devices.

Concerning GaN devices and the GaN MOSFETs in particular, there are three major fields of research that need to be advanced in order to make them competitive with SiC power switches and to successfully introduce them into the market. The first one is the growth of GaN substrates and epitaxial layers. The main objectives are reduced defect density, reduced cost and increased substrate size. While the latter two can be addressed by the introduction of a foreign substrate, this compromise usually degrades the quality of the epitaxial GaN layer [70]. Solutions such as special substrates or super lattice buffer layers exist but are, as of today, not matured. The second relevant aspect is p-type doping. As mentioned before, especially the doping procedure via ion implantation is still problematic [55]. Kachi et al. [71] presented a promising approach for improved activation of acceptors in p-type GaN and fully ion implanted devices have been demonstrated [42], but further work is required to better understand impurity incorporation and activation. Especially the passivation of the magnesium acceptors by hydrogen during epitaxial growth or subsequent processing steps is of great importance [72] for controllable process conditions and temperature related device stability. Partially related to p-type doping and therefore included in this point, is the matter of p-type contacts. The large work function of p-type GaN of $\approx 7.3\,\mathrm{eV}$ [73] requires metals with similarly large work functions. The resistance of p-type contacts based on gold (5.5 eV), platinum (5.6 eV) or

nickel (5.2 eV) is, however, still orders of magnitude larger than for contacts on n-type GaN [74]. The last aspect is the channel interface. This concerns the understanding of the GaN interface in general and the MOS interface in particular. Understanding and controllability of interface charges and defects is vital for the reproducible fabrication of reliable and efficient MOSFETs. This is especially true for the vertical MOS interface of trench devices. Even for silicon, the transfer of the planar MOS interface to a trench sidewall proved to be challenging [75]. To adequately evaluate the MOS interface, surrounding components must be considered as well. This includes the GaN surface and the gate dielectric but must also take the gate electrode into account.

As laid out in section 1.1, state of the art fabrication procedures for the gate structure are limited to metal containing dielectrics and or metal gate electrodes. Furthermore, dielectrics are deposited via low temperature procedures, which yield layers of lower quality compared to ones which are fabricated by high temperature processes. This work examines the potential benefits of a completely metal-free gate structure for planar and trench MOSFETs in combination with high temperature, high quality silicon dioxide as dielectric layer. The gate electrode is based on heavily doped n-type polycrystalline silicon (poly Si) as substitute for the typically used metal electrodes. Compared to the state-of-the-art gate-last approach, where metal electrodes are formed prior to the actual gate fabrication, a gate-first approach is used in this work. Any metal related fabrication steps are performed during back-end processing and are separated from the front-end steps, including the gate fabrication, by a complete device passivation. Using MOS capacitors as test modules, an in-depth comparison of various gate dielectrics was conducted in combination with an evaluation of metal containing and metal-free gate electrodes. The outcome was used as a foundation, on which lateral and trench MOSFETs were fabricated and characterized.

The trench structure is fabricated with a chlorine-free GaN trench etching process based on sulfur hexafluoride and comparability with chlorine etched trenches is demonstrated. This includes detailed examination of GaN crystal planes at the trench sidewall and their behavior during chemical wet etching procedures. In this context, plasma induced damage and the effect of post treatment in alkaline solution is assessed.

Various fabrication procedures were used during the manufacturing of the GaN MOSFETs and test modules. Etching procedures were performed as inductively coupled plasma (ICP) etching, as wet etching or as gas phase etching. Deposition methods include different types of chemical vapor deposition, atomic layer deposition and sputter deposition. Any lithography was performed via contact method and structure dimensions were limited to a minimum of 1 µm. Physical characterization of the samples was conducted via light-, electron- and atomic force microscopy, ellipsometry and energy dispersive X-ray spectroscopy. Electrical characterization included current voltage and capacitance voltage measurements and standard transistor characterization methods.

Using the described methodology in the examination of the fabricated transistors and test modules, the chlorine-free etching method was found to be a viable alternative to the state of the art procedure. The MOS gate with poly Si showed superior robustness to comparable, metal containing structures. The trench MOSFETs with metal-free poly Si gate and high temperature silicon oxide gate dielectric showed competitive performance. To assess interface state densities and channel carrier mobility, technology computer-aided design (TCAD) simulations were carried out. The obtained model suggest indeed a high density of interface defects and charges, and in accordance with these findings, device threshold voltage was relatively low. A defectious interface is also likely to be the reason why no significant distinction was found for trenches oriented along the different GaN crystal planes.

1.3 Structure and content of this work

This section provides an overview of the content in this work and motivates the order in which it is presented. Following the introduction, the fundamentals chapter treats several topics related to device fabrication in general and gallium nitride in particular. The chapter is structured along the various components of the trench MOSFET and the corresponding fabrication methods with the MOS inversion channel in the focus. The subsequent chapters concern experimental procedures and the corresponding results. The results from the trench fabrication experiments, discussed in chapter 3, and the results from the MOS-interface developments, presented in chapter 4, build the foundation for the actual trench and lateral MOSFETs, treated in chapter 5.

Chapter 3 concerns the trench development and comprises plasma and wet etching fabrication methods for the creation and the refinement of trenches that fulfill the requirements for an application in a trench MOSFET. Apart from GaN plasma etching, the wet etching procedure is discussed in the context of the GaN crystal and its various crystal planes. Chapter 4 contains a description of the fabrication procedure for planar and trench MOS capacitors and focuses on the evaluation of different candidates for the gate dielectric. The trench version of these devices relies on the results provided in chapter 3. A second point that is discussed, is the gate electrode and the metal-free solution based on poly Si. Different versions of the MOS capacitor are electrically characterized to identify the most promising configuration, which is then adopted for the MOSFETs in chapter 5. The final section of this chapter concerns plasma-induced damage at the GaN surface and its impact on the electrical performance of MOS capacitors. Chapter 5 comprises the main part of this work. Based on the outcome of the two preceding chapters, it describes the fabrication and characterization of GaN trench MOSFETs. The characterization includes various aspects such as transfer- and output characteristic, as well as threshold voltage shift, field effect mobility, area specific on-resistance and switching characteristics. Furthermore, the chapter contains a discussion of lateral MOSFETs that act as reference

devices, to put the quality and performance of the vertical MOS channel of the trench device into perspective, by comparing it with a lateral channel. Chapter 6 describes a device simulation model, which focuses on the MOS inversion channel carrier mobility. After a matching with literature data for impurity ionization and bulk carrier mobility, the mobility model for the MOS inversion channel was calibrated with the experimental results of chapter 5. Also included are simulations concerning the field shielding of the gate dielectric during the off-state. Since no such structures were fabricated in the experimental part of this work, the simulations were carried out to act as guidelines and basis for future work on such structures. The summary and outlook in chapter 7 conclude this work and provide an overview of the outcome and the respective relevance in the context of the current state of research. A reflection on the research objective is followed by the limitations of this work and a set of points that need to be addressed in future work.

2 Fundamentals

This chapter provides basic information about the topics treated in this work. After a description of different power device types, the trench MOSFET and its various aspects are analyzed in detail. This includes an overview of GaN as semiconductor material, design and requirements for different components of the trench MOSFET as well as doping and etching of GaN. The center part of the chapter concerns the function principle of a MOSFET and the MOS inversion channel in particular. In this context, electrical properties, carrier mobility and characterization methods are discussed.

2.1 Types of GaN power devices and their fields of application

Today, electrical power is essential in almost every sector of our society. From gigawatts of power plant output to single digit watt audio electronics, from line frequency to gigahertz, a wide range must be covered. This task is achieved by taking advantage of the strengths of a large variety of different semiconductor power switches. The diagram in figure 2.1 shows the field of operation for some common power switches and semiconductor materials in terms of power and operating frequency. Wide band gap semiconductors such as SiC and GaN built the frontier in the direction of high power and high frequency applications. Despite its maturity and highly elaborated device designs, silicon starts to fall behind in these areas.

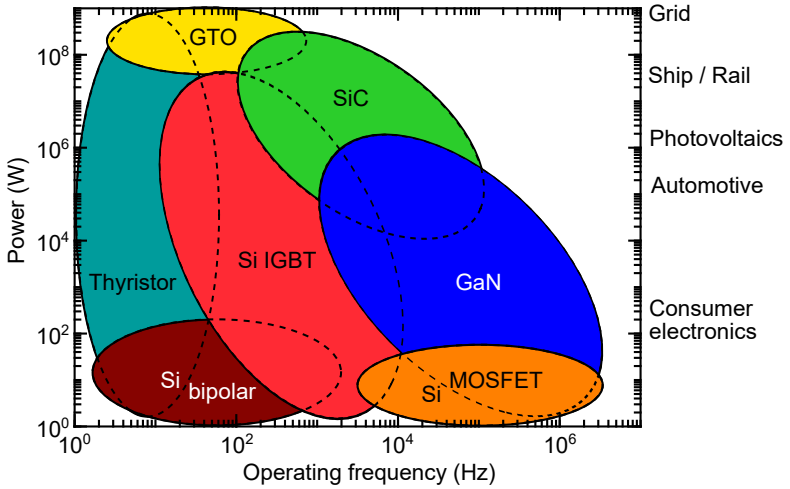

Figure 2.1: Various types of power switches and semiconductor materials categorized into application fields rated by power and operation frequency.

Depending on the area of operation, the requirements for a power conversion device are highly specific and it is beyond the scope of this work to give a thorough description. On the level of the discrete switch there are three basic requirements.

- The ability to withstand voltage in the off-state: This means the device must neither break down, nor allow a significant leakage current.
- The ability to be highly conductive: This is relevant in the on-state to minimize dissipation, which would lead to loss in efficiency and heating of the switch.
- Fast switching: Meaning a quick and clean transition between on- and off-state in order to minimize transition losses and to allow high switching frequencies in the first place.

While the first two requirements seem quite obvious albeit not easily achievable, the last point might need a more detailed description. The graph in figure 2.2 illustrates, in a simplified way, the current, the voltage drop and the power loss during a switching cycle for inductive load. The leakage current in the off-state is typically low and the related power dissipation can be neglected. The on-state power loss is determined by the voltage drop across the switch. Depending on the application and especially in the low and medium frequency range, the on-state power dissipation is the predominant cause for heat generation and efficiency loss. The power loss during transition is generally higher since both, current and voltage are elevated. This requires, especially for high frequency switches, for these transition phases to be as short as possible. Yet another loss contribution is due to charging and discharging of the gate capacitance. However, this is only relevant for high frequency devices with low power output. The described operation mode, where the transition between on- and off-state is done under full power load, is called hard switching. This is the designated operation mode for the devices developed in this work.

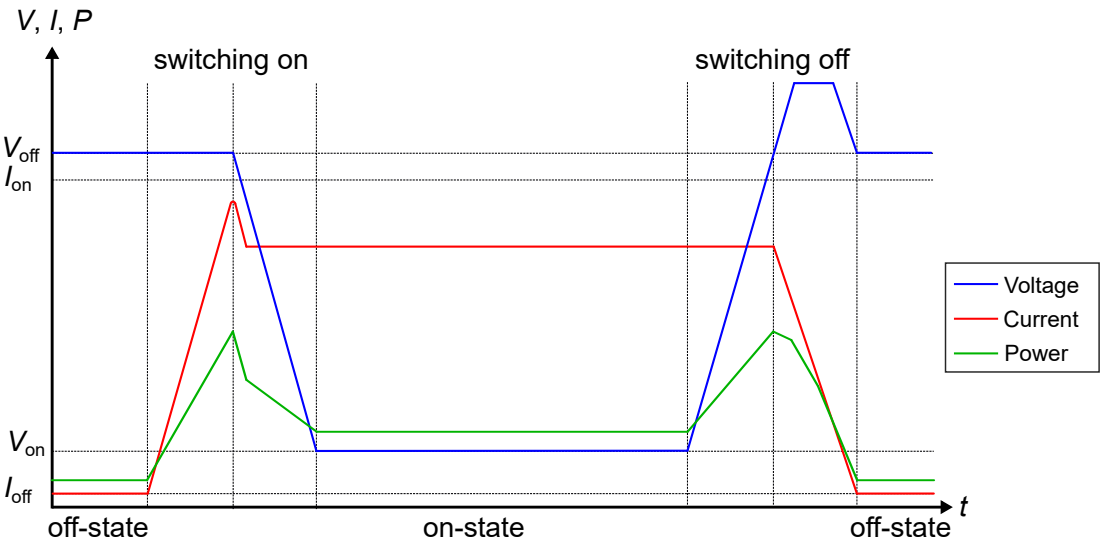

Figure 2.2: Simplified illustration of power loss during on and off-state as well as during the transition between those states. Adapted from [76].

To address the requirements for power switches, numerous different device types have been developed. A brief introduction will be given for a representative selection of power switches, with the aim to motivate the decision to focus on the trench MOSFET in this work. Figure 2.3 shows schematics of various power device types. Note that some of the devices displayed, namely the HEMT or CAVET, are exclusively fabricated from GaN (or other compound semiconductors for example gallium arsenide, which are not relevant in the context of power applications). Other examples such as FinFET or MOSFET are not unique to one material and can also be fabricated from silicon or SiC. It should also be mentioned that the IGBT, and bipolar structures in general, are typically not made from GaN. Since GaN is a direct semiconductor, carrier lifetimes are very short, which in turn leads to low gain factors in bipolar devices.

Apart from performance specifications such as operation voltage limit or on-resistance, the most important characteristic, directly linked to the device design, is its threshold voltage V_{th}. Or more precisely, whether the device is normally-on or normally-off. For safety reasons, power switches are typically required to be normally-off in order to prevent short circuiting in the case of a gate driver failure. Depending on the application, the desired threshold voltage is in the range of 3 V.

A categorization of the various device types can be made on a physical level based on the channel type. Very low channel resistance and fast response is obtained by using a 2DEG channel in a HEMT. However, the 2DEG originates between an intrinsic GaN layer and an AlGaN layer due to material related polarization and not due to gate bias, which makes this channel a normally-on type. Moreover, good conductivity is obtained from an accumulation channel. The most promising device type that features an accumulation channel is the power FinFET. Depending on the fin width and interface charge density, normally-off behavior can be achieved but is not inherent to this channel type. The most common channel type is the MOS inversion channel. It is by default normally-off and can reach a relatively high carrier density. However, its extension is limited to a few nanometers and the proximity to the MOS interface in combination with a significant field strength orthogonal to the carrier flow direction, usually causes poor carrier mobility. This is especially true for novel semiconductor materials where the MOS interface is not as well understood as in the case of silicon [77].

A second way to classify device types is their architecture, which is divided into lateral and vertical (cf. fig. 2.3). Lateral devices have all contacts on the top side of the chip. The current flows in lateral direction and usually close to the surface. Trenching or even deep etching of the semiconductor is not necessary for the planar topology. However, along with the current, high field strength is also located predominantly at or near the surface, which can be problematic regarding breakdown and reliability. To achieve a high blocking voltage, the distance between source and drain, or rather gate and drain, must be large, so that the voltage drop can take place over a sufficiently long distance and the field strength remains low. This makes the device larger in general and thus more

expensive. Larger dimensions also increase parasitic effects, which affect efficiency and switching performance. Vertical architecture on the other hand, allows scaling of the operating voltage by increasing the device thickness. The current flows from the front side through the device to the back side. The by far largest part of the voltage drop occurs in the so called drift region inside the semiconductor. By increasing the thickness of this layer, the operation voltage can be increased as well. The distance between the front side contacts can be as small as fabrication tolerances and capacitance limits allow. This increases current density and reduces resistance as pitch size is minimized. The pitch size specifies the distance between two identical features in the repetitive structure of transistor cells connected in parallel. Furthermore, the current flow through the device is found to be more favorable regarding heat spreading and thermal control, which reduces the demand for cooling compared to lateral devices [78]. A further distinction of vertical devices is made with respect to their gate structure. Devices such as the VD-MOSFET have a planar gate structure with a laterally oriented channel. This makes the fabrication easier, since no deep etching in the semiconductor is required. It also allows to use the planar interface for the channel, which is easier to prepare and control than a trench side wall. The drawback is a larger pitch and the fact that the current, exiting the channel in lateral direction, must be guided in vertical direction through a restricting aperture. This is illustrated in figure 2.3 for the VD-MOSFET and the CAVET. The alternative to a gate on the surface is a gate on a sidewall. Again depicted in figure 2.3 for the vertical HEMT or the trench MOSFET. By etching a trench or V-groove in the semiconductor, the interface, and thus, the channel is already oriented in vertical direction. Although the gain in lateral spacing is not resolved in figure 2.3, the gate on sidewall approach allows significantly smaller pitch sizes ($\approx 50\,\%$). The vertical channel is also preferable regarding current spreading. To achieve the lowest drift layer resistance possible, the current must spread as fast and wide as possible at the transition between drift layer and channel. The disadvantages compared with the planar gate approach is a more elaborated processing due to the necessity of deep etching in the semiconductor and the fact that this etching creates a less favorable interface. Determined by the crystal itself and by damage and irregularities caused during the etching process, the interface quality and thus the carrier mobility in the channel, is typically lower than for a lateral oriented channel located at the surface.

The focus of this work is the GaN trench MOSFET due to several reasons. Firstly, it is a normally-off device and the trench MOSFET concept is well adopted in the power device market. Secondly, it can be fabricated on epitaxy only and implanted regions are not mandatory. This is advantageous since especially p-type doping is still challenging for GaN [54, 55]. Lastly, it is a promising intermediate design between simpler configurations such as the lateral or vertical diffused MOSFET and elaborated ones for example the FinFET and V-HEMT. Processes that need to be developed for the trench MOSFET, such as trench etching, interface treatment and gate dielectric properties, can be reused for more advanced designs.

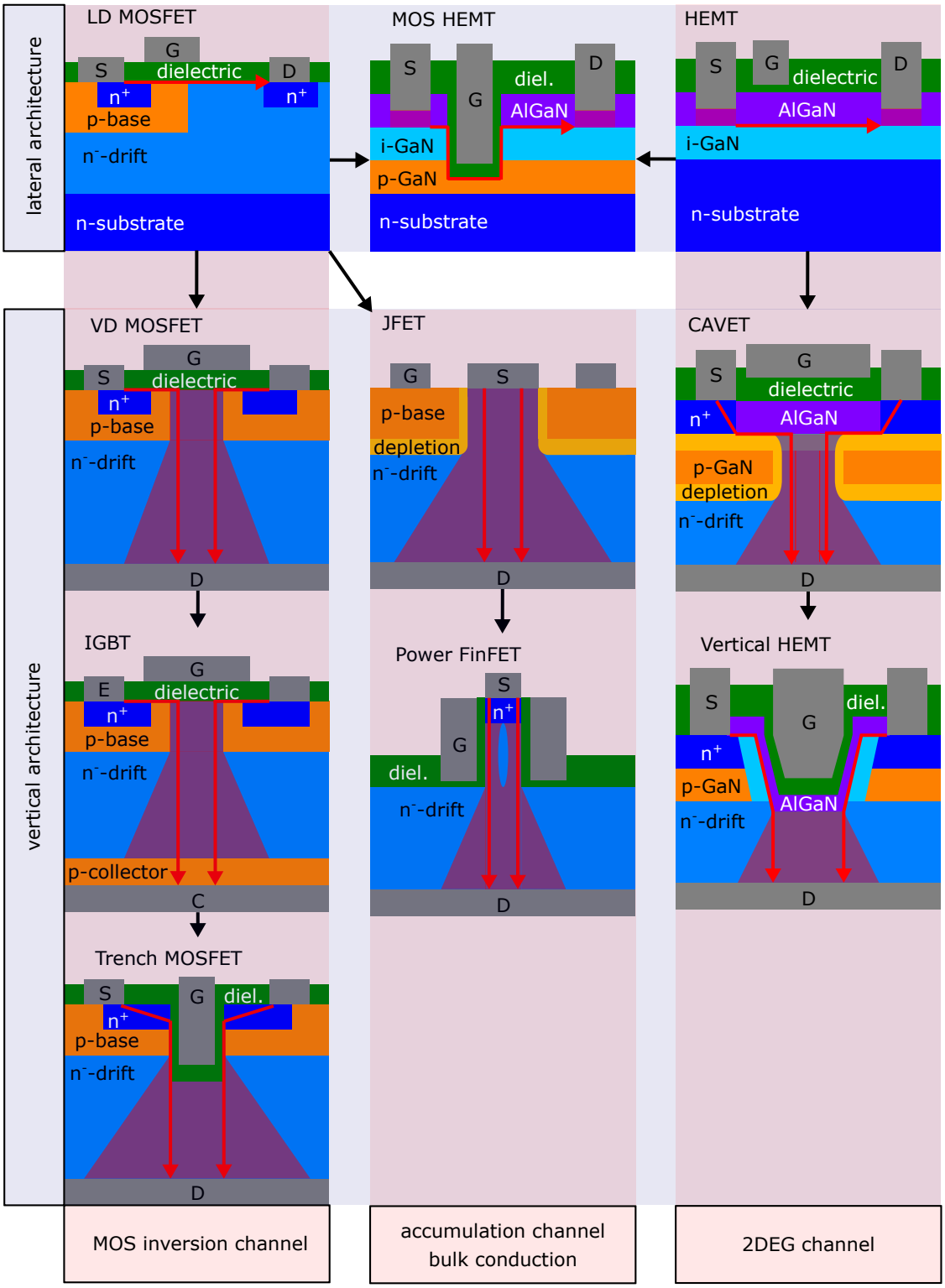

Figure 2.3: Schematic depiction of various power transistor types. Red arrows represent the electron flow while the dark shaded area symbolizes the spreading of the carriers at the exit of a channel or aperture. Black arrows between the devices indicate a transition to more elaborated devices with potentially higher performance. Note that due to specific application requirements a direct comparison between the various branches is not reasonable. Only essential parts are depicted, auxiliary regions such as substrate or passivation have been omitted in some cases.

2.2 Structure and design of a trench MOSFET

This section provides an introduction to the GaN trench MOSFET, its various components and how they should be designed in order to cope with the operation voltage and on-resistance requirements. This on-resistance is directly proportional to the area of the chip, therefore the on-state drain to source resistance is usually stated as the area specific measure $R_{\mathrm{DSon}}A$. Further distinctions can be made depending on whether the respective area refers to the active area i.e sum of cells times pitch and cell length or to the chip area, where contact pads and edge termination structures are included. Since the latter is highly design dependent, it is not relevant for devices in the early state of development. In this work the $R_{\mathrm{DSon}}A$ will always be calculated by using the active area.

Figure 2.4 a) shows the schematic of a MOSFET with the various resistance components. The plot in b) illustrates the impact on the said components on the total resistance with the drift layer resistance as function of the doping concentration. A description of the components is provided in the following paragraphs, together with a statement regarding their impact on the overall on-resistance, as displayed in figure 2.4 b) and a reference to the section in which they are discussed in detail.

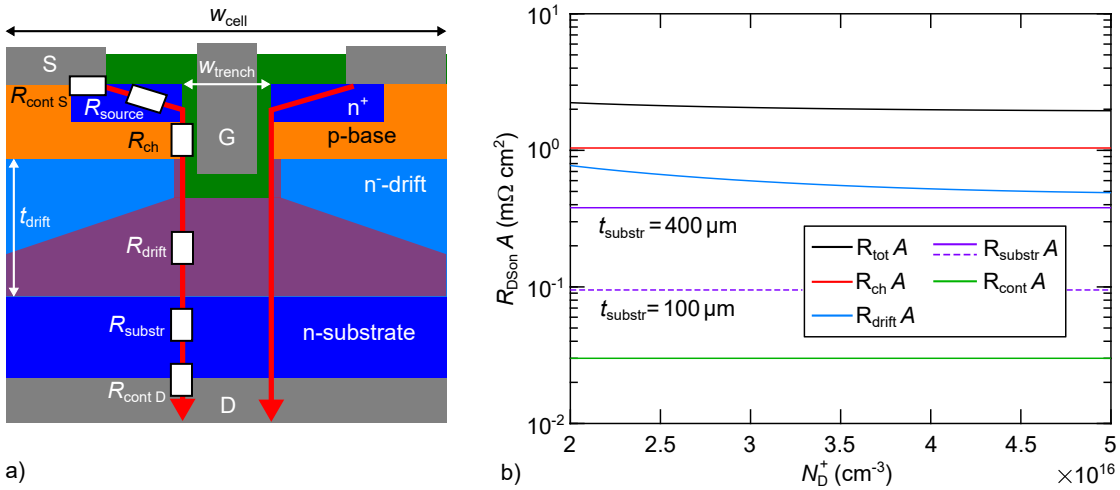

Figure 2.4: a)Schematic depiction of a trench MOSFET cell with the electron path indicated by red arrows as well as the various resistance components on that path. b) Relevant contributions to the overall device resistance over a typical range of drift layer doping concentrations. Note that source and drain contact resistance are combined in R_{cont} and that the total resistance is calculated for the case of a 400 µm thick substrate.

Substrate: Concerning GaN devices, there are two types of substrates. The first type comprises foreign substrates such as silicon, sapphire, SiC etc. The second refers to native substrates, that is bulk GaN. In this work, devices were fabricated on the latter and section 2.3 provides information regarding the growth procedure, the GaN crystal structure and relevant material parameters. The bulk GaN wafers used in this work are 300-400 µm thick and n-type doped. Despite a low resistivity of $\rho_{\mathrm{substr}} \approx 0.01\,\Omega\,\mathrm{cm}$,

achieved by a relatively high doping concentration of $10^{18}\,\mathrm{cm}^{-3}$ and more, the thickness of the substrate makes its contribution to the overall resistance relevant. Assuming a homogeneous current density, the substrate related resistance is given by

$$R_{\mathrm{substr}} A = \rho_{\mathrm{substr}} t_{\mathrm{substr}}, \tag{2.1}$$

with the substrate thickness t_{substr}.

For optimization reasons, it can be required to reduce the substrate thickness by regrinding the wafer during back-end processing. However, this is not done for the research devices in this work as the substrate contribution to the on-resistance can easily be accounted for and the results can be corrected accordingly.

Drift region and p-base layer: During the off-state, the largest voltage drop occurs in the drift region and this layer makes a major contribution to the on-resistance. The assumption of a homogeneous current density, used for the substrate, is not valid for the drift region, which is implied by the triangular shape of the current spreading area in figure 2.4 a). When the electrons exit the MOS channel, they need to spread out as they travel through the drift layer. By assuming a spreading angle of 45° [8], the drift layer resistance in the on-state can be calculated as

$$R_{\mathrm{drift}} A = \rho_{\mathrm{drift}} \left[\frac{w_{\mathrm{cell}}}{2} \ln\left(\frac{w_{\mathrm{cell}}}{2 w_{\mathrm{trench}}} \right) + t_{\mathrm{drift}} - \frac{w_{\mathrm{cell}}}{2} + \frac{w_{\mathrm{trech}}}{2} \right], \tag{2.2}$$

where w_{cell} and w_{trench} are the cell and trench width in accordance with figure 2.4 a).

A design specific transition region between channel exit and drift layer, denoted as JFET- or spreading region, can improve the current spreading and reduce the resistance. However, this component is mostly relevant for shielded devices and is not implemented for structures fabricated in this work.

The p-base layer represents the counterpart to the drift layer and must be balanced with it. Thickness and doping concentration of this layer have a direct impact on the MOS channel length and the device threshold voltage. Section 2.4 concerns the dimensioning of these layers and provides an introduction to doping and impurity ionization in GaN. Also included is a modeling approach concerning the doping related carrier bulk mobility.

Gate trench and dielectric: The gate structure is more elaborated for a trench MOSFET than for lateral devices or the VD-MOSFET. Before the actual gate can be fabricated, a trench must be etched into the semiconductor and the geometry, as well as the interface, need to be refined. Trench depth and width affect channel length and pitch size, respectively. The later corresponds to w_{cell} in figure 2.4 a) and is directly proportional to the MOS channel resistance given by equation (2.3). This implies that a narrow trench and a

small pitch size are desirable. Also affected by the trench shape and the surface quality, are the field strength in the dielectric and the carrier mobility in the MOS inversion channel. Information concerning dry and wet etching of GaN, the techniques used for the trench fabrication, is given in section 2.5. A more specific description of the actual trench fabrication and refinement is provided in the experimental chapter 3.

The MOS inversion channel: This is the key feature of the MOSFET and the focus of this work. Next to the drift layer, the MOS channel is the predominant factor regarding device resistance and its contribution is given in [8] as

$$R_{\mathrm{ch}}A = \frac{L_{\mathrm{ch}}w_{\mathrm{cell}}}{2\mu_{\mathrm{inv}}C^{*}_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{th}})} \tag{2.3}$$

where μ_{inv} is the inversion channel carrier mobility and L_{ch} is the channel length.

The function principle of a MOSFET and the fundamentals of a MOS channel, along with its electrical properties and the characterization of MOS structures in general, is described in section 2.6.

Electrical contacts: The current in the MOSFET flows from drain to source and must enter and exit the device at these ports. To avoid voltage drop and power dissipation, both contacts should be ohmic and possess a low contact resistance. Although contact optimization can be quite demanding for n-type GaN, as is the case in this work, the procedure is relatively straight forward. Typically, the contact resistance makes only a small contribution to the total resistance. While the proper choice of metal stack and interface treatment determine the resistivity, the area of the source contact is also a relevant criteria. However, maximizing this contact directly contradicts the intention to minimize cell pitch.

No separate section is dedicated to electrical contacts in this chapter and a description of the actual fabrication process and the contact characterization is provided in the corresponding experimental chapter 5.

Bulk resistance of the n^+-source layer: The last and least relevant resistance component is the bulk resistance of the source layer through which the electrons must flow from the source contact to the channel entrance. Due to the high doping concentration of the source layer, its resistivity is low. The contribution to the overall resistance is usually negligible and not displayed in the graph in figure 2.4 b).

2.3 GaN as semiconductor material

To fabricate and optimize a semiconductor device, it is essential to understand the material it is made of. This section provides information about the gallium nitride crystal and material parameters. The latter will be put in perspective to silicon, SiC and other semiconductors.

2.3.1 Crystal structure of GaN

Depending on the condition, gallium and nitride can crystallize in three different phases: cubic rock salt, zinc blende or hexagonal wurtzite. The latter is the most common phase and the relevant one for the fabrication of electrical devices [79]. The crystal base consists of a gallium atom and a nitrogen atom with a predominantly covalent bond and a tetrahedral arrangement. Due to a large discrepancy in the electronegativity of gallium (1.81) and nitrogen (3.04), the bond features also an ionic character. In c-direction [0001], the crystal is stacked in ABAB order and is non-symmetric. This combination of asymmetry and ionic bonding character gives rise to a spontaneous polarization and two distinguishable crystal orientations, namely N-face and Ga-face. Both orientations are depicted in figure 2.5. The spontaneous polarization is oriented towards the N-face side of the crystal and can be increased or decreased if the crystal is put under tensile or comprehensive strain, respectively. This is due to the superimposed piezoelectric polarization, which occurs due to a shift of the centers of charge as the c/a ratio is altered when the crystal is put under stress. The c-planes, both (0001) and $(000\bar{1})$, are polar planes, while vertical planes on the other hand are, due to perfect crystal symmetry in lateral direction, non-polar. Important vertical planes are the a- and m-plane, also denoted with $(1\bar{2}10)$ and $(\bar{1}010)$, respectively, as they form the channel interface in trench MOSFETs. Apart from polarization effects, the various crystal planes posses different chemical stability. This leads to strong anisotropic behavior during wet etching procedures and will be discussed in more detail in section 2.5.2.

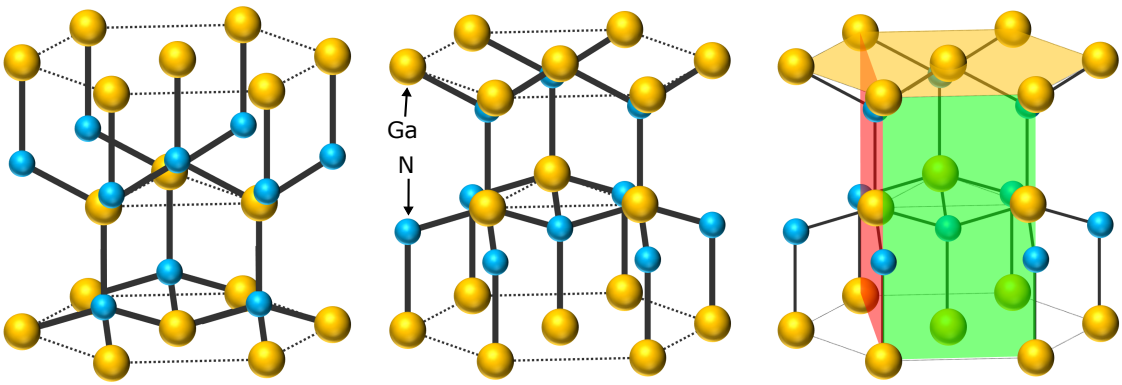

Figure 2.5: Ball and stick model of the GaN crystal in a) N-face and b) Ga-face orientation. c) GaN crystal in Ga-face orientation with the polar c-plane in orange and the nonpolar a- and m-planes in red and green, respectively.

2.3.2 Material parameters of GaN

Gallium nitride and other materials such as silicon carbide, gallium oxide, diamond, etc. are considered promising candidates for future power electronic devices. To understand the reason for this, it is useful to study some of the relevant material parameters that make them suitable and to put them in perspective with those of silicon, the most common semiconductor today. These parameters can be separated into two groups. The first, with parameters such as band gap, critical electric field and intrinsic carrier density, represents the ability of the semiconductor to withstand high voltage and is important during the off-state of the switch. The second group contains parameters such as carrier mobility, saturation velocity and thermal conductivity and represents the semiconductors ability to conduct current and heat, which is important during the on-state. Listed in table 2.1 are some important material parameters for several promising semiconductors as well as Baliga's figure of merit for power devices. Here normalized to silicon as

$$BFOM_{\mathrm{norm}} = \frac{\varepsilon_{\mathrm{r}} \mu E_{\mathrm{crit}}^3}{\varepsilon_{\mathrm{r_{Si}}} \mu_{\mathrm{Si}} E_{\mathrm{crit_{Si}}}^3}, \tag{2.4}$$

which is a measure of how suited a certain semiconductor is for power device application. The BFOM is typically normalized to its value for silicon. By evaluating these parameters, a theoretical limit for potential devices can be stated. This limit is plotted as the trade-off between area dependent on-resistance $R_{\mathrm{DSon}} A$ and breakdown voltage V_{B} for several materials in figure 2.6. The desired corner is the bottom right where high blocking capability is combined with low on-resistance, i.e. low on-state power dissipation. As can be seen from table 2.1 and the plot in figure 2.6, GaN is by far not the ideal power semiconductor. At least in theory, it is surpassed by more exotic candidates for example gallium oxide (Ga_2O_3), aluminium nitride (AlN) or diamond. However, several criteria beyond these material related parameters are essential to the adoption of a

new semiconductor in the wider market of power electronics or semiconductor devices in general. One is manufacturability of wafers and epitaxy with the key requirements of wafer cost, size and quality. Another is applicability to various sectors. Semiconductor processing lines and process development are expensive and the investments, necessary for the adoption of a new material, are considerable and only possible if a sufficiently large market can be targeted. Gallium nitride holds a relevant share in optoelectronics as well as in radio frequency and power electronics, which promotes its adoption. Finally, technical requirements such as availability of n- and p-type doping, contact resistance or interface quality and compatibility with existing materials and processing techniques, must be taken into account. Most of the more exotic materials lack sophistication or competitiveness in many of the mentioned areas, cost being chief among them. It is therefore unlikely to see market ready e.g. diamond transistors in the near future.

Table 2.1: Material specific parameters for various semiconductors. Also stated are the $BFOM_{\mathrm{norm}}$, cost of wafer+epitaxy and estimated defect density. Data from [80, 81, 32, 67].

Material	E_{g300} (eV)	E_{crit} (MV/cm)	μ_{e} (cm^2/Vs)	v_{sat} (10^7 cm/s)	λ (W/mK)	ε_{r}	$BFOM_{\mathrm{norm}}$
Si	1.12	0.3	1400	1	150	11.7	1
GaAs	1.42	0.4	8500	1.2	44	13.1	5
4HSiC	3.26	3	950	2	370	10	580
GaN	3.39	3.3	1000	2.5	253	9.5	765
Ga_2O_3	4.9	8	300	1.8-2	10-30	10	3450
AlN	6.2	12	300	1.7	285	8.5	10k
Diamond	5.45	10	3800	2.7	2200	5.5	47k

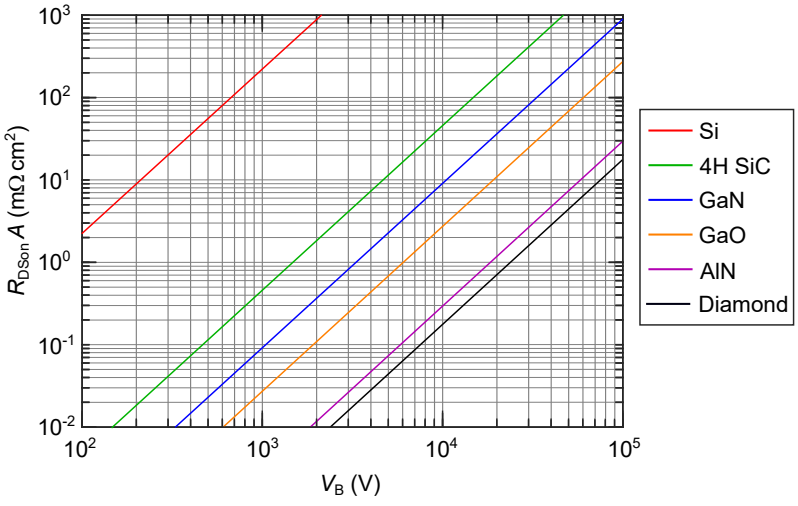

Figure 2.6: Trade-off between area dependent on-resistance $R_{\mathrm{DSon}}A$ and breakdown voltage V_{B} for silicon and various wide and ultra wide band gap semiconductors. Data from [81].

2.3.3 Bulk material and epitaxial growth of GaN

Silicon wafers can be fabricated in large quantity and diameter in high quality with extremely low cost. This has mainly three reasons: cheap and abundant raw material, i.e. quartz sand, the fact that it is possible to grow the crystals from a melt by using the Czochralski or zone melting process, and decades of experience with large quantity processing. Gallium nitride can not be grown from a melt and the growth procedures that are available are much less mature than for silicon. This limits GaN wafers to significantly smaller diameters, currently 2-4 inch, makes them inferior in quality and puts them orders of magnitude above silicon in terms of wafer cost.

The most common method for bulk GaN growth today is hydrate vapor phase epitaxy (HVPE). The gallium atoms are brought into the reactor as halides and the nitrogen atoms are supplied as ammonia. The procedure consists of two main reactions:

$$\begin{aligned} \text{Synthesis of GaCl:} \quad & 2\text{HCl} + 2\text{Ga} \longrightarrow 2\text{GaCl} + \text{H}_2 \\ \text{Synthesis of GaN:} \quad & \text{GaCl} + \text{NH}_3 \longrightarrow \text{GaN} + \text{HCl} + \text{H}_2 \end{aligned} \tag{2.5}$$

The GaCl synthesis takes place in a first chamber at 850 °C and the product is then fed into a second chamber with the GaN seed crystal present on which the second reaction and crystallization of GaN take place at 1000 °C. The growths rate of up to 500 µm/h is reasonably high and good control over material purity and doping concentration is achieved. Challenges are the density of defects and dislocations as well as their homogeneity over the wafer. Another factor that limits the wafer size is anisotropy in growth, especially in lateral direction. This causes the diameter of the crystal to shrink during growth and limits the achievable thickness.

Another promising technique is the ammonothermal growth of GaN where a high quality crystal is grown from a solvent, a technique which in principle has good scalability and the potential for significant cost reduction. Super critical ammonia at 10^5-$4 \cdot 10^5$ kPa and 400-600 °C [82] is used to dissolve gallium. So called mineralizers are added to increase the solubility. The solution is then moved to another region where it becomes supersaturated as pressure and/or temperature are changed. This causes GaN to crystallize on a prepared seed crystal.

The above mentioned techniques, as well as others such as high N_2 pressure solution growth or the Na-flux method [83], are used to grow relatively thick GaN crystals, ideally >1 cm. These crystals, called boules, are cut and polished to obtain substrate wafers. Further GaN growth is then required to fabricate epitaxial layers with specified thickness and doping concentration on the substrate. The two most common methods are metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE).

For the MOCVD process the precursor gases trimethylgallium and ammonia are, along with carrier gases, guided over the hot wafer. At temperatures of 400 to 1300 °C the precursors release gallium and N atoms, which then react to GaN on the wafer surface. The MOCVD technique achieves reasonably high growth rates, high purity and allows good control over layer thickness and doping concentration. Usually n- or p-type doping is required for the grown epitaxial layer. This is achieved by introducing precursors that contain the required dopants silicon or magnesium. Commonly used precursors are silane (SiH_4) and bis-cyclopentadienylmagnesium (Cp_2Mg) [72]. A major drawback is that many of the used gases are extremely toxic and some are pyrophoric.

The alternative is MBE, which is conducted under ultra high vacuum at lower temperatures than MOCVD. The precursors are stored in crucibles, which are heated in order to evaporate and guide the desired atoms and molecules in form of a molecular beam onto the wafer surface. By altering the heating of the crucibles, growth rate and layer composition can be controlled. Mechanical shutters allow a quick interruption of the growth process and make structures with abrupt interfaces possible. The nitrogen is usually supplied by one of two ways. Either as ammonia flowing into the chamber or in form of plasma generated nitrogen radicals. The disadvantage of MBE is its comparably high cost. Even though the control over layer growth and material composition for MBE is superior to that for MOCVD, the latter is typically preferred due to higher throughput and lower cost.

2.4 Drift- and p-base layer requirements and doping in GaN

In this section, design and configuration of drift and p-base layer will be discussed in the context of a GaN trench MOSFET. Since doping and the corresponding impurity ionization have a crucial impact on both layers, an introduction to this topic is provided as well.

2.4.1 Design of the drift- and p-base layer

The resistance of drift layer and inversion channel are the main contributors to the total device resistance. As illustrated in figure 2.4 b), other contributions such as contact resistance are far less relevant. A fundamental limitation for the drift layer is the critical field strength of gallium nitride. This is determined by the impact ionization coefficients and was empirically found to depend on doping concentration as $E_{\mathrm{crit}} \propto N_{\mathrm{D}}^{1/8}$ [8]. This relation implies at a first glance, that a higher doping concentration is beneficial for higher breakdown voltage. However, if the voltage drop across the depletion zone is considered, the relation becomes $V_{\mathrm{B}} \propto N_{\mathrm{D}}^{-3/4}$ [8]. This means, the breakdown voltage decreases with increasing doping concentration. Figure 2.7 a) shows the breakdown voltage and on-resistance as function the drift layer doping concentration for different drift layer

thicknesses along with the GaN material limit. Beyond this limit, in the area to the top right, impact ionization will occur and the depletion zone becomes conductive. If the drift layer possesses a finite thickness, punch through can occur. This is typically the case for diodes and transistors, where the punch through design is used [84]. In this case, the field distribution has a trapezoidal shape. The achievable breakdown voltage as function of the doping concentration is plotted in figure 2.7 a) for different drift layer thicknesses.

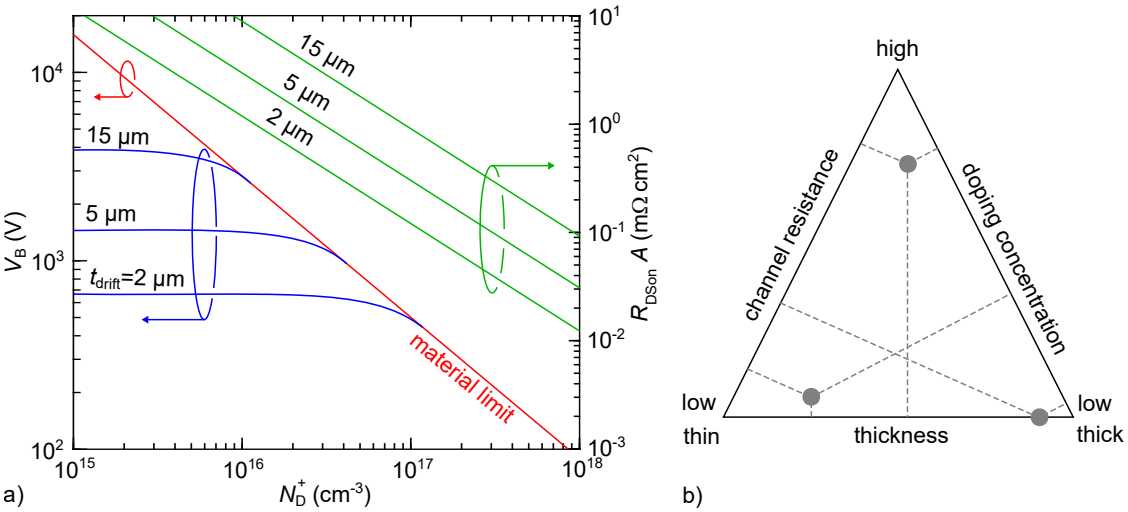

Figure 2.7: a) Critical GaN breakdown voltage due to material limitation (red) and for drift layers with finite thickness and punch through design (blue). The latter is shown exemplarily for three different thickness values. The green lines represent the respective theoretical area specific drift layer resistance. b) Qualitative illustration of the dependence between thickness and doping concentration of the p-base layer and the MOS-channel resistance at its interface for three exemplary configurations.

As mentioned above, low resistivity in the on-state is desirable for the drift layer. As illustrated by the green lines in figure 2.7 a), resistivity increases for a thicker and lower doped drift layer. This dependence between resistance and breakdown voltage is the basis for the plot in figure 2.6 and leads to a trade-off between both quantities. Note that the correlations in figure 2.7 a) are based on the assumption of a plane parallel field distribution, which represents the situation in a real device only to a certain degree. The drift layer resistance is calculated from bulk mobility values based on results from a fit to the Caughey-Thomas expression [85] for literature data from [86].

Careful designing is also mandatory for the p-base layer. Although it is usually higher doped than the drift layer, the depletion zone also extends into the p-base layer and can cause a punch through if sufficient thickness and doping concentration is not ensured. On the other hand, a thicker p-base layer means a longer MOS channel and therefore a higher resistance. The same is true for higher doping concentration, which affects the interface quality and increases the voltage required to achieve strong inversion. Both leads to a higher channel resistance. The triangle in figure 2.7 b) illustrates in a qualitative way how thickness and doping concentration of the p-base layer affect the MOS inversion channel

resistance. The high activation energy of the magnesium acceptors in GaN ($\approx 220\,\mathrm{meV}$) can make the design of p-regions quite tedious. The amount of ionized acceptors depends strongly on the lattice temperature, which can affect device behavior, e.g. due to changes in threshold voltage and channel resistance. It requires also a certain safety margin to avoid punch through during the off-state. Especially for high frequency operation and at low temperature, the phenomenon of dynamic punch through must be considered [87]. A similar phenomenon was observed in SiC [88] where ionization energies for acceptors are similarly high as in GaN. If the switching frequency is high, the rise time of the bias step from low on-state bias to high blocking bias (cf. fig. 2.2) can become shorter than the ionization time of the magnesium acceptors. The incomplete ionization of the p-base layer leads to a temporarily over expansion of the depletion region between drift- and p-base layer. If doping concentration or thickness of the latter are too small, punch through will occur [87]. A useful and often necessary measure to rule out, at least in parts, the off-state requirements for the p-base layer, is active shielding [89]. This is done by introducing additional and highly doped p-type regions that reach deeper into the drift layer. Since this work focuses on the MOS gate structure, the fabricated devices are designed exclusively for on-state operation and no shielding structures are implemented.

2.4.2 Overview of doping in GaN

Doping of a semiconductor is essential for the fabrication of any semiconductor device. The ideal scenario, as in the case of silicon, allows the incorporation of shallow donors and acceptors with an energy difference of a few $k_\mathrm{B}T$ from the respective band edge. This allows a high amount of ionization, enabling high carrier concentrations without the necessity to incorporate orders of magnitude more dopants, which in turn would lead to material degradation, generation of compensation centers and a loss in carrier mobility. For GaN as a binary semiconductor, it is relevant whether the dopant is incorporated into a gallium site or a nitrogen site. While most atom species have a preferred configuration, some are amphoteric and can occupy both. This can be problematic as they tend to act as donor or acceptor depending on the site they occupy. Silicon atoms, which replace gallium in the crystal, act as shallow donors with an energy level 20 meV below the conduction band edge and are the most common choice for n-type dopants in GaN. The incorporation of silicon is achieved by means of ion implantation or by adding silane during the bulk or epitaxial growth. Free carrier concentrations in the range from 10^{17} to $2 \cdot 10^{19}\,\mathrm{cm}^{-3}$ were achieved so far [53]. This range implies another requirement for semiconductor doping. Especially for drift layers in vertical devices or buffer layers in GaN HEMTs, a low doped or highly resistive material is preferred. This can only be achieved if background doping concentration is either kept low or is compensated. In the case of GaN, it is believed that unintentionally incorporated oxygen atoms, located at nitrogen sites, act as donors and increase the free carrier density in intrinsic GaN (i-GaN) [72]. It was found that the introduction of carbon as amphoteric impurity can be used for counter doping in order

to further reduce free carrier concentration in n-type GaN or to obtain highly resistive layers. At the other end of the range, doping concentrations beyond $2 \cdot 10^{19}\,\mathrm{cm}^{-3}$ cannot be achieved since high silicon content in the crystal causes tensile strain. This leads to a degradation of the crystal and to gallium vacancies. These act as acceptors in a self compensating manner [72]. Although the mentioned limitations exist, n-type doping in GaN is relatively easy and possible over a wide range. The p-type doping on the other hand, is much more challenging. Although group four atoms on nitrogen sites would act as acceptors, they tend to occupy the gallium sites and become donors as in the case of silicon [72]. This leaves alternatives such as magnesium, beryllium, zinc or cadmium [72], of which only magnesium has a reasonable low, but still high activation energy of $\approx 200\,\mathrm{meV}$. This leads to an activation of only about 1-10 % at room temperature and makes high impurity concentrations necessary, even for a medium hole density. Similar to the case of silicon incorporation, magnesium concentrations beyond $10^{19}\,\mathrm{cm}^{-3}$ lead to material degradation and a drastic reduction of hole mobility [72]. Furthermore, the magnesium becomes passivated by hydrogen during the growth process and needs to be activated by means of thermal annealing.

2.4.3 Impurity ionization

The challenge of p-type doping was already addressed in section 2.4 in a qualitative manner. Since it is important for the device simulations in chapter 6, a more rigorous discussion will be given in this section. The expression ionization will in this context be used to describe the extraction of an electron from the atom into the crystal and not as commonly used into the vacuum.

An atom that is introduced into the semiconductor with the intention to act as a dopant, can end up in three different states. The first one is as inactive impurity, i.e. not properly located at a crystal site but somewhere in between. The concentration of this species is denoted as $N_{[\mathrm{Si}]}$ and $N_{[\mathrm{Mg}]}$ in inverse cubic centimeters for introduced silicon and magnesium, respectively. This is usually the case after the atom was introduced, e.g. via ion implantation or during epitaxial growth. Thermal annealing leads to a relocation of these atoms so that some of them get incorporated into the semiconductor crystal. This is the second state and the respective atom has become an active dopant or more precisely an acceptor with corresponding density N_{A} in the case of magnesium or a donor with corresponding density N_{D} for silicon atoms. The extend to which impurities are incorporated into the crystal is still up to debate and the following assumption will be made for this work.

$$N_{\mathrm{A,D}} = K_{\mathrm{A,D}} \cdot N_{[\mathrm{Mg,Si}]} \quad \text{with} \quad K_{\mathrm{A,D}} = \frac{F_{\mathrm{A,D}}}{1 + \left(\frac{N_{[\mathrm{Mg,Si}]}}{N_{\mathrm{A_0,D_0}}}\right)^{\beta_{\mathrm{A,D}}}} \tag{2.6}$$

The factor $K_{\mathrm{A,D}}$ is adjusted by the fitting parameters $F_{\mathrm{A,D}}$, $N_{\mathrm{A_0,D_0}}$ and $\beta_{\mathrm{A,D}}$ and justified as follows. The graph in figure 2.8 a) shows the factor K as function of doping concentration for different values of β and the example of magnesium doping. Depending on β, K is close to unity for low impurity concentration, resulting in an approximately linear dependence between $N_{[\mathrm{Mg}]}$ and N_{A}. This is in good agreement with literature data [90–92]. For higher impurity concentrations K drops significantly and the plot in figure 2.8 b) illustrates the resulting acceptor concentration. Effects such as lattice damage can lead to a reduction of acceptors N_{A}. Due to unintended impurities and crystal imperfection, the semiconductor always contains acceptor and donor like impurities. This leads to partial compensation of the intended impurities. The parameter F in equation (2.6) is introduced to model the two competing species with different concentrations. For the intended species, F should be close or equal to one while it is significantly smaller for the unintended species.

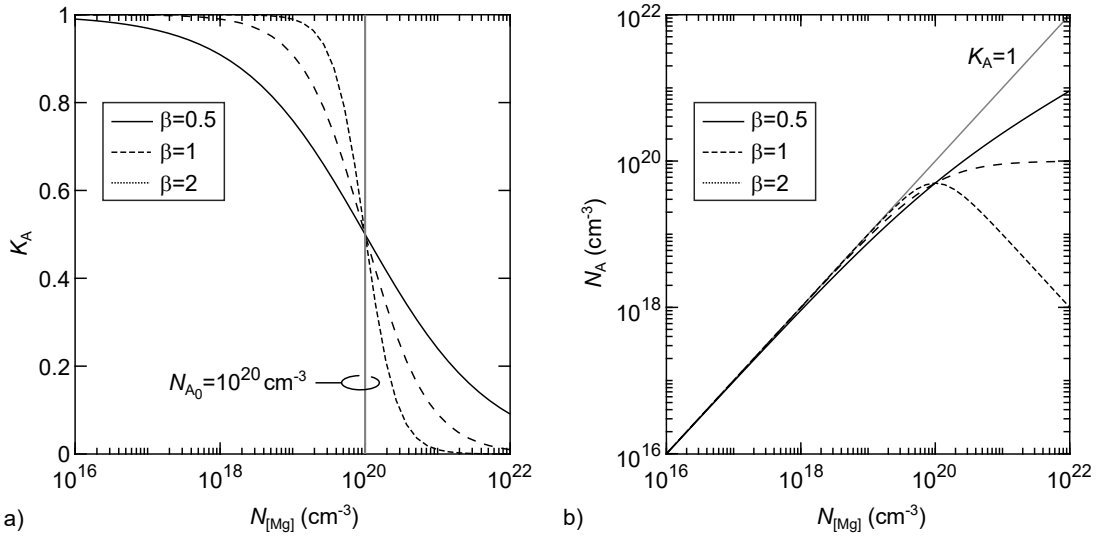

Figure 2.8: a) Exemplary curves for the proportionality factor K_{A} and the resulting dependence between acceptors and magnesium concentration in b).

Depending on the ionization energy of an active dopant, it will become ionized, which moves it to the third and final state, with the respective density denoted as N_{A}^{-} and N_{D}^{+}. Only impurity atoms at the final state, i.e ionized dopants, contribute to the free carrier density n and p. Non-incorporated impurities (state one) and active but non-ionized dopants (state two) do not contribute directly. The amount of free carriers is given by [93] as

$$p+N_{\mathrm{D}}=\frac{N_{\mathrm{A}}}{1+\frac{pg_{\mathrm{A}}}{N_{\mathrm{V}}}\exp\left(\frac{E_{\mathrm{IA}}}{k_{\mathrm{B}}T}\right)}\quad\text{for holes and}\quad n+N_{\mathrm{A}}=\frac{N_{\mathrm{D}}}{1+\frac{ng_{\mathrm{D}}}{N_{\mathrm{C}}}\exp\left(\frac{E_{\mathrm{ID}}}{k_{\mathrm{B}}T}\right)}\quad\text{for electrons.} \tag{2.7}$$

The degeneracy factors are $g_\mathrm{A} = 4$ and $g_\mathrm{D} = 2$ The effective density of states at the band edges are given as

$$N_\mathrm{V} = N_\mathrm{V300}\left(\frac{T}{300}\right)^{3/2} \quad \text{and} \quad N_\mathrm{C} = N_\mathrm{C300}\left(\frac{T}{300}\right)^{3/2} \tag{2.8}$$

with the material constants $N_\mathrm{V300} = 4.62\mathrm{e}19\,\mathrm{cm}^{-3}$ and $N_\mathrm{C300} = 2.85\mathrm{e}18\,\mathrm{cm}^{-3}$ from [94].

The ionization energy E_IA for acceptors and E_ID for donors, is a function of the doping concentration and decreases for higher doping. The reasons for this are manifold, the most relevant being a broadening of the impurity band for higher impurity concentration due to Pauli's principle. This reduces the gap towards the respective band edge, and thus, lowers the ionization energy. High impurity concentration is believed to cause valence or conduction band band-tail states [90], which also reduce the energy gap between dopant and respective band edge. Further reasons include screening of dopant potential by free carriers and a reduction of binding energy due to coulomb interaction between valence- and conduction band states and the respective dopant. The relation is typically modeled as

$$E_\mathrm{IA} = A_\mathrm{EA} - B_\mathrm{EA}\left(N_\mathrm{A}^-\right)^{1/3} \quad \text{and} \quad E_\mathrm{ID} = A_\mathrm{ED} - B_\mathrm{ED}\left(N_\mathrm{D}^+\right)^{1/3} \tag{2.9}$$

with $A_\mathrm{EA,ED}$ and $B_\mathrm{EA,ED}$ being fitting parameters.

Using equations (2.6) to (2.9), the carrier density can be expressed as

$$\begin{aligned} N_\mathrm{A,D}^{-,+} = p, n = &\left[-\frac{N_\mathrm{V,C}}{2g_\mathrm{A,D}}\exp\left(\frac{-E_\mathrm{IA,ID}}{k_\mathrm{B}T}\right) - \frac{N_\mathrm{D,A}}{2}\right] \\ &+ \left[\frac{N_\mathrm{V,C}^2}{4g_\mathrm{A,D}^2}\exp\left(\frac{-2E_\mathrm{IA,ID}}{k_\mathrm{B}T}\right) + \frac{N_\mathrm{V,C}N_\mathrm{D,A}}{2g_\mathrm{A,D}}\exp\left(\frac{-E_\mathrm{IA,ID}}{k_\mathrm{B}T}\right)\right. \\ &\left. + \frac{N_\mathrm{D,A}^2}{4} + \frac{N_\mathrm{V,C}(N_\mathrm{A,D} - N_\mathrm{D,A})}{g_\mathrm{A,D}}\exp\left(\frac{-E_\mathrm{IA,ID}}{k_\mathrm{B}T}\right)\right]^{1/2} \end{aligned} \tag{2.10}$$

This term includes the effect of compensation by donors in the case of doping with acceptors and vice versa. It is the basis on which the properties of drift- and p-base layer, as well as the respective carrier mobility, are determined.

2.4.4 Carrier bulk mobility

Building on the relations for dopant ionization, established in section 2.4.3, a model for carrier mobility in bulk material can be set up. Unlike for silicon, there is no universal and reliable mobility model for GaN. The general approach for the simplest case, i.e. carrier mobility in bulk material, is a dependence on temperature and impurity concentration.

While the former is relatively clear, the latter can be interpreted in different ways. As introduced in section 2.4.3, there are three different concentrations of impurities in a doped semiconductor and it is not clear what their contributions to mobility reduction are. In this work, the assumption will be made that the bulk mobility is only affected by ionized impurities. This assumption is reasonable since the scattering cross section of neutral impurities is much lower than for ionized ones [95]. The contributions to bulk mobility reduction, which will be taken into account, are coulomb scattering at impurities as well as scattering at bulk phonons. The following equation, proposed by Uhnevionak et al. [96], is used:

$$\mu_\mathrm{b} = \mu_\mathrm{min}\left(\frac{T}{300}\right)^{\alpha} + \frac{\mu_\mathrm{bp1}\left(\frac{T}{300}\right)^{\mathrm{exp1}} + \mu_\mathrm{bp2}\left(\frac{T}{300}\right)^{\mathrm{exp2}} - \mu_\mathrm{min}\left(\frac{T}{300}\right)^{\alpha}}{1 + \left(\frac{T}{300}\right)^{\mathrm{exp3}}\left(\frac{N_\mathrm{A,D}^{-,+}}{N_\mathrm{ref}}\right)^{\mathrm{exp4}}} \tag{2.11}$$

For this work, literature values were used to calibrate the model and to obtain a foundation upon which the more advanced mobility model for the MOS inversion channel was built. A description of the said channel mobility is provided in section 2.6.4.

2.5 Dry and wet etching of GaN

Although this section covers dry and wet etching in a fairly general manner, the focus lies on the etching of GaN. Information about the etching of more common materials such as silicon dioxide and silicon, can be found in literature, such as [97], and is not provided in this section. Specific etching processes concerning poly Si and SiO_2 that were used in this work are described in the respective sections in chapters 3, 4 and 5.

Etching of semiconductor and dielectric materials are essential process steps in semiconductor device fabrication. The two most important properties of an etching process are selectivity and isotropy. Selectivity describes the ratio of the etch rates of two different materials for a given etching process and is usually desired to be high. Isotropy is a measure for how uniform a material is etched in different directions, e.g. lateral vs. vertical etch rate and is, depending on the structure, desired to be low. The two basic types of etching used in semiconductor processing are wet and dry etching. Wet etching, and also gas phase etching, is a purely chemical etching procedure with generally high selectivity but a usually higher isotropy. This makes the process unsuitable for the fabrication of small structures with high aspect ratio. Dry etching uses plasma generated, positively charged reactants, which are directed onto the surface that is to be etched. This adds a physical component to the chemical etching and achieves a more anisotropic etching with the drawback of reduced selectivity.

2.5.1 Dry etching of GaN

Compared to wet etching, which is a fairly simple and easily scalable process, dry etching is much more sophisticated and many different types of dry etching, also called plasma etching, exist. However, the basic principle is always similar and will be described here for inductively coupled plasma (ICP) etching. This is a common technique today and was used for this work. Depending on the specimen that is to be etched, the etch chemistry must be chosen. Commonly used gases are sulfur hexafluoride or chloride based compounds for etching of Si, SiC or GaN. A dielectric with oxygen bonds such as SiO_2 is usually etched by using carbon rich gases such as CF_4 or C_4F_8. The essential components of an ICP-tool are visualized by the schematic in figure 2.9 a) and the etching process is conducted as follows. The reactive gas is typically mixed with an inert gas such as helium (He) or argon (Ar), which can be easily ionized and increases the plasma density. This in turn stabilizes the plasma during ramp-up or switching phases. This stabilization gas also provides ions for the physical bombardment of the wafer surface. The mixture of reactive and inert gases is inserted through the gas inlets at the top of the reaction chamber. A magnetic radio frequency (RF) field, in fig. 2.9 a) generated by the coils near the chamber top, leads to excitation, ionization and dissociation for a fraction of the gas molecules. Due to official requirements, a frequency of 13.56 MHz is commonly used. The reactive species in the gas mixtures are single atom radicals such as $F^\bullet$ and $Cl^\bullet$ as well as monomers and ions for example $C_xF_y^+$, SF_x^+ or Cl^+. If brought in contact with the wafer surface, they cause chemical reactions and form etch products such as SiF_4 or $SiCl_4$ for silicon etching, CO and O_2 for SiO_2 etching and gallium trifluoride (GaF_3) or gallium trichloride ($GaCl_3$) in the case of GaN etching. These etch products are then removed either due to their own volatility or by means of sputter desorption.

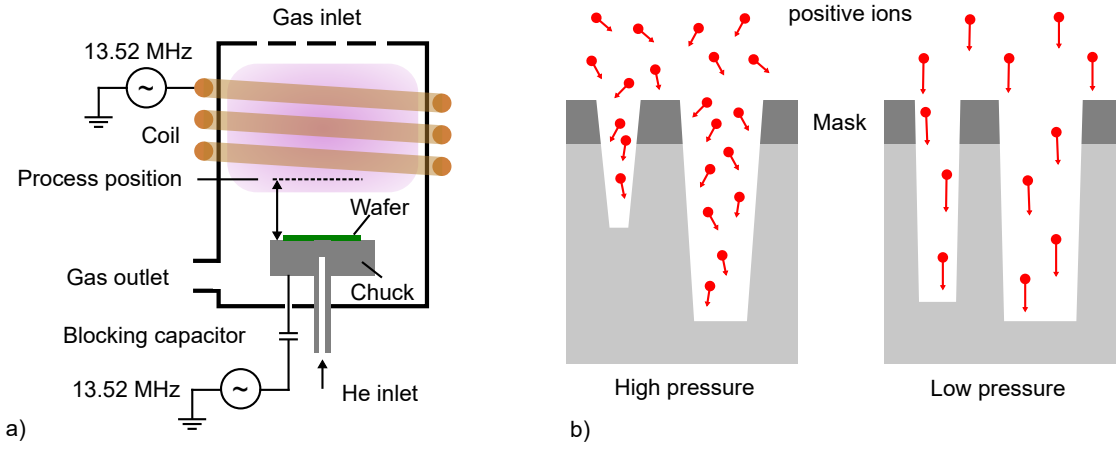

Figure 2.9: a) Schematic drawing of an ICP etching tool. b) Visualization of the etching process and ion scattering during a process with low and high chamber pressure for a narrow and wide trench structure.

Depending on the power that is coupled into the plasma, denoted as coil power, the plasma density and number of reactive species can be influenced. The chamber pressure

for ICP tools is typically in the range of 5 to 25 mTorr. The generated plasma is a low temperature plasma that is, with 10^9 to 10^{12} ions per cubic centimeter, only weakly ionized [97]. However, compared to other dry etching techniques such as capacitively coupled plasma etching, the plasma generated by an ICP etching tool is rather dense. In addition to the magnetic RF field at the chamber top, a linear electric RF field of the same frequency is generated between the chamber top and the chuck at the chamber bottom on which the specimen or wafer is located and kept in place by either mechanical or electrostatic clamping. Only the electrons in the plasma can follow the frequency and can reach the chuck and the walls at the chamber top. These two surfaces act as electrodes of which the chuck has by design the smaller area and thus a lower electric potential due to a higher density of electrons located there [97]. This circumstance implies that the etching result depends not only on the process parameters but also on the chamber geometry, and thus, is significantly related to the tool that is used. The so called platen bias builds up between the plasma region and the chuck and is stabilized by the blocking capacitor (cf. fig. 2.9 a)). The result is an acceleration of positive ions towards the chuck where they cause physical bombardment on the specimen. The negative bias of the mentioned electrodes repels negative charged particles and leads to an electron free region directly above them. This so-called ion sheath or dark region [97] is several hundreds of microns thick and ensures a quasi collision free approach of the positive ions. This leads to a more directed ion bombardment and increases anisotropy. According to the hot spot model [97], the ions that bombard the surface of the specimen cause a localized rise in temperature, which lowers the amount of energy necessary to break the chemical bonds of the material. This enhances the chemical etching described above and, in combination with other effects such as sputter desorption and guiding of reactants, allows a more anisotropic etching compared to wet or gas phase etching, i.e. chemical etching alone. The drawback is a decrease in selectivity. The physical bombardment applies to all materials equally and also increases the etch rate for materials that are less prone to be etched due to chemical reactions alone.

The ICP etching tool allows, to a certain degree, an independent tuning of coil and platen power. Therefore, the plasma density, i.e. the amount of chemical etching and the platen bias, affecting the amount of physical etching, can be adjusted independently. Another important aspect is the wafer temperature during the etching process. Especially for processes with a high physical component, the wafer temperature can rise beyond 100 °C [98] if no sufficient cooling is provided. This is achieved by a flow of helium in the microscopic voids between the wafer and the actively cooled chuck. The high thermal conductivity of helium ensures a good heat transfer. The wafer surface temperature has a crucial impact on the chemical reactions during the etching. Especially during processes with thermally sensitive materials such as photoresist, high temperatures can be fatal. Loss of contours due to a rise beyond the glass transition temperature or resist burning can be the result. Therefore, an equilibrium between temperature input due to coil and

platen power and cooling from the chuck must be obtained for a temperature that is tolerable for the process and the materials.

The etching of trenches, as needed for the trench MOSFET or other vertical devices, requires plasma etching. Highly directional, i.e. anisotropic, etching is mandatory for high aspect ratios and uniformity between wide and narrow structures. The anisotropy of the etching process in an ICP tool is determined by two major aspects, platen power and chamber pressure. The platen power affects the platen DC bias and therefore the energy and velocity of the ions, which bombard the wafer surface. The chamber pressure determines the collision rate of the particles and therefore is related to the particle density and the mean free path of the ions. ICP etching tools achieve a comparably high plasma density and hence are able to maintain a stable plasma under low pressure. As illustrated in figure 2.9 b), low chamber pressure reduces ion scattering, leads to higher ion velocity, and a more directional etching. This in turn increases sidewall steepness and reduces the etch rate difference between narrow and wide structures. The down side of highly physical etching and dry etching in general, is ion induced damage. The ionic impact can cause crystal damage and can lead to a non-stoichiometric, rough surface as well as the incorporation of charges and impurities. This causes a challenge for dry etching of GaN. Its high binding energy of 8.92 eV/atom [56, 99] for the Ga-N bonds in combination with the requirement of steep and narrow trenches requires a substantial amount of physical etching [57, 99]. High ion energy was found to be most efficient in bond breaking and sputter desorption of etch products [100]. The common etch chemistry for GaN dry etching is a combination of boron trichloride (BCl_3) and chlorine (Cl_2) [56, 57]. The reactive species in this process are chlorine radicals, which form the relatively volatile etch product gallium trichloride ($GaCl_3$) with a boiling point of 201 °C [100]. The addition of BCl_3 was found to be useful for sputter desorption due to its higher mass [100]. Using 100 W coil power and 300 W platen power, Zhou et al. [59] demonstrated high etch rates of 850 nm/min and a good selectivity to SiO_2 hard masks of 8 for this process. The down side of chlorine based dry etching is the high safety standard required to handle the corrosive and hazardous gas [56]. This makes the etch tool as well as peripheral infrastructure expensive. In addition, several process steps, especially such that are related to silicon-SiO_2 interfaces, are prone to chlorine contamination. This makes chlorine based etching partially incompatible with certain fabrication lines. It is also known that the chlorine attacks the aluminum walls of the etching chamber causing removal of wall material and, depending on previous processes, other impurities [101, 102]. This can be problematic for interface related processes such as the etching of the gate trench.

An alternative is a sulfur hexafluoride SF_6 based etching chemistry, the approach that was pursued in this work. The SF_6 is dissociated into $F^\bullet$ radicals and SF_x^+ monomers. The radicals react at the GaN surface to gallium trifluoride GaF_3 and nitrogen trifluoride (NF_3). Using SF_6 in combination with N_2 or Ar, allows equally high etch rates but requires higher ion energy, i.e. more platen power. The reason for this is the non-volatility of the etching product GaF_3. While NF_3 has a low boiling point of -130 °C,

the boiling point of of GaF_3 is 1000 °C. The latter can therefore only be removed by sputter desorption. The necessity of high ion energy leads to several challenges that must be addressed in order to fabricate trenches that satisfy the requirements regarding geometry and surface quality.

2.5.2 Wet etching of GaN

Similar as for dry etching, the high bond energy of GaN makes it inert against many of the common etchants such as HCl, HF, H_2O_2, H_2SO_4 etc. [103]. However, it was found that strong alkaline solutions for example potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) do etch certain planes of the GaN crystal. The etching follows the chemical equation

$$2\,\mathrm{GaN} + 3\,\mathrm{H_2O} \xrightarrow{\text{KOH, TMAH}} \mathrm{Ga_2O_3} + 2\,\mathrm{NH_3} \tag{2.12}$$

and is driven by the hydroxide ions OH^- in the alkaline solution. These ions bind to the gallium atom and form GaO_x, which is then dissolved [104, 105]. The remaining nitrogen binds to the hydrogen atoms to form NH_3, which is also dissolved. The key factor and reason for the anisotropic etching of GaN in these solutions is the accessibility of the GaN atoms for the OH^- molecules. This accessibility depends on the crystal plane, or more precisely the specific surface energy of a certain facet of the GaN crystal. Lai et al. [64] proposed the etching barrier index (*EBI*) as a measure of how good OH^- molecules can reach the GaN atoms and how good or fast a GaN facet is etched. The *EBI* is defined as the product of planar density P_D, i.e. atoms per $\mathring{A}^2$ and number of dangling bonds per nitrogen atom n_N. A high P_D represents a surface that is more closely packed and provides less access points for the OH^- molecules. Due to their negative charge, the dangling bonds of the nitrogen atoms repel the also negatively charged OH^- molecules. This means a crystal plane with higher *EBI* is etched slower or not at all, while planes with smaller *EBI* are etched faster. The ball and stick models in figure 2.10 a) and b) show the most important nonpolar and semipolar planes of the GaN crystal. The plot in figure 2.10 c) displays *EBI*, P_D and n_N for various crystal planes. The respective values are also stated in table 2.2.

Note that two different *EBI*s are listed for some of the planes. The reason for this is the asymmetric crystal pattern along the respective axes, which leads to representations with $n_\mathrm{N} = 1$ or 2 at different positions. This circumstance is illustrated exemplary for the m-plane in figure 2.11. Assuming the crystal is etched from right to left, the surface configuration for the blue plane features two nitrogen atoms with one dangling bond each. When the etching proceeds, the surface configuration changes as the green plane is reached, where each nitrogen atom features two dangling bonds. This leads to the two different values of n_N stated in table 2.2 and occurs in a similar manner for other planes such as the s_1, s_3 or s_4 plane. Since the different configurations are etched consecutively,

Table 2.2: Planar density, number of dangling bonds and etching barrier index for planes in the GaN crystal lattice.

Crystal plane	Miller index	Angle (°)	P_D (atoms $Å^2$)	n_N (1/atom)	EBI ($1/Å^2$)	Ref.
c^+	(0001)	0	0.1138	3	0.3414	[64]
m	$(10\bar{1}0)$	90	0.1211	1, 2	0.1211, 0.2422	[64]
a	$(1\bar{2}10)$	90	0.1398	1	0.1398	this work
c^-	$(000\bar{1})$	0	0.1138	1	0.1138	[64]
s_5	$(\bar{1}011)$	61.68	0.0534	1.5	0.08	this work
s_4	$(\bar{1}012)$	42.86	0.0414	1, 2	0.041, 0.0828	this work
s_2	$(\bar{1}2\bar{1}2)$	58.12	0.06	1	0.06	this work
s_3	$(\bar{1}2\bar{1}1)$	72.72	0.0337	1, 2	0.0337, 0.067	this work
s_6	$(\bar{2}021)$	74.92	0.0292	1.5	0.0438	this work
s_1	$(\bar{1}2\bar{1}3)$	46.97	0.0278	1, 2	0.0278, 0.056	this work

the EBI was, in first approximation, assumed to be the average of both configurations, which is also the value that is plotted in figure 2.10 c). Furthermore, some planes are listed with $n_N = 1.5$, as for these configurations half of the nitrogen atoms feature two dangling bonds and half of them only one. Compared to above, where two different surfaces occur consecutively during the etching, in this case, all surface configurations are identical and the EBI is unambiguous. Based on the EBI, it can be predicted, which planes of the crystal emerge during etching processes. The related experiments and results will be discussed in section 3.2.

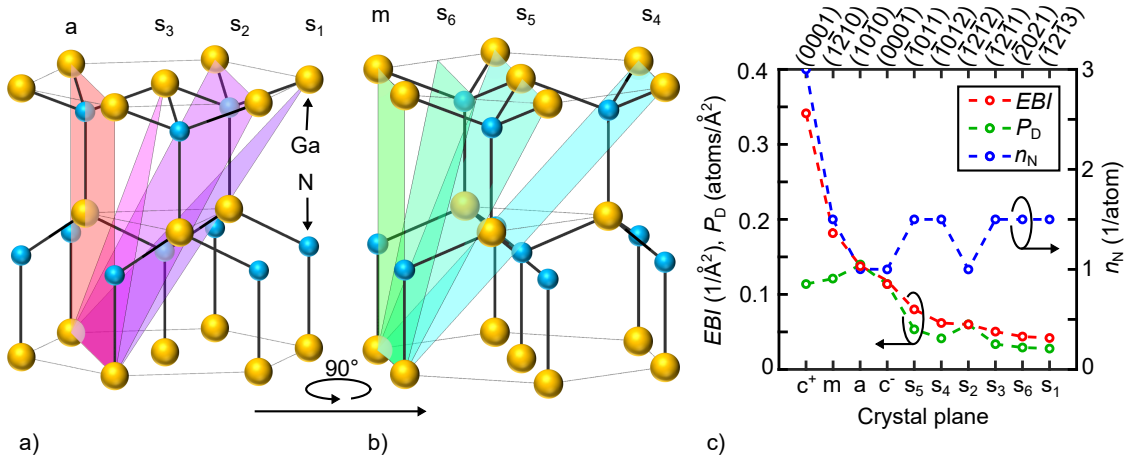

Figure 2.10: a) Nonpolar a-plane and related inclined semipolar s_{1-3} crystal planes in the wurtzite GaN unit cell. b) nonpolar m-plane and related inclined semipolar s_{4-6} crystal planes. c) Plot of EBI, P_D and n_N for various crystal planes in wurtzite GaN.

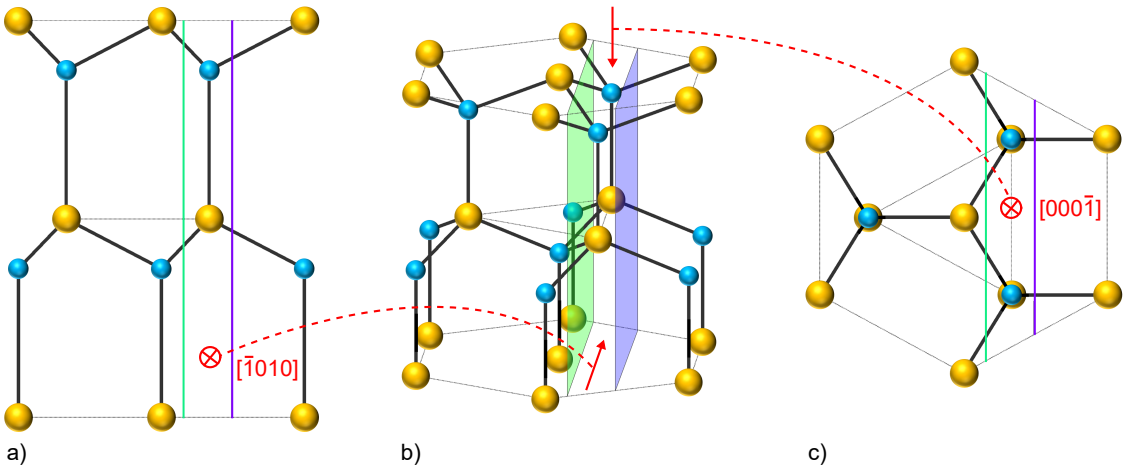

Figure 2.11: Illustration of the m-plane crystal ambiguity. Depending on the location, the plane features one dangling bond per nitrogen atom (blue) or two (green).

2.6 MOSFET function principle and fundamentals of the MOS inversion channel

This section constitutes the main part of the fundamentals chapter. It concerns the MOSFET in general and treats the physical and electrical aspects of the MOS inversion channel in particular. For illustrative reasons, the function principle of a MOSFET is described for a lateral device, followed by a description of the origin and properties of an ideal MOS inversion channel and an account on the electrical properties of a MOSFET. Subsequently, aspects of a real MOS interface, with focus on defect and charge density, are described and their effect on the electrical behavior is discussed. The section concludes with a passage regarding MOS capacitors and methods concerning their electrical characterization.

2.6.1 Function principle of the MOSFET

As a unipolar device the MOSFET has the ability of fast switching and the field effect based function principle requires much less gate drive current than for a bipolar device. A basic distinction can be made between p- and n-type MOSFETs were the charge carriers, contributing to the current flow, are holes or electrons, respectively. Power MOSFETs are almost exclusively n-type devices. This is not only the case for silicon but also for the wide band gap semiconductors SiC and GaN. The reason is the much higher mobility of electrons compared to that of holes in all these materials, which makes n-type MOSFETs more conductive and thus, more efficient than their p-type counterparts. Therefore, the function principle of the MOSFET will be discussed on the basis of an n-type MOSFET. A schematic of a basic planar n-type MOSFET is shown in figure 2.12. The device consists of a p-type area with two highly n^+-doped regions connected to the source and drain contacts, respectively. Insulated by a non-conductive layer, the gate electrode

bridges the n^+-regions and forms, if positive bias is applied, a conductive channel between them. This channel is referred to as MOS inversion channel and is the key component of a MOSFET. To form an inversion channel, a potential barrier must be established between a metal, or metal like material, and the semiconductor. Two common ways to achieve this are a Schottky barrier or an insulating material that is located between metal and semiconductor. If the insulator in the latter case is an oxide, the device is referred to as a MOSFET. If this barrier blocks the carrier flow in at least one direction, a potential difference between metal and semiconductor can be established and leads to a bending of the conduction and valence bands. Depending on semiconductor type and potential gradient, minority or majority carriers can be accumulated at the semiconductor surface. In the case of majority carriers, the channel is denoted as accumulation channel, for minority carriers it is referred to as an inversion channel. Figure 2.13 shows the energy bands for an n-type MOS channel in various states.

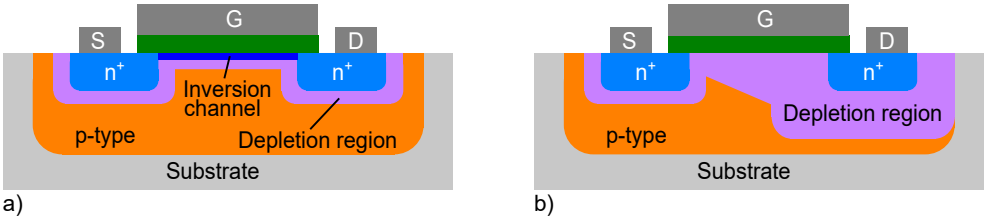

Figure 2.12: Schematic drawing of a basic n-type MOSFET in the on-state a) and off-state b).

If a negative voltage is applied to the metal electrode, the Fermi energy is raised and the semiconductor bands are bent upwards in accordance with the potential Φ_{surf} at the semiconductor surface. While minorities, here electrons, are repelled from the interface, the majorities, here holes, are attracted and form an accumulation channel (fig. 2.13 a)).

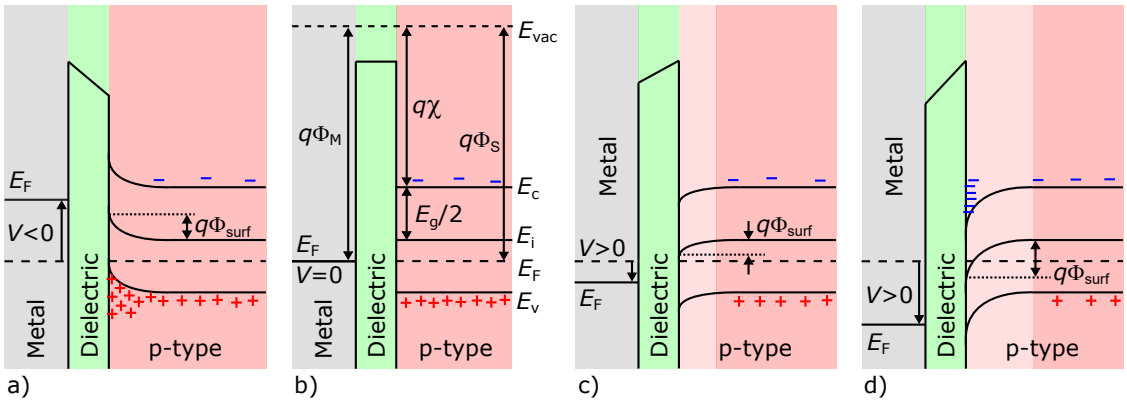

Figure 2.13: Band diagram of a MOS interface for a) accumulation, b) flat band case, c) depletion and d) inversion. For simplicity, a perfect interface without charges as well as equality of the work functions for metal $q\Phi_M$ and p-type semiconductor $q\Phi_S$ are assumed, so that the flat band voltage is $V_{FB} = 0\,V$. The lighter shaded areas in c) and d) represent the depletion region.

In the flat band case, the externally applied voltage compensates any internal bias caused by a difference between metal and semiconductor work function $q\Phi_\mathrm{M}$ and $q\Phi_\mathrm{S}$ as well as interface and dielectric charge densities. As illustrated in figure 2.13 b), this refers to $\Phi_\mathrm{surf} = 0\,\mathrm{V}$ and therefore flat bands with carrier concentrations that are identical to those in the bulk. If work function differences and interface charges are taken into account, the flat band voltage is expressed by

$$V_\mathrm{FB} = \Phi_\mathrm{M} - \Phi_\mathrm{S} - \frac{Q_\mathrm{it}}{C_\mathrm{ox}} - \frac{1}{\varepsilon_0 \varepsilon_\mathrm{S}} \int_0^{t_\mathrm{ox}} \rho_\mathrm{ox}(x) x \, \mathrm{d}x \tag{2.13}$$

with Q_it being the interface charge density at the semiconductor surface, ρ_diel the location-dependent charge density in the dielectric layer and C^*_diel and t_diel the oxide layer area specific capacitance and thickness, respectively. The work function of a metal is usually determined experimentally and obtained from a work function table. For the semiconductor, the expression

$$\Phi_\mathrm{S} = \chi + \frac{E_\mathrm{g}}{2q} + \frac{k_\mathrm{B}T}{q} \ln\left(\frac{N_\mathrm{A}^-}{n_\mathrm{i}}\right) \tag{2.14}$$

is used, where N_A^- denotes the density of ionized acceptors, n_i is the intrinsic carrier density and χ is the material specific electron affinity with 4.1 eV at 300 K for GaN.

By applying a positive voltage, band bending is reversed and holes are repelled from the interface. The consequence is the formation of a depletion region where the ionized, and thus, negatively charged acceptors compensate the positive charge at the metal electrode (cf. fig. 2.13 c)). By using the full depletion approximation, i.e. assuming a completely depleted region with well defined edges, the width of the depletion region is given by

$$w_\mathrm{depl} = \sqrt{\frac{2\varepsilon_0 \varepsilon_\mathrm{S} \Phi_\mathrm{surf}}{q N_\mathrm{A}^-}}. \tag{2.15}$$

If the positive voltage at the metal electrode is increased further, the band bending increases as well and an inversion channel forms (fig. 2.13 d)). Figure 2.14 a) shows the inversion case in more detail. Depending on the doping concentration, a difference Φ_bulk between the intrinsic Fermi energy E_i and the Fermi energy of the p-type semiconductor E_Fp exists throughout the material. The onset of inversion is defined as the point where $\Phi_\mathrm{surf} = \Phi_\mathrm{bulk}$. The semiconductor becomes intrinsic at the surface and if Φ_surf increases further, minority carriers can be generated. As long as $\Phi_\mathrm{bulk} < \Phi_\mathrm{surf} < 2\Phi_\mathrm{bulk}$, the state is defined as weak inversion. If $\Phi_\mathrm{surf} > 2\Phi_\mathrm{bulk}$, the minority carrier concentration surpasses the bulk majority carrier concentration and the state is defined as strong inversion. The corresponding potential at the metal electrode is referred to as threshold voltage V_th, the point where a MOSFET switches from off- to on-state. Note that this

is the physical definition of the threshold voltage, which usually differs from the various technical definitions. If inversion occurs, the positive charge at the metal electrode is compensated by the negative acceptors in the depletion region w_{depl} and by the electrons in the inversion channel. This circumstance is illustrated in figure 2.14 b) where charge density, electric field strength and potential are displayed along a cut line through the MOS interface for the state of inversion. The electrical aspects of the MOS inversion channel require a more technical consideration and will be discussed in section 2.6.2.

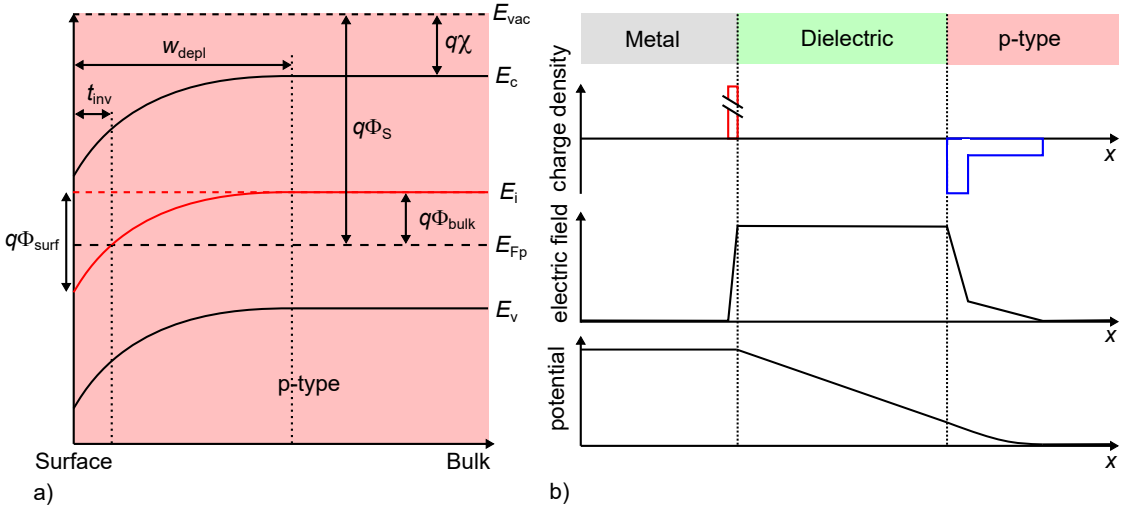

Figure 2.14: a) Band diagram for an n-type MOSFET in inversion mode. b) illustration of charge density, electric field strength and potential for a cut line across the MOS interface in inversion.

Complementary to the MOS channel and crucial during the on-state of the transistor, the current blocking depletion region is essential during the off-state. Compared to equation (2.15), which states the depletion width at a MOS interface, the depletion region in the off-state occurs at a p-n-interface and must take into account both sides of the junction. This results in

$$w_{\mathrm{depl}} = \underbrace{\sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{S}}\Phi_{\mathrm{bi}}N_{\mathrm{D}}^{+}}{qN_{\mathrm{A}}^{-}(N_{\mathrm{A}}^{-}+N_{\mathrm{D}}^{+})}}}_{w_{\mathrm{depl,p}}\text{ into the p-type}} + \underbrace{\sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{S}}\Phi_{\mathrm{bi}}N_{\mathrm{A}}^{-}}{qN_{\mathrm{D}}^{+}(N_{\mathrm{A}}^{-}+N_{\mathrm{D}}^{+})}}}_{w_{\mathrm{depl,n}}\text{ into the n-type}} \tag{2.16}$$

with the ionized acceptor and donor concentrations N_{A}^{-} and N_{D}^{+} and the built-in voltage

$$\Phi_{\mathrm{bi}} \approx k_{\mathrm{B}}T \ln\left(\frac{N_{\mathrm{A}}^{-}N_{\mathrm{D}}^{+}}{n_{\mathrm{i}}^{2}}\right). \tag{2.17}$$

Due to charge neutrality,

$$N_{\mathrm{A}}^{-} w_{\mathrm{depl,p}} = N_{\mathrm{D}}^{+} w_{\mathrm{depl,n}} \tag{2.18}$$

must hold. This means that the depletion region expands further into the lower doped side of the junction, which also causes more voltage drop across this side if the junction is reverse biased. Depending on the required accuracy, for $N_{\mathrm{A}}^{-} \ll N_{\mathrm{D}}^{+}$ or $N_{\mathrm{A}}^{-} \gg N_{\mathrm{D}}^{+}$ it can be assumed that the depletion region does only form on one side of the junction. This leads to equation (2.15) where the metal electrode at the MOS interface possesses a high charge carrier concentration so that the width of the resulting depletion region is negligible. Aspects of drift layer specification and the balancing with the adjacent p-base layer were discussed in section 2.2

2.6.2 Electrical properties of the MOSFET

Based upon the physical introduction to the MOSFET in section 2.6.1, this section expands on the electrical properties of MOS structures such as the MOSFET and the MOS capacitor. This is followed by a description of different measurement methods that were used in this work to electrically characterize such structures.

The MOSFET is defined as turned-on if the gate source voltage is above the threshold voltage $V_{\mathrm{GS}} > V_{\mathrm{th}}$. In the on-state, it is distinguished between two operation regimes, illustrated by the output characteristic in figure 2.15 a). The linear regime is characterized by a linear dependence between drain current I_{D} and drain source voltage V_{DS}, which results as an approximation for small V_{DS} from

$$I_{\mathrm{D}} = \kappa \left(V_{\mathrm{GS}} - V_{\mathrm{th}} - \frac{V_{\mathrm{DS}}}{2} \right) V_{\mathrm{DS}}, \tag{2.19}$$

with the amplification factor

$$\kappa = \frac{C_{\mathrm{diel}} \mu_{\mathrm{inv}}}{A_{\mathrm{active}}} \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \tag{2.20}$$

where C_{diel}^{*} denotes the area specific dielectric capacitance , μ_{inv} the inversion channel carrier mobility and W_{ch} and L_{ch} the channel width and length, respectively.

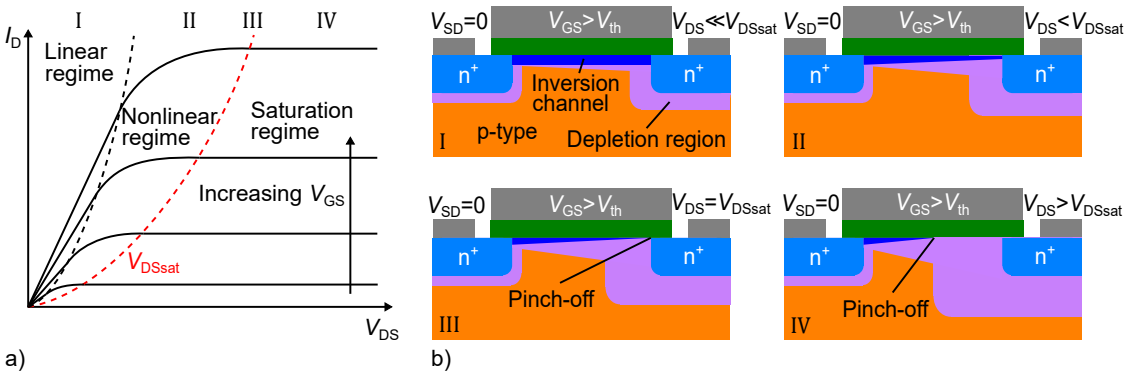

Figure 2.15: a) MOSFET output characteristic with indicated linear, nonlinear and saturation regime. b) Schematic depiction of the MOS inversion channel and depletion regions in the linear regime I, in the nonlinear regime II, at the onset of saturation III and in the saturation regime IV. The Roman numbering links the images in b) to the respective regimes and transitions in the plot in a).

The dependence (2.19) holds as long as $V_{\mathrm{DS}} \ll V_{\mathrm{Dsat}}$ with V_{Dsat} being the saturation voltage corresponding to the abscissa values of the dotted red line in figure 2.15 a) and given in [106] as

$$V_{\mathrm{DSsat}} = \frac{V_{\mathrm{GS}} - V_{\mathrm{th}}}{1 + \sqrt{\frac{q\varepsilon_0\varepsilon_{\mathrm{S}} N_{\mathrm{A}}^-}{2C_{\mathrm{diel}}^{*\,2}\Phi_{\mathrm{bulk}}}}}. \tag{2.21}$$

The importance of V_{DSsat} is emphasized by the schematics in figure 2.15 b), where its impact on the state of the MOS inversion channel is illustrated. For the linear regime, as depicted in I, an inversion channel is formed along the complete channel region. In the nonlinear regime, as V_{DS} approaches V_{DSsat}, the increased potential at the drain side of the channel compensates the gate voltage and the inversion channel carrier density decreases (fig. 2.15 b) II). At $V_{\mathrm{GS}} = V_{\mathrm{DSsat}}$, channel pinch-off occurs at the drain side and defines the onset of the saturation regime. At this point, inversion has returned to depletion and any additional potential, added at the drain side, drops across the expanding depletion region while the channel pinch-off point gradually moves toward source (fig. 2.19 b) IV). The current is then independent from V_{DS} and given by

$$I_{\mathrm{D}} = \frac{K}{2}(V_{\mathrm{GS}} - V_{\mathrm{th}})^2. \tag{2.22}$$

The operation in the saturation regime is usually not advisable since the high voltage drop across the channel leads to significant power dissipation in the MOSFET, which reduces efficiency and causes undesired generation of heat. Further increase in drain source current is only possible if V_{DSsat} is increased by raising V_{GS}. The dependence

between I_D and V_{GS} is referred to as transconductance g_m and is, in the quasi linear regime for small V_{DS}, given as

$$g_m = \frac{dI_D}{dV_{GS}} \tag{2.23}$$

From equations (2.19) to (2.22) it is apparent that a highly conductive MOSFET should feature a short channel length L_{ch} and a large channel width w_{ch}. The latter must always be considered in an area specific context, which leads to the concept of integration density. Therefore, repeating cell blocks of the MOSFET should be small so that the channel width per area is maximized. The limiting aspect in general are usually the photolithography tolerances, but the capacitance between gate and source also increases and thus must be considered as well. The later factor is irrelevant for research devices since cell dimensions are relatively large.

Another important aspect regarding current optimization, is the conductivity of the MOS inversion channel, which is defined by the mobility μ_{inv} and the density of the electrons in the inversion channel. The former depends strongly on the quality of the dielectric to semiconductor interface and will be discussed in section 2.6.4. As described in section 2.6.1, the latter depends on the band bending at the semiconductor surface and is thus affected by the gate voltage and the thickness of the dielectric layer. A way to increase the drain current is increasing the gate voltage V_{GS} while simultaneously reducing the dielectric layer thickness, i.e. increasing C^*_{diel}. This, however, results in an increase of the dielectric field strength, which in turn is limited by material properties. The fundamentals of a MOS capacitor based development of gate dielectrics will be discussed in section 2.6.5.

2.6.3 MOS inversion channel and interface

A key component of any MOSFET is the MOS inversion channel. Its origin was treated in section 2.6.1 in a theoretical manner. The MOS channel of a real device, and a GaN device in particular, deviates significantly from ideal behavior. Multiple factors affect quantities such as field distribution, carrier concentration and mobility. Apart from breakdown effects and leakage current concerning the gate dielectric, discussed in section 2.6.5, the current flow and especially the carrier mobility responsible for it, are paramount. Four aspects that affect the said mobility are considered in this work:

- Carrier scattering due to surface roughness
- Carrier scattering due to surface phonons
- Fixed interface charge density
- Interface defect populations

Carrier scattering related to surface roughness and phonons will be addresses in a qualitative manner and taken into account by adding the respective terms to the expression for the carrier mobility. The effect of interface defects and interface charge in general is particularly relevant for the devices fabricated in this work and the interface model that was used, will be laid out in more detail. A quantitative description of the respective defect and charge densities will be given in chapter 6.

Fixed oxide charges, mentioned in section 2.6.5, can be estimated from the flat band voltage. At a MOS interface, they decrease or enhance the actual gate potential depending on their polarity. The plot in figure 2.17 a) illustrates how the transfer characteristic of an n-channel trench MOSFET is affected by positive (red) or negative (blue) interface charges. Assuming an n-type MOS channel, a negative interface counters the positive gate potential and shifts the threshold voltage to more positive values. At a specified work point, this results in a reduced current flow through the inversion channel compared to a neutral interface. The opposite is true for a positive interface, which complements the gate bias and leads to strong inversion at lower gate voltage. Threshold voltage is shifted to the left and compared to the neutral interface, the current flow at a given work point is increased. If the interface charges are truly fixed and no charging or discharging occurs at high temperature and bias stress, a lower threshold voltage has the potential advantage of reduced channel resistance. The maximum applicable gate voltage is limited by the field robustness of the dielectric layer (cf. sec. 2.6.5). However, if the positive charge is located at the interface to the semiconductor or distributed within the insulator, the dielectric field strength originating from it is lower than it would be if the charges were located on the metal side of the insulator. The draw back on the other hand is the potential risk of normally-on behavior if the threshold voltage is too low.

Schematically depicted in figure 2.16 a) are the various defect bands that were implemented in this work. Located at the edges of valence- and conduction band are donor and acceptor like defect states with a tail distribution modeled as

$$\begin{aligned} g_{\mathrm{TA}} &= N_{\mathrm{TA}} \exp\left[\frac{E - E_{\mathrm{C}}}{W_{\mathrm{TA}}}\right] \quad \text{for acceptor like defects and} \\ g_{\mathrm{TD}} &= N_{\mathrm{TD}} \exp\left[\frac{E_{\mathrm{V}} - E}{W_{\mathrm{TD}}}\right] \quad \text{for donor like defects.} \end{aligned} \tag{2.24}$$

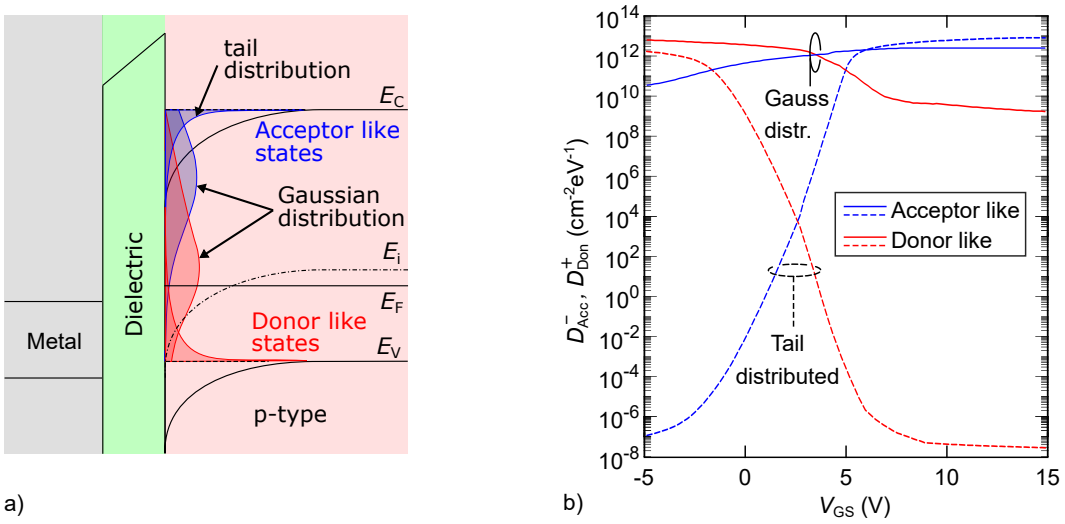

Figure 2.16: a) Schematic illustration of donor and acceptor like defect populations with tail and Gaussian distribution at a p-type MOS interface. b) Ionized interface defect states corresponding to the populations depicted in a) for different gate bias.

The peak defect density, located at the respective band edge, is denoted as N_{TA} and N_{TD} in $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ and the tail decay length is defined by W_{TA} and W_{TD} in eV. The quasi continuous distribution is modeled as 40 discrete energy levels. The other pair of defect bands is modeled as two Gaussian distributions

$$\begin{aligned} g_{\mathrm{GA}} &= N_{\mathrm{GA}} \exp\left[-\left(\frac{E_{\mathrm{GA}}-E}{W_{\mathrm{GA}}}\right)^2\right] \quad \text{for acceptor like defects and} \\ g_{\mathrm{GD}} &= N_{\mathrm{GD}} \exp\left[-\left(\frac{E_{\mathrm{GD}}-E}{W_{\mathrm{GD}}}\right)^2\right] \quad \text{for donor like defects.} \end{aligned} \tag{2.25}$$

With $N_{\mathrm{GA,GD}}$ and $W_{\mathrm{GA,GD}}$ denoting again peak concentration and width and $E_{\mathrm{GA,GD}}$ representing the energy at which the Gaussian peak is located. The latter is referenced to the conduction band edge for donor like defects and to the valence band for acceptor like defects.

Figure 2.17 shows the effect of interface charge and defects on the simulated transfer characteristic of a trench MOSFET. The plot in a) illustrates the impact of a fix interface charge and the effect of interface defects is illustrated in figure 2.17 b) and c). The difference between acceptor and donor like states is twofold. First, acceptor like states are negative when ionized, i.e. gain an electron, while donor like states become positive as they lose an electron. Second, acceptor like states are neutral if the Fermi level E_{F} is below their energy level and ionized if it is above. Donor like states on the other hand are neutral if E_{F} is above their energy level and ionized if it is below their energy level. This leads to differences regarding their impact on the transfer characteristic. As can be seen from figure 2.17 b), the impact of tail distributed donor defects is small and relatively

constant for different gate voltages. Considering the band diagram in figure 2.13 d), it becomes apparent that, at the interface and during inversion, E_F moves away from the valence band edge and gets closer to the conduction band edge. Thus the donor like defect population is mostly below E_F and therefore neutral. Its effect is restricted to the subthreshold regime where part of the tail distribution is above E_F and thus ionized. This circumstance is visualized by the plot in figure 2.16 b), where the density of ionized defects is plotted as function of V_{GS}. The amount of ionized donors in the tail distributed population decreases rapidly as V_{GS} rises and is negligible above threshold voltage. Depending on population peak density and how far it reaches into the band gap, a minor left shift due to a more positive interface at $V_{GS} \approx V_{th}$ is the observable consequence.

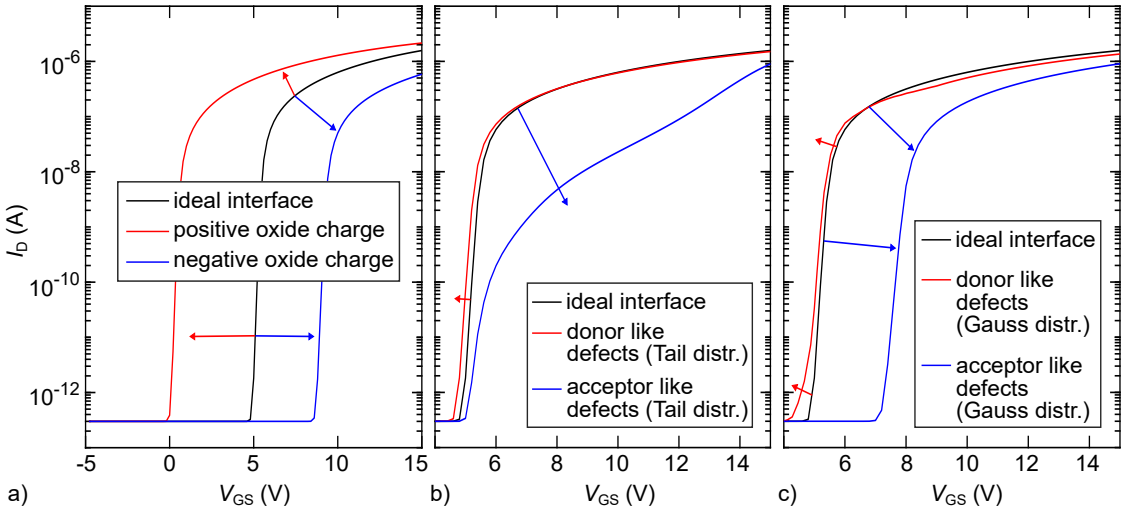

Figure 2.17: a) Effect of positive and negative fixed oxide charges on the transfer characteristic of a MOSFET. Effect on the transfer characteristic for donor and acceptor like defects with tail distribution b) and quasi uniform Gaussian distribution c).

As strong inversion occurs, the Fermi level at the interface moves towards the conduction band. This is where the tail distributed acceptors become relevant as the initially neutral defects are ionized, and thus, become negative. As shown in figure 2.16 b), with increasing gate bias the amount of ionized acceptors grows, slows down the increase of E_F and eventually leads to Fermi level pinning. This compromises the inversion effect, leads to lower channel carrier density and reduced drain current. The logarithmic plot in figure 2.17 b) illustrates the effect of the tail distributed acceptor like states on the transfer characteristic. The shift in threshold voltage is only a minor one since the defect density at this energy level is very small (cf. fig. 2.16 b)). Their impact is more pronounced as the Fermi level moves deeper into the tail distribution were the acceptor concentration is significantly higher.

The impact of Gaussian distributed populations differs from that of tail distributed defects. According to literature [107], it is useful to model the Gaussian distribution with a large width, which leads to a broad and nearly continuous defect density for donor and

acceptor like states across the band gap. This assumption, illustrated in figure 2.16 a), is based on the fact that the GaN to insulator interface must be considered as highly defective. A multitude of defect populations with various densities and energy levels leads to the described continuum. The result is a more uniform impact on the transfer characteristic, similar to a fixed interface charge. The impact of such defect populations with quasi uniform Gaussian distribution is plotted in figure 2.17 c). At low gate voltage, most of the donor population is above the Fermi level, and thus, ionized (cf. fig. 2.16 b)). The resulting positive interface character leads to a left shift of the transfer curve. However, as E_F increases and surpasses more and more of the donor energy levels, the effect decreases. If V_th is reached, a substantial amount of donor like states lies already below E_F and the impact on the interface charge density is small. The observable shift in V_th is therefore only a marginal one. For acceptor like defects, the interface character is initially slightly negative and becomes increasingly negative as E_F moves upwards, causing more acceptor states to become ionized. The result is a general right shift of the transfer curve similar to the case of a fix negative interface charge. As V_GS approaches V_th, a large and growing number of acceptor like states are ionized. Therefore, the threshold voltage shift is more prominent than for the donor like states.

To properly model a realistic MOS interface, it is necessary to account for all mentioned defect populations in conjunction with a realistic estimation for the inversion channel carrier mobility.

2.6.4 Carrier mobility in the MOS inversion channel

To adequately describe the carrier flow in a MOSFET, it is essential to consider the MOS interface. The MOS channel contributes in a considerable way to the overall resistance (cf. sec. 2.2). Therefore, an accurate description of the carrier mobility at and near this interface is mandatory. Modeling of inversion channel carrier mobility is usually based on four mobility components [96, 108]:

- Bulk mobility μ_b
- Surface phonon scattering μ_sp
- Surface roughness μ_sr
- Coulomb scattering μ_c

the total mobility is then obtained via the Matthiessen's rule as

$$\frac{1}{\mu_\mathrm{tot}} = \frac{1}{\mu_\mathrm{b}} + \frac{1}{\mu_\mathrm{sp}} + \frac{1}{\mu_\mathrm{sr}} + \frac{1}{\mu_\mathrm{c}}. \tag{2.26}$$

Starting from the bulk mobility, the model assumes a reduction of carrier mobility at the MOS channel based on factors such as the distance from the interface, the electric

field strength, carrier and doping concentration as well as interface charge and defect densities.

The expressions of the various mobility terms are stated in section 6.2 and their impact is discussed for real data along with a description of the related fitting procedure.

Concerning measurements, the true carrier mobility is usually not accessible due to its correlation with carrier density. To separate both quantities, Hall measurements are used. This technique allows to separate carrier density and mobility and is often used on planar samples. Although Hall measurements are commonly used to determine bulk mobility, gated hall structures can be deployed to obtain the carrier mobility in an inversion channel. However, if this channel is located at a trench sidewall, the required test structure becomes quite elaborated and a multitude of uncertainties arise. Therefore, the inversion channel mobility of a trench MOSFET is typically determined as field effect mobility

$$\mu_{\mathrm{FE}} = \frac{I_{\mathrm{D}}}{\frac{w_{\mathrm{ch}}}{L_{\mathrm{ch}}} C^{*}_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{th}}) V_{\mathrm{DS}}}. \tag{2.27}$$

The area specific oxide capacitance is denoted with C^{*}_{ox}, w_{ch} and L_{ch} are gate length and width, respectively. A commonly used method [109] to determine the threshold voltage V_{th}, is the linear extrapolation of the I_{DS}-V_{GS}-curve at its maximum slope. The intercept of the extrapolation with the voltage axis is then defined as V_{th}. By using this definition, equation (2.27) can be rewritten as

$$\mu_{\mathrm{FE}}(V_{\mathrm{GS}}) = \frac{g_{\mathrm{m}}(V_{\mathrm{GS}})}{\frac{w_{\mathrm{ch}}}{L_{\mathrm{ch}}} C^{*}_{\mathrm{ox}} V_{\mathrm{DS}}} \tag{2.28}$$

where $g_{\mathrm{m}}(V_{\mathrm{GS}})$ denotes the transconductance. Due to the dependence on the gate-source voltage, the resulting mobility is only reasonable where the transfer curve is close to linear, i.e. $g_{\mathrm{m}}(V_{\mathrm{GS}}) \approx$ constant. In addition, it is crucial to account for any serial resistance due to contacts, substrate and drift region, which would otherwise negatively impact the resulting channel mobility. This can be done by correcting the drain current via equation (2.29)

$$I_{\mathrm{D_{corr}}} = \frac{I_{\mathrm{D}}}{1 - \frac{V_{\mathrm{DS}}}{I_{\mathrm{D}} R_{\mathrm{serial}}}}. \tag{2.29}$$

The drain current I_{D}, measured at drain source voltage V_{DS}, is always smaller than the corrected current $I_{\mathrm{D_{corr}}}$. The serial resistance R_{serial} represents the sum of all resistance components except from the channel itself.

The field effect mobility of actual devices, as well as the simulated and calibrated channel mobility are discussed in the experimental and simulation chapter 5 and 6, respectively.

2.6.5 Methods for electrical characterization of MOS capacitors

A MOS capacitor is a relatively simple but very useful device for MOS interface examination and can act as test module during the development process. As shown in the black box in figure 2.18 a), the basic planar MOS capacitor consists of a MOS stack and a backside contact. Depending on the measurement, further features such as front side contacts in the case of low doped or p-type epitaxy as well as mesa isolation can be necessary. A variant closer to the actual trench MOSFET is the trench MOS capacitor depicted in figure 2.18 b). Crucial aspects such as the trench corner and the etched sidewall interface along with the flat but etched trench bottom are represented in this version of the MOS capacitor.

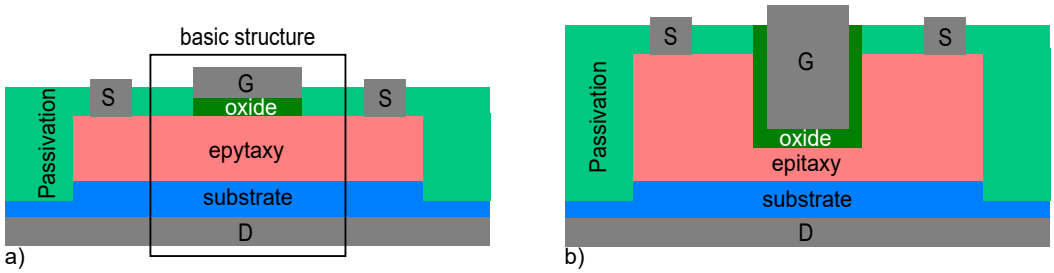

Figure 2.18: a) Planar MOS capacitor with mesa edge termination and front side contacts. The black box frames the basic structure. b) Trench version of a MOS capacitor.

Compared to a proper MOSFET, the planar MOS capacitor is easier to fabricate since less process steps are required. The essential steps for a simple planar MOS capacitor are:

- Semiconductor interface preparation.
- Deposition and post treatment of the gate dielectric.
- Deposition of the front and backside contacts.

The semiconductor layer system of the MOS capacitor is also simpler than for a MOSFET and consists only of the substrate and one optional epitaxial layer on top, depending on the interface that is to be examined. The following characteristics can be measured at a MOS cap:

- Forward and reverse breakdown voltage and peak electric field strength for the gate dielectric.
- Forward and reverse leakage current through the gate dielectric.
- capacitance voltage (CV)-measurements to determine the flat band voltage, interface and oxide defects as well as the dielectric constant of the deposited dielectric.

The following paragraphs will briefly cover the basics necessary for the mentioned measurements.

Current voltage measurement: Several relevant characteristics of a MOS capacitor can be obtained from a current voltage (IV)-curve. Measuring the current voltage characteristic of a MOS capacitor yields information about the breakdown field strength E_B of the dielectric, leakage current through the dielectric and, in combination with additional surface examinations, gives insight to surface characteristics of the semiconductor and the interface quality in general.

Commonly used dielectrics such as silicon dioxide, silicon nitride or aluminum oxide are insulating materials with very low electrical conductivity. However, several conduction mechanisms can become relevant if the layer thickness is small, which is usually the case in MOS capacitors. Some of the most relevant mechanisms [110] are

- Direct tunneling
- Several types of defect assisted hopping or tunneling
- Schottky Emission
- Pool-Frenkel Emission
- Fowler-Nordheim tunneling

Figure 2.19 illustrates these conduction mechanisms by means of band diagrams for a metal insulator semiconductor stack.

Direct tunneling (fig. 2.19 a)) occurs only for very thin layers, that is below 4 nm. Therefore, it is not relevant for the samples examined in this work, which possess layer thicknesses of at least 30 nm. The same is true for types of trap assisted hopping or tunneling. As long as the dielectric layer is intact, no significant number of bulk defects and traps is to be expected in the dielectric and the related conduction mechanisms can usually be neglected.

Schottky emission occurs when thermally activated electrons overcome the electric barrier of the insulator as illustrated in figure 2.19 b), and thus, is relevant at elevated temperatures. Even though this mechanism is unlikely to have an effect on the measurements performed in this work, the Pool-Frenkel Emission, a combination of field assisted tunneling and Schottky Emission, must be considered as a relevant conduction mechanism. As illustrated in figure 2.19 c), for Pool-Frenkel Emission, electrons that overcome the barrier, are trapped at sites inside the dielectric. The present electric field lowers the barriers, and thus, increases the probability for the electrons to be released and to move towards the positive electrode.

According to [111], the current density is given as

$$I_{FP} = qN_C\mu_{diel}E_{diel}\exp\left[-\frac{q}{k_BT}\left(\Phi_T - \sqrt{\frac{qE_{diel}}{\pi\varepsilon_0\varepsilon_{diel}}}\right)\right] \tag{2.30}$$

with the semiconductor conduction band density of states N_C, the electronic drift mobility in the dielectric μ_{diel}, the field strength in the dielectric layer E_{diel} and the trap barrier height Φ_T.

The second relevant conduction mechanism is field assisted tunneling, also known as Fowler-Nordheim tunneling, schematically depicted in figure 2.19 d). This effect becomes relevant at high electric field strength and is therefore essential during the robustness measurements in this work. The Fowler-Nordheim current density is given in [112] as

$$I_{FN} = \frac{q^2 E_{diel}^2}{16\pi^2 \hbar \Phi_B} \exp\left[\frac{-4\sqrt{2m^*_{diel}}(q\Phi_B)^{3/2}}{3\hbar q E_{diel}}\right] \tag{2.31}$$

where Φ_B is the barrier height at the dielectric interface and m^*_{diel} is the effective electron mass in the dielectric.

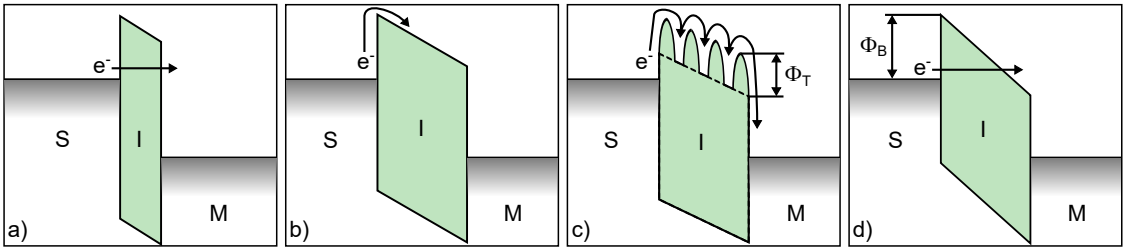

Figure 2.19: Band diagrams for conduction mechanisms through dielectric layers (I) between semiconductor (S) and metal (M). a) Direct Tunneling, b) Schottky Emission, c) Pool-Frenkel Emission and d) Fowler-Nordheim Tunneling.

None of the mentioned conduction mechanisms should play a relevant role during normal MOSFET operation. That means, the measured gate leakage current is dominated by measurement noise as illustrated by the IV-curve in figure 2.20 a) for the low voltage regime (I). For increasing gate bias, usually j_{FN} becomes dominant and leakage current increases (region II). Eventually, the dielectric is damaged and current rises drastically until fatal breakdown occurs (region III). The gate bias limit as well as the approximated dielectric field strength $E_{diel} = (V_G - V_{FB})/t_{diel}$ are vital parameters for sustainable MOSFET operation and can also be obtained from IV-measurements on MOS capacitors.

Capacitance voltage measurement: An important parameter in the MOSFET equations in section 2.6.2 is the dielectric capacitance C_{diel}. An ideal MOS capacitor can be described by an equivalent circuit consisting of a fix oxide capacitance C_{diel} connected in serial with a voltage dependent semiconductor capacitance $C_S(V_G)$. The total capacitance is therefore

$$C_{tot}(V_G) = \left[\frac{1}{C_{diel}} + \frac{1}{C_S(V_G)}\right]^{-1} = \frac{C_{diel} C_S(V_G)}{C_{diel} + C_S(V_G)}. \tag{2.32}$$

The semiconductor capacitance depends on the measurement frequency that is the alternating component superimposed on the sweep voltage. This is due to the relation to the depletion region at the semiconductor surface, which can be approximated according to [106] as

$$C_{\mathrm{S}} \approx \sqrt{\frac{\varepsilon_0 \varepsilon_{\mathrm{S}} q p_{\mathrm{p0}}}{2\Phi_{\mathrm{surf}}}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{S}}}{w_{\mathrm{depl}}} \quad \text{for} \quad (2\Phi_{\mathrm{bulk}} > \Phi_{\mathrm{surf}} > k_{\mathrm{B}}T/q) \tag{2.33}$$

with the p-type bulk carrier concentration p_{p0}.

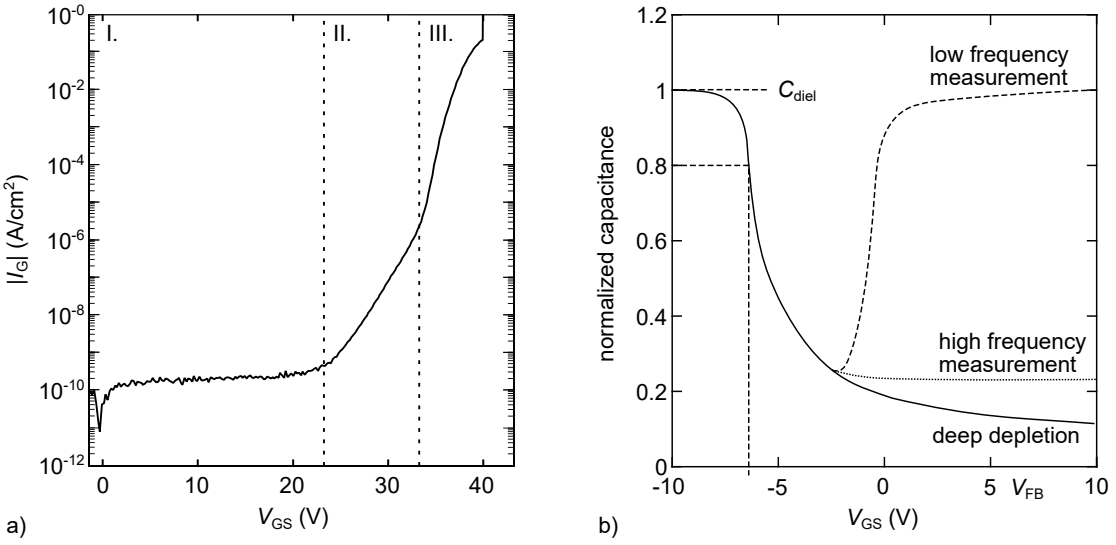

Figure 2.20: a) IV-curve of a planar MOS capacitor. b) CV-curve of a p-type MOS capacitor normalized to the capacitance dielectric layer C_{diel} for low and high frequency measurement.

Assuming a p-type semiconductor, a negative gate voltage causes, as depicted in figure 2.13 a), accumulation of holes, i.e. majority carriers. Thus the gate charge is compensated at the semiconductor-oxide interface, the total capacitance reaches its maximum as C_{S} can be omitted and $C_{\mathrm{tot}} = C_{\mathrm{diel}}$ holds. This circumstance is depicted in the plot in figure 2.20 b) where a theoretical CV-curve, normalized to the dielectric capacitance, is shown. At this point, it is possible to calculate the relative dielectric constant of the deposited insulator as

$$\varepsilon_{\mathrm{r}} = \frac{C_{\mathrm{diel}} t_{\mathrm{diel}}}{\varepsilon_0} \tag{2.34}$$

where t_{diel} denotes the thickness of the dielectric layer.

For increasing gate voltage, accumulation is reduced, the flat band state is reached and eventually inversion occurs. The arising depletion region acts as the capacitance C_{S}, which decreases during the expansion of the depletion region. However, as minority carriers accumulate near the semiconductor surface, part of the gate charge is compensated

and C_{tot} increases. At this point, the measurement frequency becomes important. If the frequency is low, the minority carriers have enough time to be generated and to recombine. An inversion channel is formed and the main part of the gate charge is compensated at the interface. Thus, C_{S} becomes negligible and for strong inversion $C_{\mathrm{tot}} \approx C_{\mathrm{diel}}$ holds. If the frequency is high, minority carriers cannot respond fast enough so that any alternating gate charge is compensated by a response of the majority carriers at the border of the depletion region, which leads to a expansion or contraction of the same. The result is a low C_{S}, and thus, a low C_{tot}. A special case arises if the sweep speed is so fast that the minority carriers are unable to follow, which then leads to so called deep depletion where the complete gate charge is compensated by a wide depletion region.

The shape of a measured CV-curve, or more precisely its deviation from the theoretical curve, can be used to characterize the interface regarding charge and defect density. Two common measurement methods are the quasi static CV-measurement QSCV-measurement and the high frequency CV-measurements HFCV-measurement.

Although CV-measurements are not a focus of this work, the QSCV-measurement will be briefly introduced since quantities such as flat band voltage and oxide capacitance were obtained via this method.

The basic definition of capacitance is the ratio between a change in charge and the change in the voltage causing it. The QSCV-method measures this differential capacitance from the charge $\Delta Q_{\mathrm{G}}(V_{\mathrm{GD}})$ that is added to the gate at a certain V_{GD} if the gate voltage is increased by ΔV_{G}.

$$C_{\mathrm{QS}}(V_{\mathrm{GD}}) = \frac{\Delta Q_{\mathrm{G}}(V_{\mathrm{GD}})}{\Delta V_{\mathrm{GD}}} \tag{2.35}$$

The current flow is monitored and an increasing voltage step is only applied after the current has dropped below a specified level. This assures that no more charging of interface states and parasitics takes place. The charge flow, immediately after the next voltage step, is then used to calculate the quasi static capacitance at this bias level.

The charges and traps that can be present at the MOS interface and in the dielectric can be allocated to the following categories [113].

- Fixed oxide charges: Located in the oxide but near the interface to the semiconductor, these charges are typically positive and incorporated during the fabrication process. Their effect is usually a shift of the flat band voltage.
- Mobile oxide charges: These charges are commonly caused by Na^+, Li^+ or K^+ and are also introduced during the fabrication process.
- Oxide trapped charge: Electric fields can cause electrons or holes to enter the dielectric during device operation. The carriers are trapped and cause, similar to the fixed charges, a voltage shift. They are usually distributed throughout the oxide.

- Interface trapped charge: Located at the oxide-semiconductor interface, these charges are attributed to dangling bonds.

3 Gate trench development

This chapter treats the development and fabrication of trenches in gallium nitride and expands on the published work [114]. The trench fabrication procedure, including structure requirements and processing of the mask stack is described, followed by a description of the main etching process. Also discussed are trench requirements concerning geometry and interface roughness, which leads to the post treatment in alkaline solution and wet etching of various GaN crystal facets. Finally, an optimized fabrication procedure, including a trench size reduction is presented. The demonstrated trenches are the basis for the trench MOS capacitors treated in chapter 4 and also for the trench MOSFETs that will be discussed in chapter 5.

3.1 Trench fabrication

In this section the requirements for the trench and the trench mask are discussed and motivated. Furthermore, the trench fabrication via dry etching is described in detail. This includes the actual etching procedure and a discussion regarding the trench geometry.

3.1.1 Requirements for trench structure and fabrication process

Apart from fabrication aspects such as feasibility and reproducibility, there are three predominant requirements for the gate trench in a trench MOSFET:

- Good MOS interface quality, i.e. low surface roughness and defect density for low gate leakage current and high channel mobility
- Rounded features and an overall smooth and homogeneous geometry to avoid field peaks and to obtain high voltage robustness in the on- and off-state
- A trench width that is as small as possible in order to achieve a small cell pitch and high integration density

The last requirement is mostly important for industrialization but is of minor scientific interest. Deviations from an ideal cell pitch can always be accounted for in calculations. Therefore, the focus in this work is the quality of the sidewall interface and the smoothness of the trench bottom. The specific geometrical requirements for the trench as manufactured in this work, are a width of 2-3 µm and a depth of 1-1.5 µm. A width of 3 µm or below is a process requirement for the recess gate described in section 4.2.1.

The trench depth results from the combined thickness of n-source and p-base layer and takes process tolerances into account. The trench sidewall is desired to be vertical, which has two advantages. First, a vertical sidewall results in the smallest cell pitch and the shortest possible channel length for a given trench depth. Second, the crystallography of GaN allows a nearly perfect alignment of trench sidewall and certain crystal planes. This in turn can be advantageous for the surface quality of the sidewall in terms of roughness and defect density. The fabrication method of choice for the trench is ICP dry etching as introduced in section 2.5. The necessary structured mask layer, which in the following will simply be referred to as a mask, must also fulfill certain requirements, the most relevant being:

- Highly anisotropic etching of the mask must be possible to obtain a high aspect ratio. This is necessary since erosion of the upper mask corner is inevitable during the aggressive GaN etching process and leads to a gradual widening of the mask opening. This in turn requires a relatively thick mask layer, to achieve the mentioned high aspect ratio.
- A low etch rate during the aggressive trench etching process to minimize edge erosion, to maintain the designated trench width and to obtain steep trench side walls.
- Thermal stability during the GaN etching process.
- Chemical stability during the wet etching post treatment.
- The mask should be metal-free to avoid contamination of the semiconductor interfaces. Although this is not a mandatory requirement, in the context of a metal-free gate-first process it is important for consistency.

The dry etching tool in this work is an ICP tool of the model APS from SPTS Technologies. The absence of chlorine gas requires, as described in section 2.5, highly physical etching conditions for the dry etching of the trench. This rules out a mask based on photoresist since the erosion would be too high. Since a choice was made to avoid metal masks, silicon dioxide is a viable option. It can be deposited quickly by means of plasma enhanced chemical vapor deposition (PECVD) for non-electrical test structures or gentle and with higher quality by low pressure chemical vapor deposition (LPCVD) (cf. appendix A.1). It has high thermal stability, is robust against physical etching and has a low etch rate in SF_6 chemistry. Lastly, it is practically inert in TMAH and can be etched in HF-solution, which in turn does not etch GaN. This means the mask residues after the dry etching can protect the GaN during subsequent wet etching in TMAH and can be removed in HF solution without affecting the refined GaN trench. Since native GaN substrates are only available in 2" diameter a carrier wafer was required for this specific etch tool. The carrier acts as spacer between the GaN substrate and the chuck, which reduces the cooling efficiency significantly and leads to much higher temperatures during the etching process. Although this might be beneficial to the GaN etching process, other

steps such as etching of the mask by means of a lithographically structured photoresist layer depend on low temperatures during the etching (sec. 2.5).

3.1.2 Fabrication of the mask stack

In accordance with the requirements and challenges described above, a three layer mask stack was chosen. Figure 3.1 illustrates the corresponding fabrication process. The SiO_2 mask is 3 µm thick so that trench widening effects due to corner erosion are minimized. Since this thick SiO_2 layer must be etched with high aspect ratio at relatively high wafer temperature, a resist mask is not suitable. A layer of 1 µm amorphous silicon (aSi) was added to solve this problem. The thinner aSi layer was etched by using photoresist under low power etch conditions to avoid burning of the resist.

The first step in the mask structuring process sequence is the lithography. A contact lithography tool was used to generate 1 to 2 µm wide lines in the 1 µm thick photoresist. The so structured resist layer was used as the mask to structure the aSi cap layer underneath by using a low power etching process. The corresponding parameters are stated in table 3.1. The SF_6 molecules are dissociated into fluorine radicals and SF_x monomers. The fluorine radicals adsorb to the aSi surface and react with the silicon atoms to form SiF_4, which then desorbs.

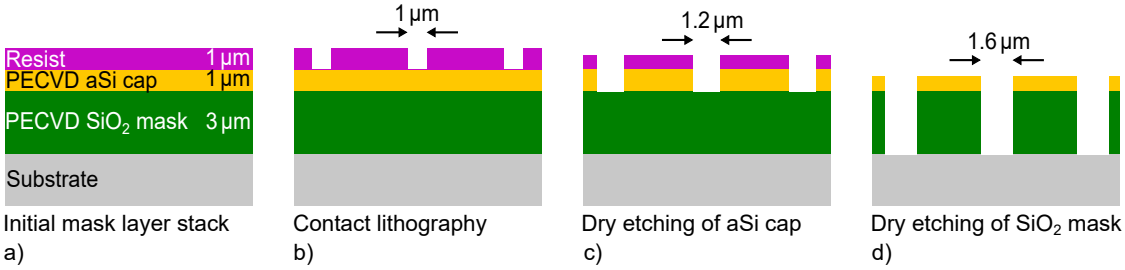

Figure 3.1: Schematic depiction of the mask layer stack used for the GaN trench fabrication process.

Generally, low coil and platen power in combination with a slow switching process consisting of a 25 s pause sequence between 5 s etching intervals, prevented burning or deformation of the photoresist and resulted in steep and narrow openings in the aSi cap layer. The scanning electron microscopy (SEM) image in figure 3.2 a) shows the aSi opening after the etching process with a width of $\approx$ 1.2 µm. The resist layer shows only minor deterioration at the sidewalls.

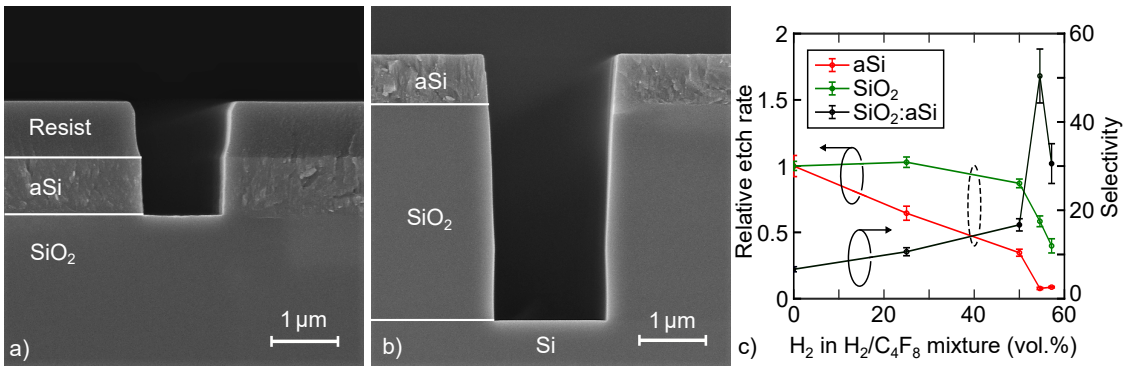

Figure 3.2: SEM images of the mask stack after the aSi cap etching a) and after the subsequent SiO_2 etching b). The plot in c) shows the etch rate for aSi and SiO_2 for different concentrations of H_2 relative to the etch rate without H_2 addition. The dashed circle indicates the configuration that was used for the actual process.

After the aSi etching, the resist is stripped since it is not needed anymore and would burn during the subsequent etching of the SiO_2 layer. Although the aSi cap is more resilient than photoresist, the etching of 3 µm of SiO_2 at elevated temperature would lead to deterioration of corners and sidewalls, which in turn affect the width and steepness of the opening in the SiO_2 mask. Therefore, a switching process was also used in this step. Prior to the etching itself, a 6 inch silicon wafer with thermal oxide was etched for 60 s to pre-condition the etching chamber. The actual etching was performed with the parameters stated in table 3.1, the result is presented in figure 3.2 b). Etching intervals of 5 s were separated by 10 s pause sequences. The etch chemistry is based on C_4F_8, which is dissociated into fluorine radicals $F^\bullet$ and $C_xF_y^+$ monomers. According to [97] the etching proceeds as follows. The monomers adsorb to the SiO_2 surface and further dissociate. Since C-O bonds are stronger (358 kJ/mol) than Si-O bonds (318 kJ/mol), the latter are broken and substituted. The resulting CO then desorbs from the surface. The fluorine radicals attach to the silicon atoms and form SiF_4, which also desorbs. Free fluorine radicals, that are present in the gas phase, can attach to the aSi surface, form SiF_4 and thus cause unintended etching of the aSi mask. This process can be suppressed by the introduction of hydrogen. The H_2 molecules are dissociated in $H^\bullet$ radicals, which bind with the $F^\bullet$ radicals to form HF. This gathering of fluorine radicals reduces the etch rate of aSi significantly and increases the selectivity of this process. The plot in figure 3.2 c) shows a decreasing aSi etch rate if more H_2 is added to the gas mixture. The SiO_2 etch rate remains relatively constant for low and medium H_2 concentrations, which leads to a significant increase in selectivity. The etching parameters were kept constant at the values stated for the SiO_2 mask etching process in table 3.1.

The platen power was relatively high and the process thus yielded an opening with nearly vertical sidewalls. As can be seen in figure 3.2 b), the aSi layer thickness is still close to its initial value and deterioration occurred only at the corners and sidewalls. This led to a general widening of the opening in the SiO_2 layer and a slight angle of the sidewalls in

the upper part. The opening depicted in figure 3.2 b) is the starting point for the trench etching, which will be described in detail in the next section.

Note that the elaborated mask stack, i.e. the additional aSi cap and corresponding process steps, is a consequence of the insufficient cooling of the GaN substrate in this particular ICP tool. Processing in a 2 inch tool or processing on 6" wafers, would simplify the procedure.

Table 3.1: Etching parameters for the dry etching steps in mask and trench fabrication.

Etching step	Coil-/platen power (W)	Platen DC bias (V)	Chamber pressure (mTorr)	Gas flow (sccm)	Etch time	Etch rate (nm/min)	Selectivity
aSi cap	400/60	130	15	300 He, 8 H_2, 20 SF_6, 8 C_4F_8	5 s etch, 25 s pause, 36 cycles	55	5 to resist
SiO_2 mask	2000/715	390	5	240 He, 15 C_4F_8, 10 H_2	5 s etch, 10 s pause, 65 cycles	185	17 to aSi
GaN main etching	1100/900	590	10	10 Ar, 35 SF_6	1.25 min	900-1100	3-4 to SiO_2
GaN soft etching	550/250	480	10	10 Ar, 35 SF_6	2 min	100	0.1 to SiO_2

3.1.3 Fabrication of the gate trench by plasma etching

As discussed in section 2.5, a chlorine based gas mixture is generally preferred for GaN dry etching due to the relatively low boiling point of the etch product $GaCl_3$. The use of SF_6, results in the non-volatile etch product GaF_3, which needs to be removed by means of sputter desorption. This requires highly physical etching and was, in this work, achieved by using high platen power and argon as stabilization gas. A strike phase that lasted 5 s with 25 mTorr chamber pressure was used to stabilize the plasma during ignition. After that, the process was performed under a lower chamber pressure of 10 mTorr. As stated in table 3.1, only 10 sccm argon were added to the reactive gas, which is a considerably lower amount of stabilization gas than used during the previous mask etching steps. The low chamber pressure in combination with high platen DC bias achieved a high etch rate of $\approx 1\,\mu m/min$ in GaN. Figure 3.3 shows SEM images of trenches and sidewalls that were etched under different process conditions. The result of the etching after 75 s GaN main etching (cf. tab. 3.1) is illustrated in figure 3.3 b). A trench depth of 1.7 µm was achieved with a sidewall steepness of $\approx 80°$. The predicted erosion of the mask corners as well as a widening of the opening are also apparent. The redeposition at the lower

part of the mask flank consists of GaF_3, which was confirmed by using energy-dispersive X-ray spectroscopy (EDX). The related measurements are presented in figure 3.16 and will be discussed in section 3.2.3. Figure 3.3 a) shows a wide opening and the specimen was prepared in such a way that the backside is visible along with the sidewall of the left flank. The redeposited layer of GaF_3 is observable with a sharp border at the transition between mask and GaN. This indicates that etching is still ongoing at the GaN surface and GaF_3 is successfully removed at the trench sidewall and bottom. The magnifications in figure 3.3 a') and b') show small grooves in the sidewall. As indicated by the red arrows in fig. 3.3 a), irregularities in the GaF_3 redeposition layer correlate with the larger clusters of sidewall grooves further down. In addition to the sidewall grooves, the most apparent feature is the mictrotrench at the base of the sidewall. Microtrenching is usually attributed to charged sidewalls [115] and specular reflection [116–118]. A large ratio between high energy ions and chemically active radicals leads to anisotropic etching but also facilitates microtrenching. A high platen DC bias leads to a negatively charged surface, which in turn attracts the positive ions. Although this is the basic idea of directional etching, it can cause problems in narrow structures with high aspect ratios such as a trench. As the positive ions enter the trench, they get attracted towards the negative sidewall. If these ions are reflected at grazing angles, their energy is mostly conserved. This can lead to the ion flux being focused to the area at the base of the sidewall [115]. The effect is enhanced if the sidewall of the mask is slightly inclined [116]. Two criteria, large flux of high energy ions and slightly inclined mask sidewalls, fit the etching process for the GaN trench and lead to the observed effect of microtrenching. A more negative potential of the insulating SiO_2 mask compared to the conductive GaN underneath is also likely and the effect cannot be diminished. Lower ion energy, i.e. less platen power is not feasible as GaF_3 would build up and stop the etching process. And a vertical sidewall of the mask would, even if achievable, be deteriorated quickly.

The reason why microtrenches should be avoided was already quickly addressed at the beginning of section 3.1 and will be discussed here in more detail. The first problem that can originate from a microtrench, is inhomogeneous covering during the deposition of the gate dielectric. If the dielectric is thinner at some places, or features a void at the interface to metal or semiconductor, this spot is prone to electrical breakdown. Furthermore, even if the dielectric is deposited homogeneously, a disproportionately high electric field strength is inherent to the geometry of the microtrench. The plot in figure 3.4 a) illustrates the maximum electric field strength versus trench corner radius. Figure 3.4 b) shows the two dimensional field distribution for various corner radii and structures with and without a microtrench. The simulation assumes a 50 nm thick SiO_2 layer as gate dielectric and a 100 V potential difference between semiconductor and gate electrode. The field strength in the dielectric was extracted as maximum value from the corner region and the area at the bottom with no curvature. The plot shows data for simulations with and without microtrenches and indicates a radius of $r_{\mathrm{trench}} \geq 100\,\mathrm{nm}$ as desirable for the trench geometry in order to avoid high field strength in the gate dielectric. Although the

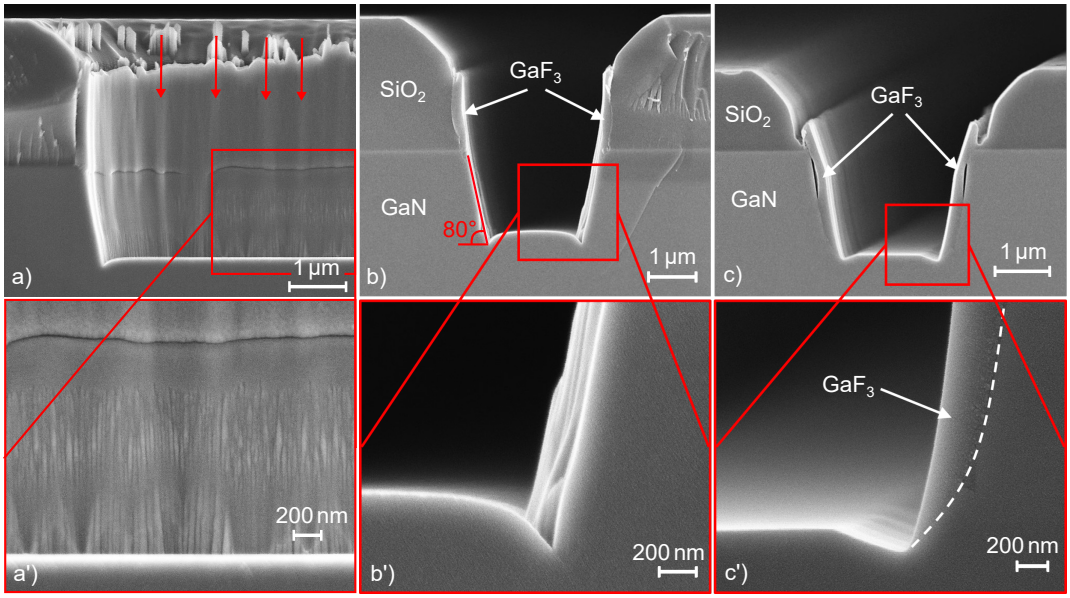

Figure 3.3: a) SEM image of a wide opening after the GaN main etching process (tab. 3.1) with focus on the backside. The red arrows indicate slight irregularities in the redeposited GaF_3 layer at the lower part of the mask flank, which correlate with clusters of grooves in the GaN trench sidewall, magnified in a'). b) SEM cross section of a 1.7 µm deep trench after the GaN main etching process fabricated with a 2 µm lithography mask. c) Trench structure from b) after the additional GaN soft etching step with rounded microtrenches and GaF_3 deposition along the complete trench sidewall. Reproduced from [114], with the permission of the American Vacuum Society.

structures with microtrench show an overall higher field strength at the trench corner, the simulation also shows clearly the necessity to avoid small radii in general.

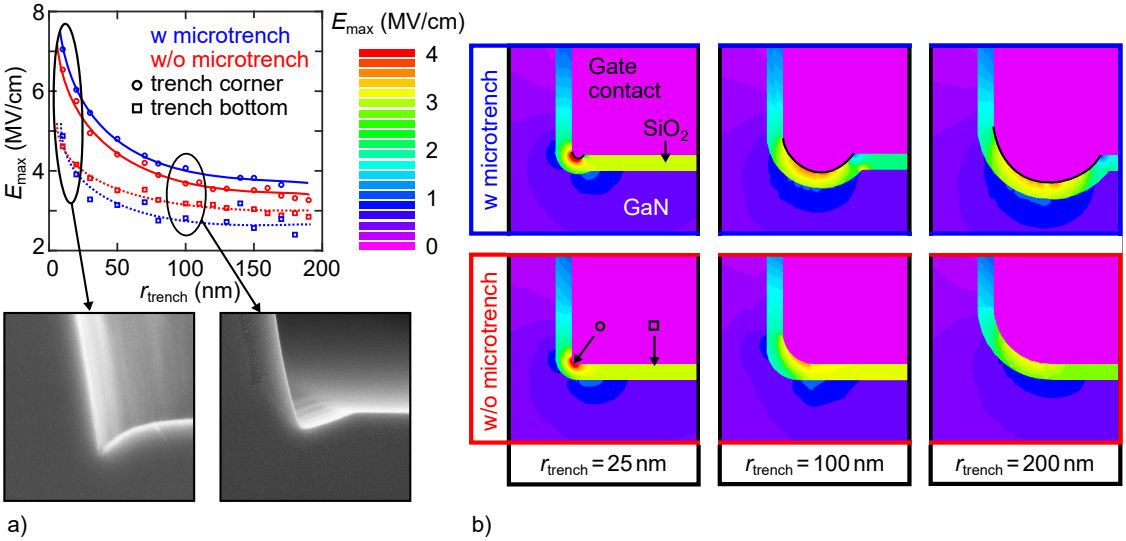

Figure 3.4: a) Maximum electric field strength in the 50 nm thick SiO_2 layer for 100 V potential difference between gate electrode and semiconductor. The circles and squares are related to the locations indicated in the color plots in b). b) Electric field strength for a geometry with and without microtrench, shown for three different values of the trench corner radius r_{trench}.

As stated above, diminishing of microtrenches by a reduction of the amount of physical etching is not viable for SF_6 based etching. The plot in figure 3.5 shows the GaN and SiO_2 etch rate versus the platen power as well as the corresponding selectivity. If platen bias is reduced, the selectivity between GaN and the SiO_2 mask drops significantly and prevents the fabrication of a deep and narrow trench with steep sidewalls. The solution is the trench fabrication with high platen power in combination with a subsequent soft etching step. The parameters for the soft etching are given in table 3.1. Less platen power and more chamber pressure decrease the ion energy and lead to a rounding of the microtrenches. This can be seen in figure 3.3 c). However, along with rounder microtrenches, severe redeposition of GaF_3 and a considerable deterioration of the SiO_2 mask are consequences as well. The selectivity of the process drops to only 0.1 and even after 2 min process time, the trench depth has only marginally increased.

Although the soft etching step lead to diminished microtrenches and trench corner radii in the range of 100 nm as desired, the redeposited GaF_3 is not tolerable at the trench sidewall since this is going to be the future MOS interface. In addition, the sidewall angle is still only $\approx 80°$. Both problems can be addressed by a wet etching post treatment, which will be described in the following section.

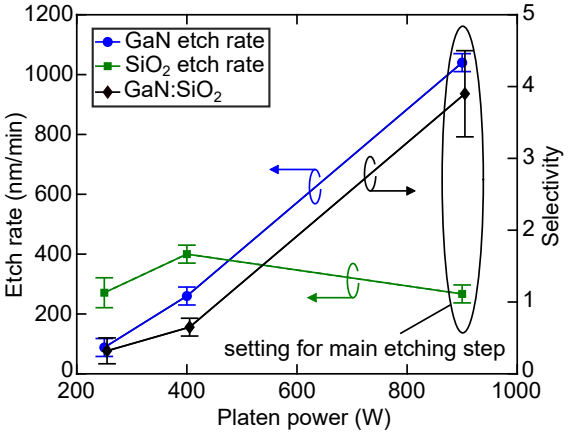

Figure 3.5: GaN and SiO_2 etch rate for the GaN main etching process if only platen power is changed. All other process parameters are identical to those stated for the main etching procedure in table 3.1. While the GaN etch rate drops with decreasing platen power, etching of the SiO_2 mask is mostly independent from this parameter. This leads to a significant decrease in selectivity for low platen power.

3.2 Wet etching post treatment of the gate trench structure

According to the etching barrier theory, introduced by Lai et al. [64] and discussed in section 2.5, the c^+-plane features the largest *EBI* and should be practically inert against alkaline etchants. Along with the polar c^+-plane, the nonpolar a- and m-planes have the highest *EBI*s, which means that these planes should occur during wet etching since the inclined s-planes are etched much faster. Such a behavior is advantageous as

it allows a quasi self aligned fabrication of a vertical and crystal plane oriented trench sidewall. It should be noted that this is only true for trenches fabricated on Ga-face GaN where the c^+-plane constitutes the horizontal surface. However, since Ga-face is the commonly used orientation, this restriction is only a minor one. If the wafer has said Ga-face orientation and therefore the horizontal surface is the inert c^+-plane, the trench depth remains practically unchanged as semiconductor material is etched in lateral direction. This circumstance is illustrated in figure 3.6. Image a) shows the trench after dry etching as described in section 3.1.3 with the redeposited GaF_3 indicated exemplarily for one sidewall in orange. Together with a significant amount of GaN (outlined in blue), the GaF_3 is removed during wet etching. This alters the lateral dimension of the trench as well as the inclination of the sidewall, which is now vertical and, depending on the alignment of the trench, oriented along the a- or m-plane of the GaN crystal. The removal of a significant amount of GaN also leads to the removal of defects and impurities that were generated and incorporated during the preceding plasma etching in the vicinity of the etched surface. Therefore, the resulting trench sidewall is a wet etched surface, which is beneficial as it represents the interface for the MOS inversion channel.

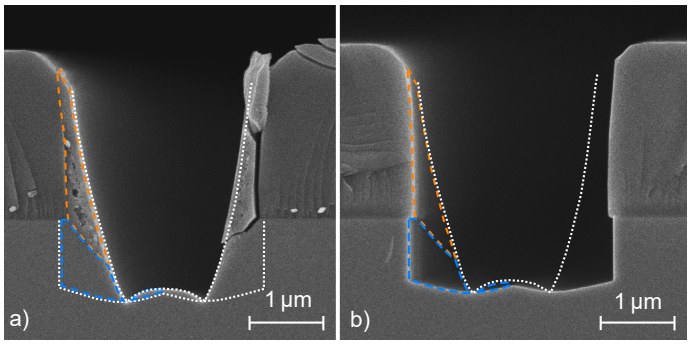

Figure 3.6: a) SEM image of a plasma etched trench. The orange line indicates GaF_3 redeposition at the trench sidewall. The white outline represents the shape of the trench before and after subsequent wet etching while the blue outline indicates the section of semiconductor material that is removed during wet etching. b) SEM image of the trench in a) after 30 min in 25 % TMAH solution at 90 °C with the white dotted line representing the trench shape prior to wet etching.

Several questions arise from figure 3.6 and will be discussed in section 3.2.1:

- What is the surface orientation of the trench sidewall after wet etching?
- What are the requirements for the plasma etched trench regarding alignment and initial geometry to provide a good starting point for the wet etching procedure?
- What role does the SiO_2 mask play during the wet etching process?

A fourth point, the effect of plasma- and subsequent wet etching on the surface quality and electrical properties of the GaN interface, will be discussed in section 4.3 in the next chapter.

3.2.1 Wet etching of the vertical crystal planes in GaN

To examine the etching of GaN trench sidewalls in KOH and TMAH, square structures with side lengths between 25 and 200 µm were etched approximately 2 µm deep into two samples of Ga-face GaN by using the main and soft dry etching steps stated in table 3.1. After the dry etching, one sample was etched for 40 min in 25 % TMAH at 60 °C, the other one was etched for 30 min in 33 % KOH at 80 °C. Both concentrations refer to a solution in water. By examining the corner of a square, all three relevant planes, i.e. c^+-, a- and m-plane can be observed and compared to each other for the exact same etching condition.

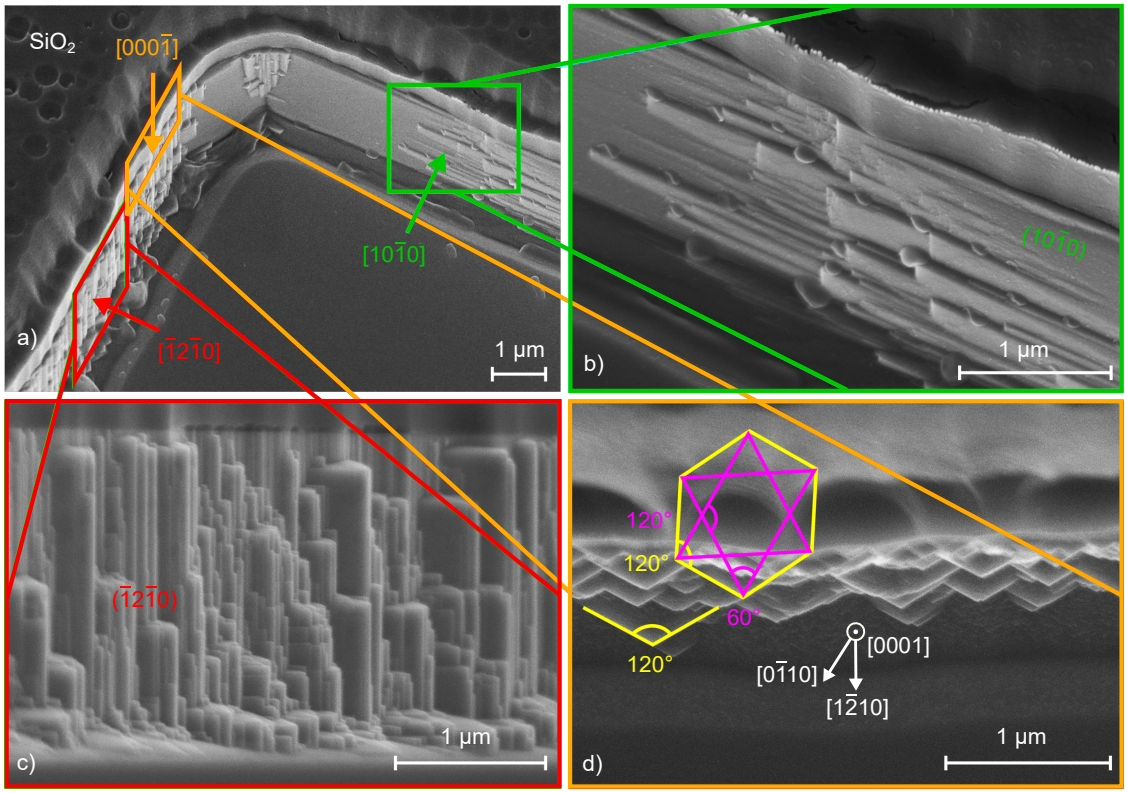

Figure 3.7: Corner of a square that was fabricated by dry etching and wet etching post treatment in 25 % TMAH for 40 min at 60 °C. Image a) shows the overview of the corner, b) is a zoom-in on the m-plane and c) a zoom-in on the a-plane. d) Is the top view on the a-plane sidewall. Reproduced from [114], with the permission of the American Vacuum Society.

Figure 3.7 a) shows a SEM image of a square corner for the sample treated with TMAH. The bottom of the structure, i.e. the c^+-plane, is completely smooth. By using a profilometer and by comparing SEM cross sections before and after the wet etch treatment, it was found that the depth of the structure did not change due to wet etching (cf. also fig. 3.6). The fact that the c^+-plane is not wet etched is important due to two reasons. First, it assures that the trench depth does not change during the treatment which makes the process more controllable. Second, it allows the formation of vertical sidewalls in parallel to the a- and m-planes of the GaN crystal. In the following, this inherent

process of preparing wet etched surface in parallel to crystal planes will be denoted as self-alignment. As will become clear from a wet etching experiment on N-face GaN, described in section 3.2.2, the absence of an inert horizontal plane, that prevents etching in vertical direction, leads to the formation of inclined semipolar s-planes. In this case, a trench with vertical sidewalls cannot be fabricated in a self aligning manner. However, if the inert c^+-plane is present, vertical sidewalls are formed during wet etching.This can be seen from figure 3.7 and especially 3.8, the latter showing the same situation as figure 3.7 but after a 30 min wet etching in 33 % KOH at 80 °C.

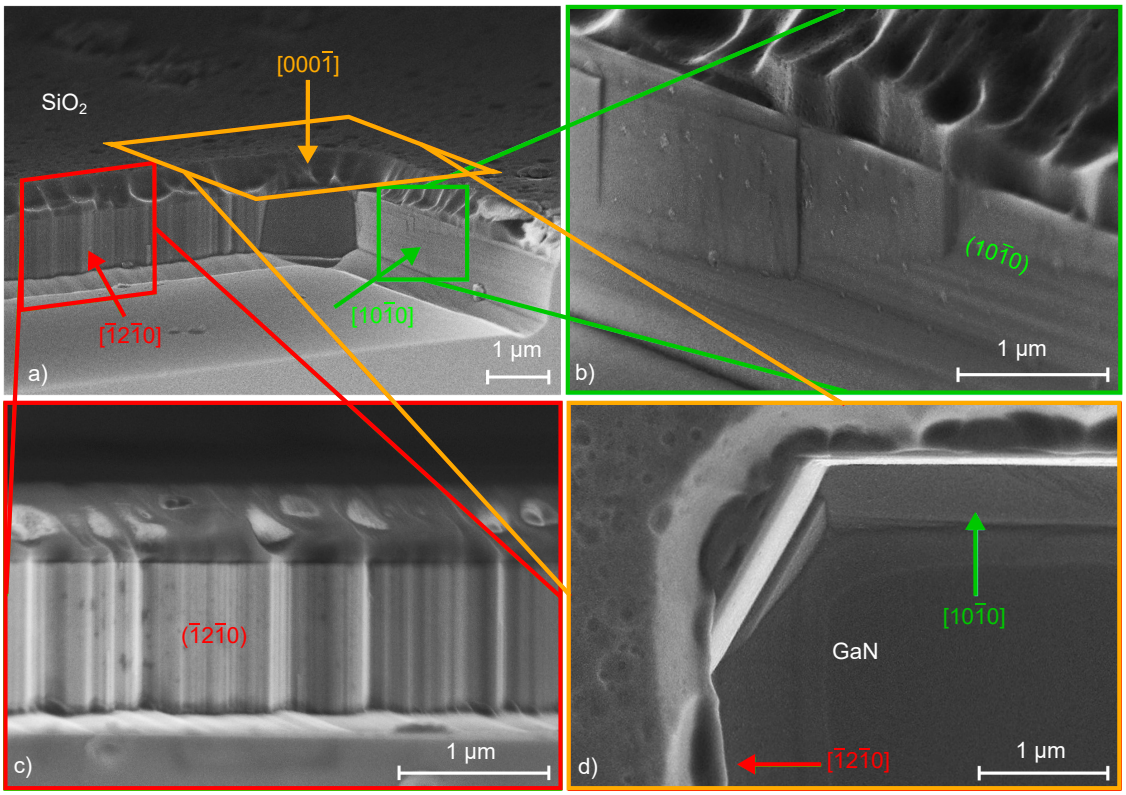

Figure 3.8: Corner of a square that was fabricated by dry etching and wet etching post treatment in 33 % KOH for 30 min at 80 °C. a) is the overview while b) and c) show the zoom-in of m- and a-plane, respectively. Image d) shows the top view for the corner. Reproduced from [114], with the permission of the American Vacuum Society.

The interface parallel to the m-plane shows a smooth surface and is practically vertical close to the corner of the square (cf. fig. 3.7). However, the zoomed image in figure 3.7 b) shows step-like structures that occur further away from the corner. The steps themselves have a perfectly plane surface and are caused by misalignment of the trench, as well as a not perfectly vertical sidewall after the dry etching process. During longer etching or etching with higher etch rate, the steps are gradually leveled out. This results in a smooth m-plane surface. There are two reasons for the occurrence of these steps. The first one is illustrated schematically in figure 3.9 a). It can be seen that misalignment of the trench in horizontal direction causes steps that tend to compensate the deviation from the crystal plane. Note that the schematic in figure 3.9 a) is exaggerated for illustrative reasons. The

second reason is the initial inclination of the trench sidewall after plasma etching. While the remaining SiO_2 mask pins the upper trench corner and prevents further etching in lateral direction, the lower part of the sidewall is etched and retracts gradually while revealing the vertical facets of the m-plane (fig. 3.9 b)). A similar phenomenon occurs for the a-plane shown in figure 3.7 c) and figure 3.9 c). Although the surface properties are different, the mechanism that transfers the inclined trench sidewall into a vertical one, is the same. The height of the pillars in figure 3.7 c) correlates with the steepness of the sidewall. Low pillars at the bottom are etched away and higher pillars occur as the sidewall gradually retracts during the etching process. Eventually, the sidewall becomes vertical as is the case after the KOH etching in figure 3.8 c). As shown in figure 3.9 c), the top of the pillars is the flat c^+-plane. Since this plane is inert, the height of the pillars does not change as they are etched only in lateral direction. Note that the sidewalls of the pillars are not the expected a-plane. As can be seen in the lower image in figure 3.9 c), the revealed planes are inclined and do not form a plain surface. To avoid distortion of length and angles, it is advisable to observe the structure in two dimensions as done in figure 3.7 d). The top view shows the hexagonal shape of the pillars protruding from the sidewall. The measured angle of the corner is 120°, which indicates the visible planes as inclined m-planes, indicated by the yellow hexagon. This hexagon represents the top view of the GaN unit cell. If the planes were a-planes, the measured angle would be 60° as shown by the magenta colored star. The reason why inclined m-planes and not the expected a-plane is visible, lies in the lower EBI of said a-plane (cf. tab. 2.2 and fig. 2.10 c)). The plane with the highest EBI is etched at the lowest rate and will eventually be revealed while faster etching planes disappear.

The SEM images of the second sample, etched in KOH at higher temperature and depicted in figure 3.8, show a more advanced state of the etching process. Only some shallow steps are visible at the m-plane sidewall in b) and the irregularities at the corner of the square are also eliminated. The a-plane sidewall is now vertical although, the surface is still rippled. Interesting is the higher etch rate in the a-direction. As can be seen in the top view in figure 3.8 d), the m-plane sidewall is just visible as a bright line at the edge of the SiO_2 mask while the a-plane has retracted so far underneath the SiO_2 mask, so that it is no longer visible. This can be explained by the rougher surface, which allows faster etching as two sides of the pillars are etched simultaneously.

So far it has been shown that after wet etching, surface conditions along the a-plane differ significantly from those along the m-plane. This circumstance is interesting in the way that atomic force microscopy (AFM) measurements of an a-plane surface that was subjected to equal TMAH wet etching, revealed no such difference. Figure 3.10 shows 5x5 µm tapping mode AFM scans of cross sections for samples that were cleaved along the a- and m-plane and measured before and after TMAH wet etching. Images a) and b) show the m- and a-plane before any treatment. The RMS roughness is in both cases below 0.2 nm, which is close to the resolution limit of the measurement tool. The near vertical lines in image a) represent steps of m-plane plateaus that occur with irregular spacing.

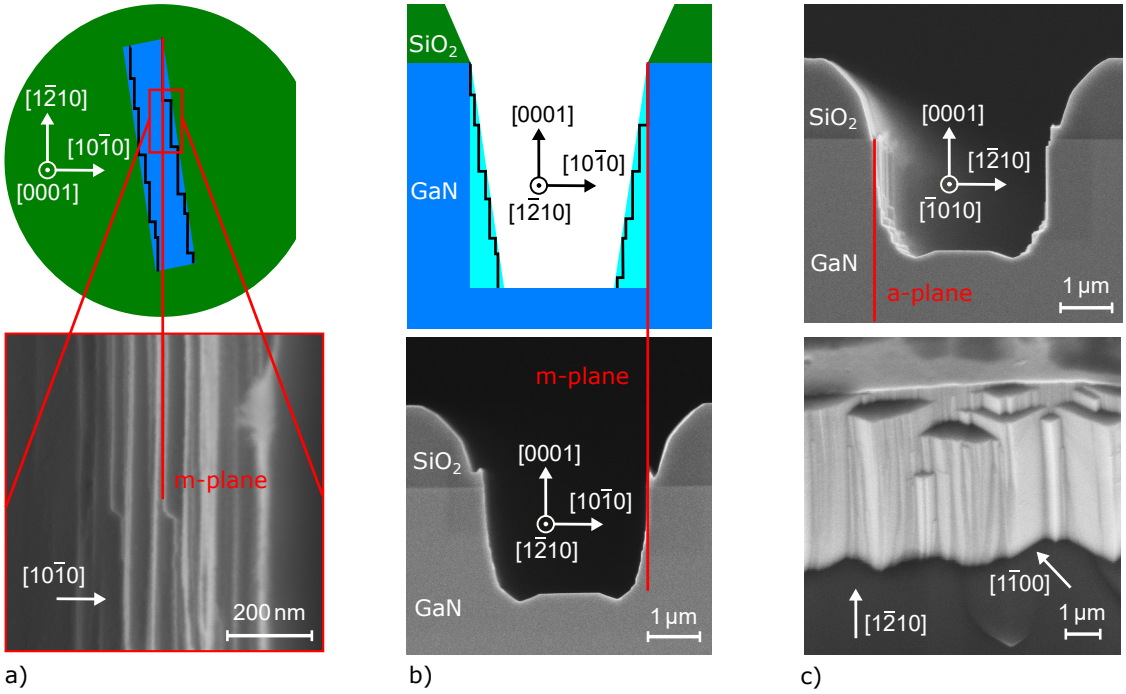

Figure 3.9: Illustration of the step wise etching of GaN in alkaline solutions. a) Exaggerated schematic of steps in horizontal direction at the m-plane sidewall due to trench misalignment with a corresponding SEM image below. b) Schematic of vertical step formation at the non-vertical m-plane sidewall with the corresponding SEM image below. c) SEM images of a trench with a-plane sidewall (top) and an a-plane sidewall revealing m-plane facets after wet etching (below).

Note that these steps are very flat and not comparable with those at the trench sidewall displayed in figure 3.7 b). The equidistant lines, running under an angle of approximately 45 °, must be regarded as a measurement artifact. The image in b) shows the scan for an a-plane surface, where a multitude of stripes suggests the absence of a coherent crystal plane. However, the roughness is extremely low and comparable with that for the m-plane orientation in a). After wet etching in TMAH at 90 °C for 30 min, the m-plane surface features a patchy appearance but roughness is still close to the resolution limit. For the a-plane surface, the TMAH etching reveales the vertical stripes as shown in d). The surface resembles that at the trench sidewall in figure 3.8 c). The roughness however, is only 0.39 nm, meaning that this surface would appear almost featureless during SEM examination and the protruding corners observed in figure 3.7 would not appear for this sample. To find the reason for the significant difference between the a-plane surface at a trench sidewall and the one on the sample in figure 3.10 d), the structures displayed in the SEM image in figure 3.11 were fabricated and examined as follows. A SiO_2 mask was deposited on the sample, then removed in square shaped areas and GaN trench etching was performed. Subsequently, the sample was cleaved, wet etched in TMAH and the cross-section was examined at the fringe of a square. From the SEM image a) in figure 3.11 and the related AFM scan in a'), it becomes clear that the cross sectional surface area only shows excessive roughness if the related top side surface was either

exposed to plasma etching, or not covered by the SiO_2 mask. As demonstrated in image b), the effect reaches about 100 µm deep until it gradually levels out. As expected, the depth down to which the effect reaches, correlates closely with the time of the wet etching treatment. In this case, 100 µm for 30 min etching at 90 °C in 25 % TMAH. From the height indication of the AFM scans it becomes clear that the rougher surface is etched significantly faster.

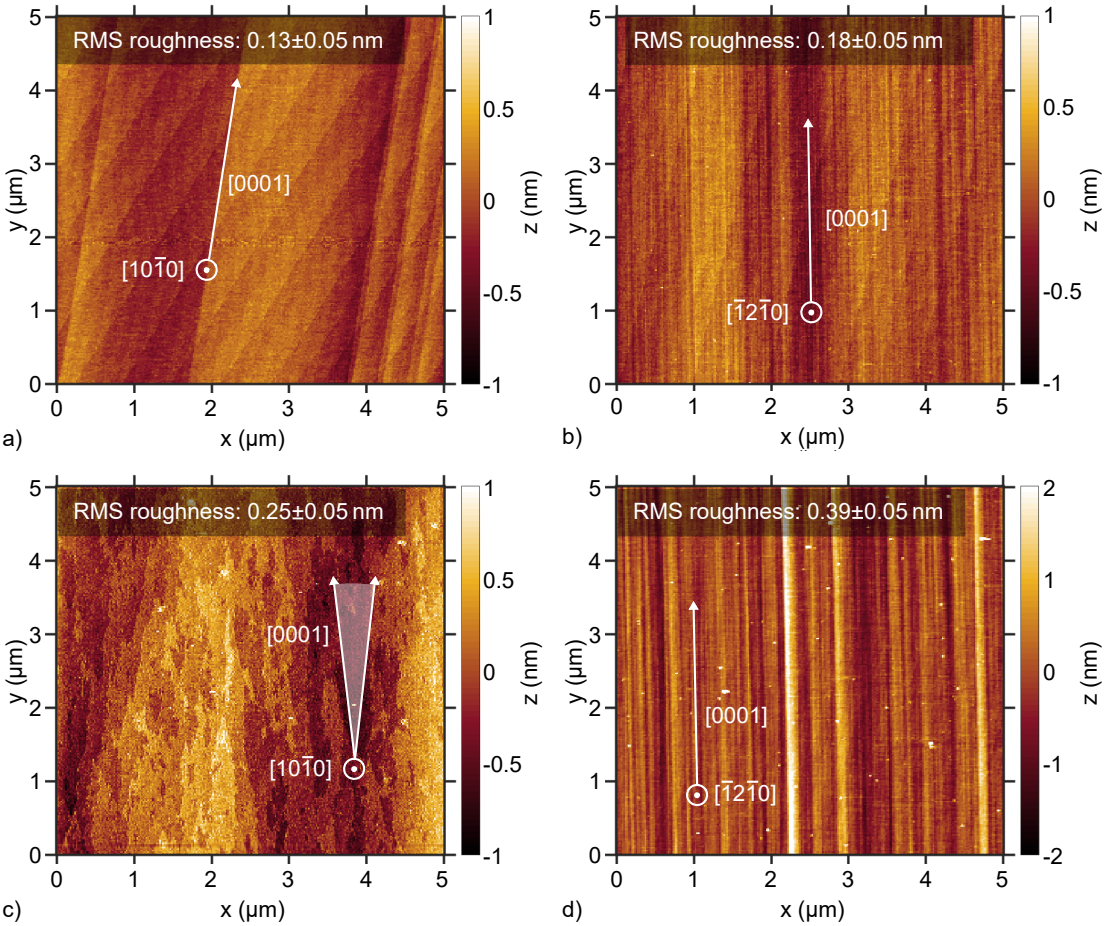

Figure 3.10: a) AFM scan of an untreated m-plane surface obtained by cleaving a GaN sample. b) Untreated a-plane surface. c) m-plane surface after a 30 min treatment in 90 °C TMAH. Due to a lack of representative features, the crystal orientation cannot be determined precisely, but the [0001]-direction is known to be close to the y-direction. d) a-plane surface after TMAH wet etching. The bright spots in c) and d) are due to particle contamination.

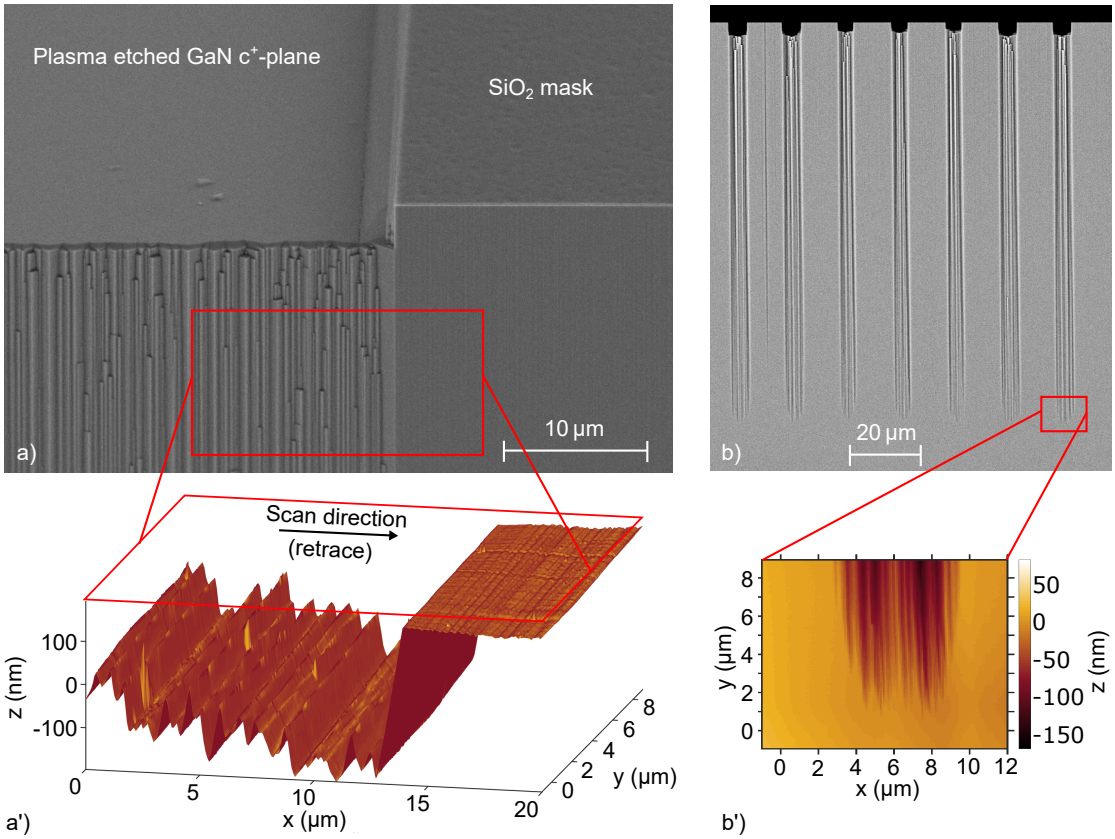

Figure 3.11: a) SEM image of an a-plane cross section at the transition between an etched surface on the left and an unetched surface, covered by SiO_2 on the right. The red box indicates, true to scale, the location where the AFM scan, displayed in a'), was performed. b) Shows the extend of the surface anomaly caused by trenches at the top. Again the red box is a true to scale marker for the AFM scanning area. The corresponding data is plotted in b').

The observations so far suggest two possible explanations for this phenomenon. The first one is an altered interface at the top side surface due to plasma etching. Impurity incorporation and generation of defects could weaken the crystal structure and either cause a different surface after the sample is cleaved, or result in better access for OH^- groups, leading to an increased etch rate. The second explanation is related to the absence of the SiO_2 mask in the areas where the rougher and faster etched surface is observed. It is known that the SiO_2 pins the GaN crystal at the interface during wet etching to a certain degree [65]. This is verified by the SEM image in figure 3.6 b), where the top corner of the trench is kept fix by the SiO_2 mask, while a considerable amount of GaN is etched in lateral direction at the bottom region. A simple way to determine which mechanism is the root cause for the phenomenon, observed in figure 3.11, is to remove the SiO_2 layer after the sample was cleaved, but prior to TMAH treatment. If the excessive roughness is still observed, crystal damaging by plasma etching as well as effects of mechanical stabilization by the SiO_2 layer during the cleaving procedure can be ruled out since the SiO_2 layer was still present during both steps. Figure 3.12 presents SEM images for a sample with SiO_2 capping in a) and without in b). The results demonstrate

that the SiO_2 being present during wet etching is indeed the decisive factor. If the mask is kept in place, as was done in image a), the area between the trenches remains comparably smooth. If the mask is removed as was the case for the sample in image b), the complete cross sectional surface is affected. The AFM scan in c) shows, once again, the deep recess caused by wet etching. The two smooth areas to the left and right allow reasonable good data leveling, so that a cut-line can be used to extract the inclination angle of the protruding structures (fig. 3.12 d). Although the large topography reduces the measurement accuracy, the more reliable retrace scan reveals inclination close to 30 °. This supports the presumption from the SEM image in figure 3.7 d), that the observed facets represent two m-planes inclined towards each other.

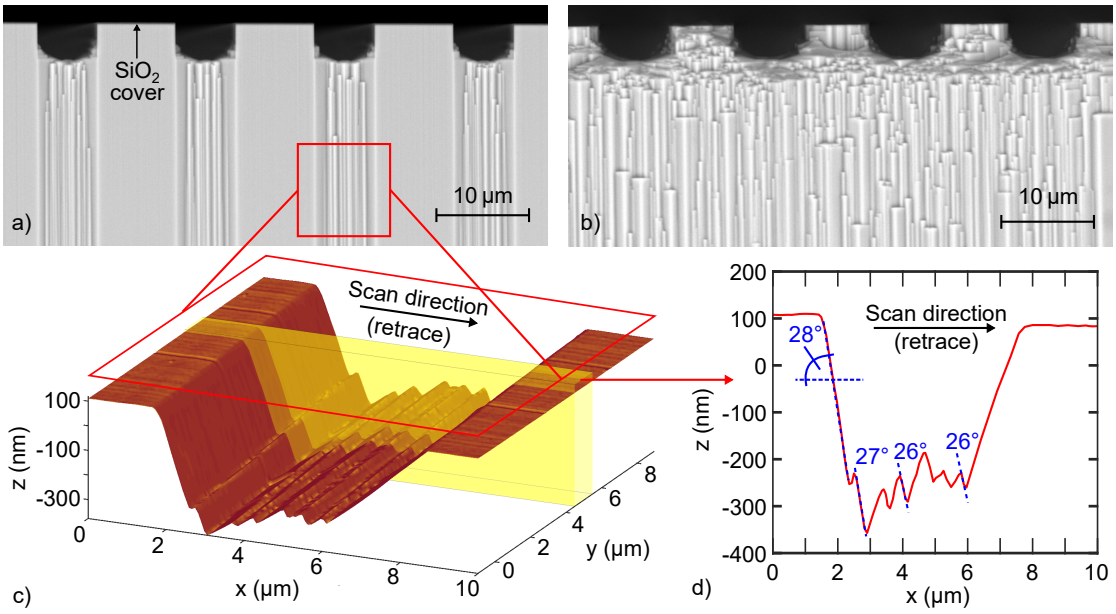

Figure 3.12: a) SEM image of an a-plane cross section after TMAH wet etching. Note that, although not visible, a layer of SiO_2 is still present on the topside surface where no trenches were formed. b) a-plane cross section surface after TMAH wet etching without SiO_2 mask ton the top side surface. c) AFM scan conducted on the 10x10 µm indicated by the red box in a). d) Cut line along the x-direction of the AFM scan in c) with data averaged along a width of 1 µm in y-direction indicated by the yellow box.

It should be noted that the differences between the TMAH- and KOH-etched surfaces in figures 3.7 and 3.8 are not due to the etch chemistry but due to the etch time and etch rate. Indeed, it could be shown that smooth and vertical sidewalls can also be obtained by using TMAH at 80 to 90 °C. The difference in the images of figures 3.7 and 3.8 is due to the difference in temperature and the difference in etch rate resulting thereof. The experiment showed that, by using TMAH or KOH, vertical sidewalls and smooth m-planes can be fabricated and the results are in good agreement with the *EBI*-theory. The inert c^+-plane on the Ga-face inhibits vertical etching, and thus, prevents the formation of vertically inclined planes. This is advantageous for the trench formation and the

reason why vertical sidewalls are formed. However, to further support the findings and explanations, observation of inclined planes would be useful. An additional experiment, conducted on N-face GaN, revealed such inclined semipolar crystal planes and will be discussed in section 3.2.2.

3.2.2 Wet etching of N-face GaN

The lower *EBI* of the c^--plane, compared to the c^+-plane, allows vertical wet etching of the N-face so that a simple, mask-free treatment in TMAH or KOH already leads to distinguishable features. The occurring structures are hexagonal pyramids with sides aligned along the m-plane. The SEM image in figure 3.13 shows such pyramids that formed after 10 min in 25 % TMAH at 105 °C. Measuring the angle of the pyramid edge yields $\alpha = 62° \pm 0.5°$. The line of view is exactly along the a-axis, i.e. the $[1\bar{2}10]$ direction, which means that α corresponds to the angle illustrated in the schematic in figure 3.13 b). Checking table 2.2 gives the s_5-plan as unambiguous solution. The only other plane with an angle close to 60° is the s_2-plane, which is oriented along the a-plane, and therefore, can be ruled out. The *EBI* of the s_5- and c^--plane have the highest values after c^+-, a- and m-plane. The c^+-plane can obviously never occur on N-face GaN and the a- and m-planes cannot form because, compared to the c^+-plane, the c^--plane is not inert and by being etched, prevents the formation of any vertical structures. Note that areas of c^--plane are present along with the s_5-facets of the pyramids, as shown in figure 3.14 a). This is in good agreement with its slightly higher *EBI* compared to the s_5-plane. Apart from pyramids with perfect s_5-facets, several unfinished pyramids with 12 facets are present as well. As indicated in figure 3.14 c), the pyramids feature six additional facets that are rotated by 30°. Although the angle cannot be measured accurately, a comparison to the already determined s_5 plane shows that it is slightly less than 61.7°. This would fit the 58° of the s_2-plane, which is oriented along the a-plane, explaining the 30° rotation to the other facets. Eventually, the s_2-planes are etched away, leaving only the s_5-planes, as shown in figure 3.14 b). Note that unlike the Ga-face surface, the N-face surface is etched continuously. This is true for all the occurring crystal planes. The gradual etching and the small difference between the *EBI* values, lead to coexistence between c^--, s_5-, s_2-planes and other planes as well.

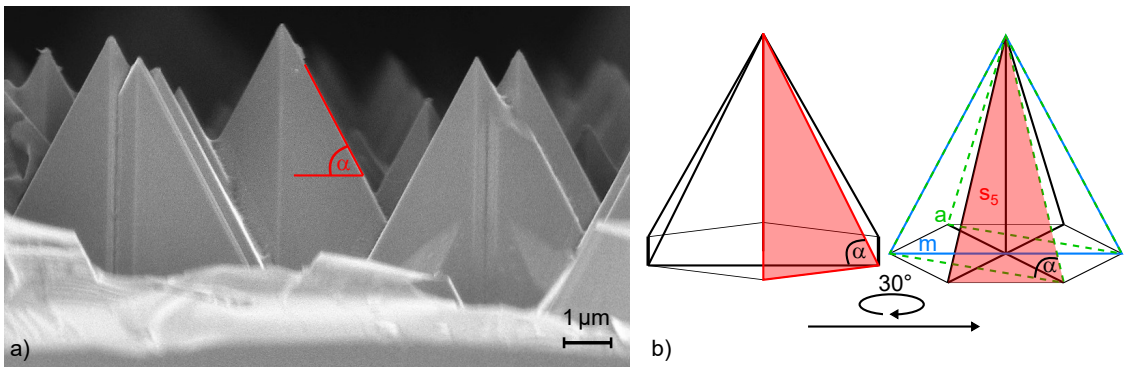

Figure 3.13: a) SEM image of N-face GaN after etching in 25 % TMAH for 10 min at 105 °C. The line of view is exactly the $[1\bar{2}10]$ direction so that the left and right side facets of the hexagonal pyramids are not visible. This allows an accurate measurement of the indicated angle α, which resulted in $62° \pm 0.5°$. b) Schematic drawing of the hexagonal pyramid for an s_5-plane surface.

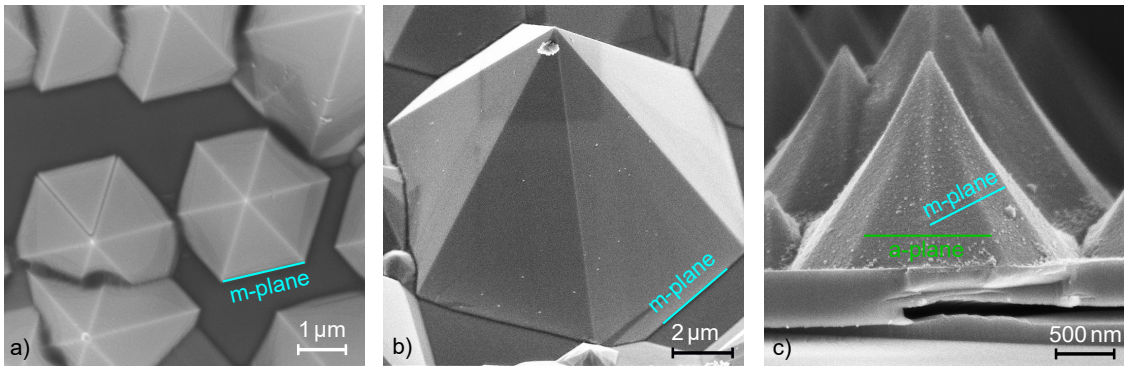

Figure 3.14: a) Top view on an N-face GaN surface after 10 min etching in 25 % TMAH at 50 °C. The dark area is the horizontal c^--plane with hexagonal pyramids protruding from it. b) Hexagonal pyramid with s_5-plane facets as determined by the angle measurement in figure 3.13. c) Twelve sided pyramid after 10 min etching in 25 % TMAH at 30 °C. The line of view is again along the $[1\bar{2}10]$ direction as in figure 3.13.

Short etching or lower temperature tends to yield more diverse structures and reveals the actual formation process of the pyramids. As shown in figure 3.15 a) a large number of small pyramids is present at the beginning of the etching process. During the course of further etching, the larger pyramids start to dominate while the smaller structures disappear. This is most likely due to facets with lower *EBI* and a generally larger surface. Even though samples feature more large and regular pyramids after high temperature etching (cf. fig. 3.14 a) and b), irregularities do still occur. As illustrated in figure 3.15 b), various facets and competition between different pyramids are also observable after etching at elevated temperature. This can be attributed to the constantly changing surface as more and more GaN is etched away. Remnants on the surface, as well as any defects or impurities in the crystal itself, do probably affect the etching procedure. Comparisons between samples etched with TMAH or KOH again showed no significant difference. The fabricated pyramids were similar in shape and size for identical etching conditions.

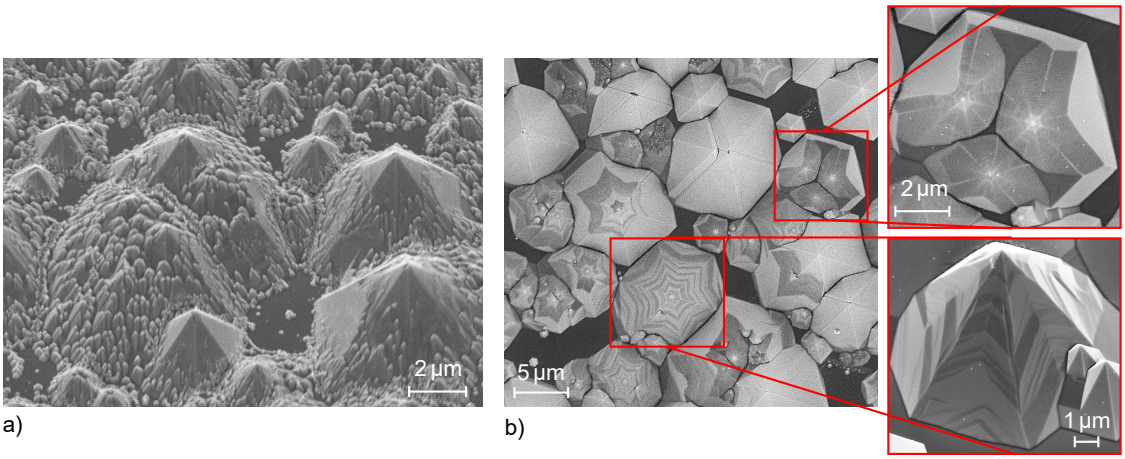

Figure 3.15: a) N-face GaN surface after 10 min etching in 25 % TMAH at 20 °C. b) N-face GaN surface after 10 min etching in 25 % TMAH at 105 °C.

3.2.3 Wet etching of trench structures in GaN

The true purpose of TMAH and KOH based wet etching of GaN is the refinement of dry etched trenches. To improve geometry and interface conditions, the following aspects need to be addressed:

- Removal of GaF_3 that was redeposited during the dry etching process.
- Increasing the sidewall steepness and creating a crystal plane oriented surface.
- Further reduction of microtrenches and creation of a concave trench bottom.
- Removal of GaN from the sidewall to create a wet etched interface without defect or impurity incorporation caused by high energy dry etching.

Removal of GaF_3: To confirm the existence of GaF_3 or GaF_x [62] in the redeposited layer, formed during the dry etching (cf. fig. 3.3), EDX measurements were carried out. Figure 3.16 depicts the relative counts of five different measurements. Position 1 is the mask flank after the main etching step where, as described in section 3.1.3, an observable layer of redeposition is located. The plot in figure 3.16 b) shows a noticeable peak at 0.675 keV indicating fluorine. The peak height corresponds to 2.2 ± 0.05 mass percent. The measurements at positions two and three revealed lower fluorine concentrations of 1.15 ± 0.04 and 0.61 ± 0.03 mass percent for sidewall and bottom, respectively. The largest amount of fluorine, with 12.82 ± 0.09 mass percent, was found at the sidewall after the soft etching step. A measurement at the trench bottom after the soft etching step (data not shown in fig. 3.16 b)) gave a peak corresponding to 1.12 ± 0.04 mass percent fluorine. These numbers confirm the assumptions that were made based on the thickness of the redeposited GaF_3 layer. They also reveal that, even though not visible with the SEM itself, the trench bottom does feature GaF_3 residues. The last measurement was performed on the sidewall of a sample that was wet etched for 10 min in 25 % TMAH

at 50 °C after the main and soft dry etching. The resulting EDX spectrum shows no detectable signal for fluorine and the analysis yielded no result for the fluorine mass percentage. Within the accuracy of the EDX system the GaN surface can be stated as free of GaF_3 after only ten minutes in TMAH at intermediate temperature. Since the actual trench refinement procedure consists of longer etching at higher temperature, it can be assumed that the samples will be completely free of GaF_3 after the wet etching procedure.

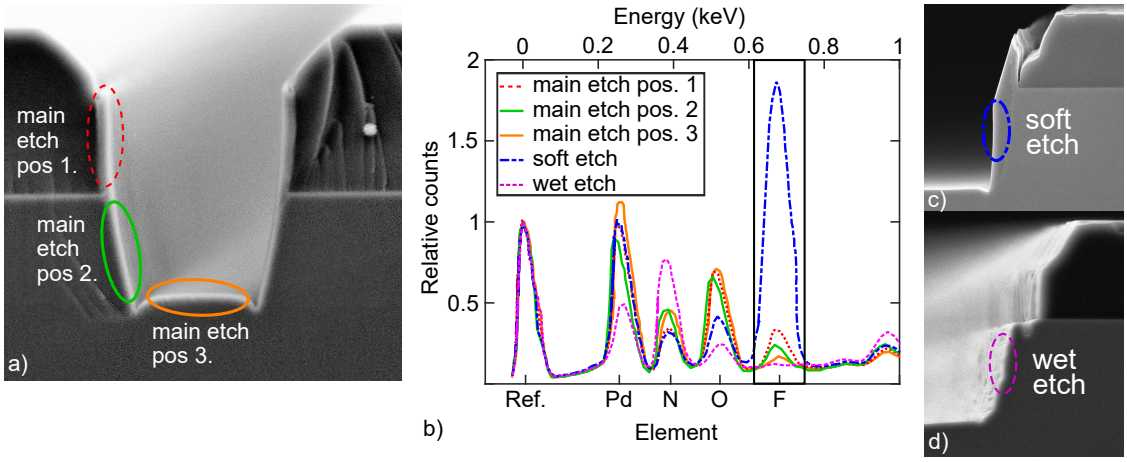

Figure 3.16: EDX spectra taken from different positions of a trench after dry and wet etching process steps. a) SEM image of a trench in GaN after the main dry etching procedure stated in table 3.1. Positions one to three indicate the EDX measurement sites at the SiO_2 mask flank, the trench sidewall and the trench bottom, respectively. b) Plot of the EDX spectra with counts normalized to one at the reference peak. c) and d) EDX measurement sites at the trench sidewall after soft etching according to table 3.1 and after 10 min in 25 % TMAH at 60 °C, respectively. Reproduced from [114], with the permission of the American Vacuum Society.

Increasing of sidewall steepness: The ability of KOH and TMAH to etch GaN in an anisotropic manner, and thus to create vertical sidewalls, was already demonstrated earlier in this section. Results for actual trenches, that were fabricated with 2 µm lithography and the combination of main and soft etching as stated in table 3.1, are shown in figure 3.17. The wet etching was performed in 33 % KOH for 30 min at 80 °C. For the image in figure 3.17 a), trench sidewall is oriented along the m-plane in b) along the a-plane. Both trenches show a perfectly vertical sidewall. However, a comparison of the two cross sections, as illustrated in figure 3.17 c), shows a difference in trench width. This becomes more clear by comparing the upper trench corners and their relation to the flank of the SiO_2 mask, indicated by the magenta circles in figure 3.17 a) and b). The higher etch rate along the a-direction, i.e. $[1\bar{2}10]$, widens the trench and reduces the distance between trench and mask corner. This clearly shows that the difference in trench width is not due to inhomogeneities during the lithography or dry etching procedures. If that were the case, the distance between the mask corners would be different as well. However, this distance is practically the same and the only explanation is a difference

in etch rate along the a- and m-direction, as was already found from the square etching experiment described in section 3.2.1.

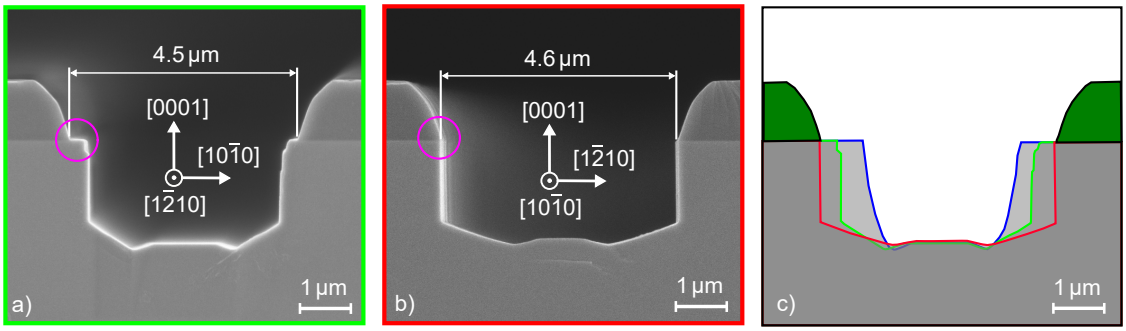

Figure 3.17: SEM cross section of trenches after wet etch treatment in 33 % KOH for 30 min at 80 °C. The trench in a) is aligned along the m-plane, the trench in b) along the a-plane. The schematic in c) is a superposition of the trench contours. After dry etching in blue, and after wet etching in green and red for the m- and a-plane aligned trench, respectively. Reproduced from [114], with the permission of the American Vacuum Society.

Reduction of microtrenches: Compared to the significant amount of GaN that is etched in lateral direction during the wet etching procedure, the material removed from the trench bottom is almost negligible. The trench depth does not change during the wet etching. As can be seen in figure 3.17, the plateau at the trench bottom is unchanged during wet etching. However, the microtrenches do allow access to crystal planes other than the inert c^+-plane, which leads to etching and an inclined trench bottom. The angles of inclination in figure 3.17 a) and b) are $32° \pm 0.5°$ and $18° \pm 0.5°$, respectively. This is far less than any of the angles listed in table 2.2 and it is not clear whether it can be related to an actual crystal plane. Although the trench bottom is not truly concave and still features corners, regarding the expected electric field distribution, the geometry is significantly improved compared to that before the wet etching. Further improvement will be discussed in section 3.3 together with other adjustments that were made to the trench fabrication process.

Removal of GaN from the sidewalls: Apart from removing the GaF_3, further removal of GaN from the sidewalls is desirable to avoid plasma caused crystal damage at the MOS interface. The schematic in figure 3.17 c) clearly shows that a significant amount of GaN is removed during the wet etching process both for m- and a-plane aligned trenches.

3.3 Trench size reduction and geometry improvement

By using the two step dry etching procedure in combination with wet etching post treatment, the obtained trench geometry fulfills most of the geometrical requirements stated in section 3.1.1. However, the trench width is over 4 µm and thus relatively large.

Depending on the channel resistance of a MOSFET, the pitch size, and thus the trench width can have a relevant impact on the on-resistance. Although such optimizations are not critical for a research device as presented here, a large trench width is still problematic since it does not allow the fabrication of a recessed gate as described in section 4.2.1. The most effective way to reduce the trench width is by reducing the lithography mask size. The lithography tool that was used has a resolution limit of $\approx 1\,\mu m$. Structures below this size cannot be fabricated reliably. Another limitation is the etching process of mask and trench itself. The high ion energy during the GaN etching and the inadequate thermal connection between wafer and chuck during the mask etching steps facilitate mask erosion and cause lateral etching. The effect is more drastic for smaller structures so that lithography below 1 µm probably would not further decrease the final trench size. However, by moving from a 2 to a 1 µm lithography mask, the achieved trench widths became sufficient for the recess process (cf. fig. 3.18). Further reduction would be possible with stepper lithography and a chlorine based etching process. The latter would allow a simpler and thinner mask system which is advantageous for smaller structures.

Apart from the size reduction of the lithography mask, the following measures were undertaken to reduce the trench width:

- Omitting the strike phase and reducing chamber pressure during the main dry etching step.
- Omitting the soft etching step.
- Focusing on TMAH for wet etching with elevated temperature of 90 °C for 40-45 min

Although the strike phase is useful for the plasma ignition, the higher chamber pressure has a negative impact on the etching procedure itself. Reduced ion energy and increased GaF_3 redeposition at the very beginning of a comparable short etching procedure hamper the trench formation. It was found that the process is stable enough to be conducted without a strike phase, which helped to reduce mask deterioration and increased the etch rate during the process from 1100 to 1350 nm/min.

Furthermore, the promising results of the wet etching treatment allowed to omit the soft etching step. Note that the remaining SiO_2 mask in figure 3.18 for the optimized procedure is thicker than in figure 3.17 for the unoptimized one. By omitting the soft etching step, the TMAH post treatment could be started with a trench structure with steeper, more defined sidewalls and far less GaF_3 deposits. This facilitated a more homogeneous etching as all features are accessible at the same time compared to before, where parts of the sidewall were covered by a thick layer of GaF_3 during the initial state of the wet etching procedure. Lastly, it was decided to step away from KOH and to perform wet etching only in TMAH, since no differences were observed in any of the previous experiments if process conditions, i.e. time and temperature, were the same. The reason for switching to TMAH is that the potassium in KOH is a potential contaminant, which should be avoided especially during the early stage of device fabrication and for MOS

interface related processes in particular. Figure 3.18 shows trenches that were fabricated with the improved process after plasma etching in a) and after wet etching in b)-d). Due to the generally smaller trench width, the microtrenches that are generated during the dry etching move towards each other and become practically irrelevant (fig. 3.18 a)). After 45 min in 90 °C TMAH, the a-plane oriented trench in b), features perfectly vertical sidewalls and a concave trench bottom. However, a sharp corner occurs at the bottom of the sidewall. The slower etch rate of m-plane oriented trenches, depicted in c), results in unfinished features and a still inclined sidewall. Step like features can be seen and the transition to the trench bottom is much smoother. To achieve a vertical sidewall, the etching must be prolonged to 130 min. The result is presented in d). Although vertical, crystal plane oriented sidewalls appear, the long etching time causes a retraction of the upper trench corner underneath the SiO_2 mask, which results in a larger, yet still acceptable trench width. As was already apparent from the trenches in figure 3.17, the trench bottom behaves differently during the wet etching procedure, with a pointier appearance of the m-plane oriented trench compared to the a-plane oriented one.

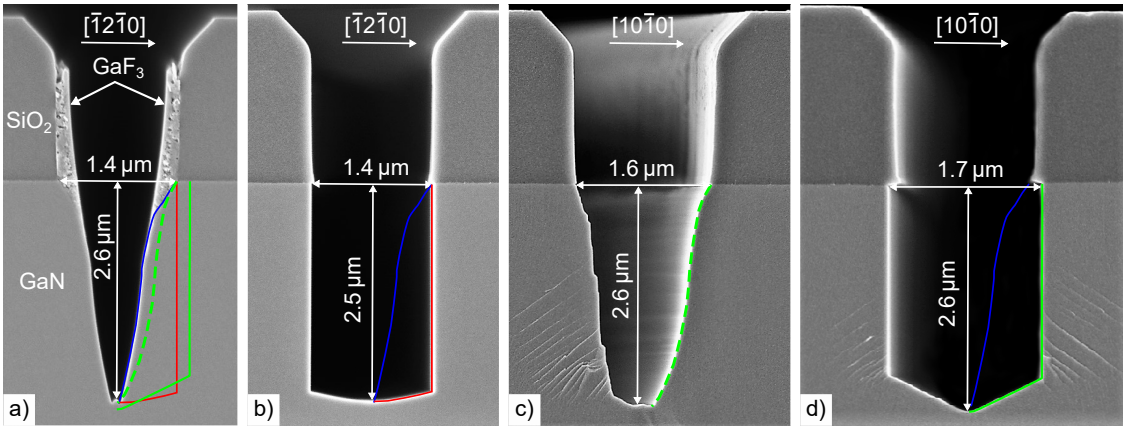

Figure 3.18: Trenches fabricated with the improved procedure and by using a 1 µm lithography mask. a) Trench after the main dry etching step without striking phase and with reduced chamber pressure of 5 mTorr. b) and c) trench from a) after subsequent wet etching in 25 % TMAH at 90 °C for 45 min, oriented along the a- and m-plane, respectively. Image d) displays the m-plane oriented trench after 130 min TMAH wet etching. Blue, red and green lines indicate the contour of the trenches in a), b), c) and d), respectively. Note that these trenches were fabricate during process engineering and are deeper than would be required for a typical trench MOSFET. Reproduced from [119], with the permission of the American Vacuum Society.

4 Planar and trench MIS capacitors

The second process block after trench fabrication and post treatment is the manufacturing of the actual gate structure. This comprises the deposition of gate dielectric, post deposition treatments and the manufacturing of the gate electrode. The chapter includes the published results from [120]. It treats the fabrication of planar and trench metal insulator semiconductor (MIS) capacitors that act as test modules for the actual MOSFETs discussed in chapter 5. Electrical characterizations concerning the following aspects were conducted:

- Leakage current flow between gate electrode and semiconductor
- Breakdown field strength of the dielectric layer
- Interface defects and hysteresis
- Temperature dependence of leakage current and breakdown field strength

4.1 Planar metal insulator semiconductor capacitors as test modules for the transistor gate structure

As discussed in section 2.6.5, the planar MIS capacitor represents a device, which is relatively simple to fabricate and yet allows the extraction of crucial information that is required during the optimization process.

Commonly used dielectrics in GaN MOSFETs are SiO_2 [25, 52] and Al_2O_3 [42, 46, 48, 27], with atomic layer deposition (ALD) and MOCVD being the preferred deposition methods. As described in section 1.1, this work focuses on a poly Si based metal-free gate structure with a LPCVD gate dielectric. For comparison, Al_2O_3 in combination with an aluminum gate will be evaluated as well. Options for LPCVD dielectrics are SiO_2 and silicon nitride (SiN), which will both be evaluated. Note that the stoichiometry of the silicon nitride can slightly deviate from the perfect ratio of Si_3N_4 and the material will therefore be termed SiN. The band offsets for the mentioned materials along with dielectric constant and breakdown field strength are displayed in figure 4.1 a). The fabrication and examination of the MOS capacitors pursues two objectives. The first is to determine the performance of various dielectrics and the effect of post deposition annealing procedures regarding dielectric breakdown and leakage current. The second objective concerns the evaluation of the gate electrode material and the advantage of a gate-first process compared to a gate-last process. Exemplary device configurations for

both process types are depicted in figure 4.1 b). The gate-last type is defined by the fact that the gate structure is fabricated after the formation of the other metal contacts. This limits the choice of gate electrode materials to a metal since metal-free process environments are no longer accessible. Therefore, the gate-last structure in figure 4.1 (top) employs an aluminum gate electrode directly on top of the dielectric. A light version of the gate-last process can be implemented by fabricating the gate dielectric before and the gate electrode after the formation of the other metal contacts. This allows the deposition of the dielectric in a metal-free environment but requires a metal containing gate electrode. The gate-first process stands out by the fact that gate dielectric and contact both are fabricated in a metal-free process and are passivated prior to any metal containing fabrication step. The sample configuration for this experiment is listed in table 4.1. Note that the samples are categorized between gate-first and last process.

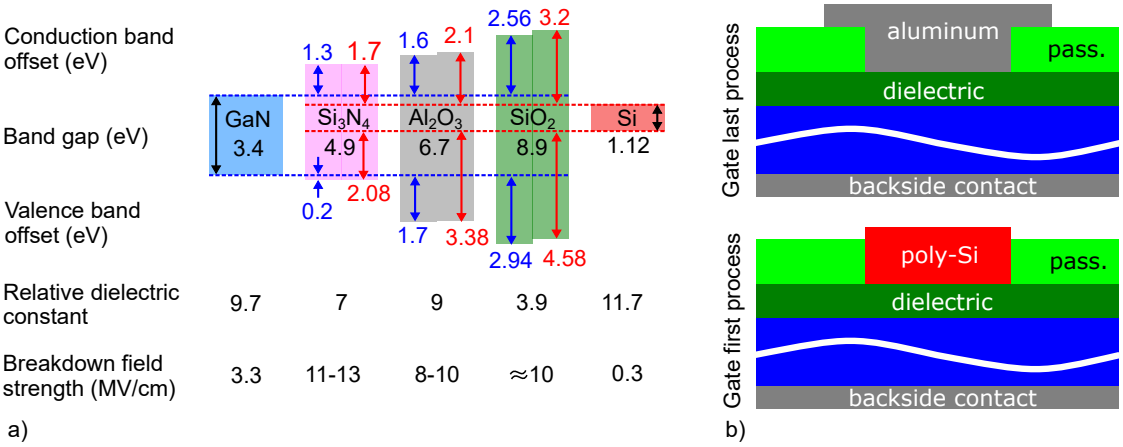

Figure 4.1: a) Conduction and valence band offsets for various dielectric materials to GaN (blue arrows and numbering) and silicon (red arrows and numbering). b) Schematic depiction of a simple planar MOS capacitor with aluminum gate (top) and poly Si gate (bottom). Data from [121, 122, 106, 123–127]. Reproduced from [120], with the permission of the American Vacuum Society.

Following a description of the process flow and fabrication procedure, the rest of this chapter treats the electrical characterization of these samples regarding leakage current density, breakdown field strength and hysteresis. Based on the outcome at different temperatures, a conclusion regarding thermal stability and robustness is drawn.

4.1.1 Process flow of planar MIS capacitors

All samples were fabricated on highly n-doped, free standing 50 mm Ga-face GaN substrates. This ensures a negligible voltage drop across the semiconductor and allows a reasonable accurate calculation of the field strength in the dielectric layer. A detailed calculation of this field strength is given in section 4.1.2. To achieve a reproducible and clean surface, a 10 min wet etching step in 37 % hydrochloric acid (HCl) at 60 °C is performed, followed by 10 min in 25 % TMAH at the same temperature. This procedure

ensures that the surface is free of any oxide. The samples are then rinsed with deionized water and dried with nitrogen. The dielectric layers were fabricated via LPCVD in the case of SiO_2 and SiN and via ALD for Al_2O_3. Thermal annealing in nitrogen ambient at 800 °C was applied for some of the samples at either 20 mTorr or atmospheric pressure to examine a potential repairing effect concerning the GaN to dielectric interface. The configurations for all examined samples are listed in table 4.1. The gate electrode was then fabricated by depositing either phosphor doped LPCVD poly Si at 580 °C with subsequent activation at 900 °C or, in the case of an aluminum contact, by sputtering on the gate dielectric. For the aluminum gated samples, the gate electrode was fabricated after the formation of the aluminum backside contact to avoid any reactions at the Al-SiO_2 interface at high temperature. This procedure can be regarded as an intermediate between gate-first and last process. The dielectric is deposited prior to any metal related fabrication steps, while the gate electrode is fabricated afterwards. The dielectric layer thickness was chosen in the rage of 40 to 60 nm to mimic the conditions in the actual MOSFET and determined via spectral ellipsometry. A gate-last process, in the precise sense, was required for the Al_2O_3 sample. As shown by Hori et al. [128], issues such as the formation of microcrystallization regions and increased leakage current can occur in ALD Al_2O_3 if the material is annealed at high temperatures as is required for the formation of the backside contact. Therefore, a special routine was used for this sample. The GaN surface was capped by LPCVD SiO_2 during backside contact formation to prevent surface contamination. After the contact annealing, the SiO_2 protection cap was removed in hydrofluoric acid and only then, after an additional 10 s TMAH dip, the ALD Al_2O_3 was deposited and the aluminum gate electrode added. This procedure ensured that neither the Al_2O_3 layer nor the uncovered GaN surface were exposed to the high temperature during backside contact formation.

The backside contact consisted of 20 nm titanium with 100 nm aluminum on top, both deposited via sputtering. To achieve an ohmic contact with the semiconductor, thermal annealing at 900 °C for 3 min was applied. Finally, a 500 nm thick aluminum layer was deposited on front- and backside to improve the contact to chuck and needles of the prober. To minimize leakage current between the different structures, a 750 nm thick passivation layer of SiO_2 was deposited. The result were square shaped capacitors with areas ranging from $5 \cdot 10^{-4}$ to $1.5 \cdot 10^{-3}\,cm^2$.

4.1.2 Electrical characterization of planar MIS capacitors

To examine and assess the various device configurations, the measurement methods described in section 2.6.5 were applied. To ensure high resolution and a low noise level of $\approx 1\,pA$, triaxial cables were used in combination with a Keithley K2636 source meter. If not specified otherwise, the sweep rate was 0.2 V/s. A K6517 electrometer was utilized for QSCV-measurements.

Table 4.1: Configuration and process parameters for different samples. If a sample was annealed, the conditions were 1 h at 800 °C in nitrogen ambient under the specified pressure.

Semi-conductor	Dielectric and thickness	Annealing pressure	Gate metal, gate-first/last
n-substrate	64 nm LPCVD SiO_2	no annealing	Al, first
n-substrate	64 nm LPCVD SiO_2	no annealing	poly Si, last
n-substrate	50 nm LPCVD SiO_2	2.67 Pa	poly Si, last
n-substrate	50 nm LPCVD SiO_2	101 kPa	poly Si, last
n-epitaxy	50 nm LPCVD SiO_2	101 kPa	poly Si, last
p-epitaxy	50 nm LPCVD SiO_2	101 kPa	poly Si, last
n-substrate	50 nm LPCVD SiN	2.67 kPa	poly Si, last
n-substrate	50 nm LPCVD SiN	101 kPa	poly Si, last
n-substrate	50 nm PECVD SiO_2	2.67 Pa	poly Si, last
n-substrate	50 nm PECVD SiO_2	101 kPa	poly Si, last
n-substrate	38 nm ALD Al_2O_3	no annealing	Al, first

CV-measurements to extract dielectric constants and flat band voltage: The results of the CV-measurement are displayed in figure 4.2 for n-type in a) and p-type in b), normalized to the dielectric capacitance C_{diel}. One outcome of this measurement is the flat band voltage V_{FB}. This measure is important to convert the capacitor voltage into the dielectric field strength as is described in the next paragraph. The flat band voltage is determined at $C/C_{\mathrm{diel}} = 0.8$ and was (-3.2 ± 0.2) V for SiO_2, (1.0 ± 0.1) V for Si_3N_4 and (2.1 ± 0.1) V for Al_2O_3. The measurement results also reveal to what extend depletion occurs. Although the measurement was only possible for voltages above -25 V (below +25 V for p-type) due to the rise in leakage current, it shows a clear distinction for the different samples. The larger thickness of the SiO_2 and Si_3N_4 layers impedes depletion. Especially for the SiO_2 sample, most of the voltage drops across the dielectric, which is plausible considering its much lower dielectric constant compared to GaN. The Al_2O_3 sample on the other hand, is pushed much further into depletion, due to a higher dielectric constant and a thinner dielectric layer. As can be seen in figure 4.2 b), depletion for the p-type sample is only marginal. IV-measurements in forward direction should hence be possible on this sample since voltage drop across the semiconductor is negligible due to insufficient depletion. The right side of the CV-plot in figure 4.2 a) shows electron accumulation and can be used to determine the relative dielectric constant ε_{r} of the insulator by using equation (2.34) since in this regime $C = C_{\mathrm{ox}}$. The calculation yielded $\varepsilon_{\mathrm{r}}(SiO_2) = 4.10 \pm 0.13$, $\varepsilon_{\mathrm{r}}(Si_3N_4) = 7.10 \pm 0.20$ and $\varepsilon_{\mathrm{r}}(Al_2O_3) = 8.6 \pm 0.4$, which is in agreement with the literature values stated in figure 4.1 and a good validation for the CV-measurement.

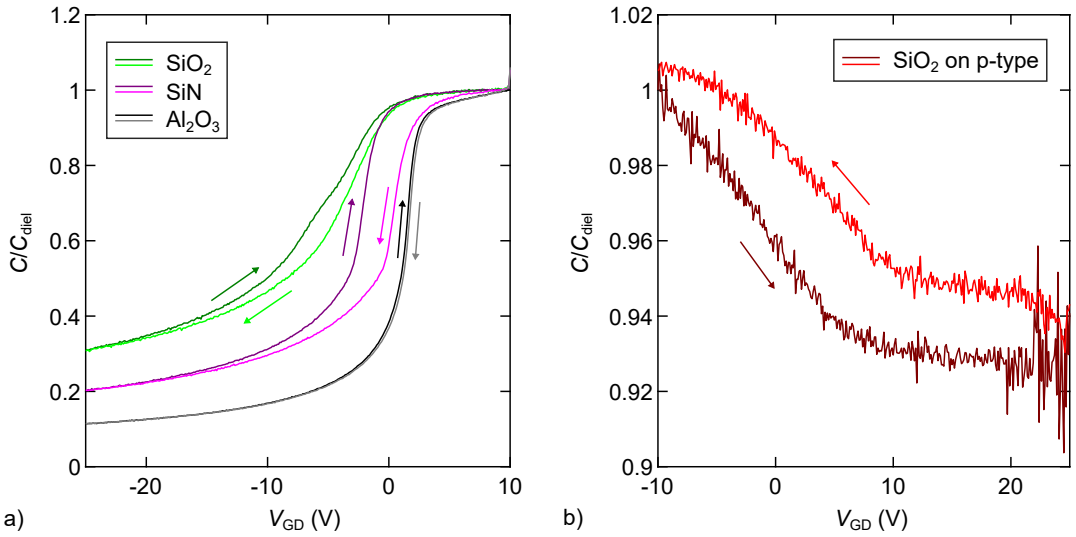

Figure 4.2: Quasi static CV-curves normalized to the capacitance of the dielectric layer for samples on an n-type GaN substrate a) and a p-type epitaxial layer b). Reproduced from [120], with the permission of the American Vacuum Society.

Measurement of dielectric leakage current density and electric breakdown: The voltage V_{GD}, applied between the front and backside contact of the MOS capacitor, was converted into the dielectric field strength via

$$E_{\mathrm{diel}} = \frac{V_{\mathrm{GD}} - V_{\mathrm{FB}}}{t_{\mathrm{diel}}}. \tag{4.1}$$

The absolute value of the measured gate leakage current in forward and reverse direction is plotted in figure 4.3 for gate-first samples with poly Si gate and SiO_2 or SiN as dielectric and a gate-last sample with aluminum gate and Al_2O_3. Focusing on the forward direction, i.e. positive bias at the gate electrode, one finds an early increase in leakage current for the SiN and Al_2O_3 samples compared to the sample with SiO_2. This can be explained by the smaller conduction band offset between GaN and these materials (cf. fig. 4.1). The relevant barrier is illustrated in the insets in figure 4.3. Note that the effect of an early increase in leakage current for the SiN and Al_2O_3 samples is smaller, if the MOS capacitor is reverse biased. As illustrated by the inset on the left side, the relevant barrier in this case is the one between silicon and dielectric, which is higher for all materials, resulting in a generally later increase in leakage current compared to forward biasing. Note that there is an increased uncertainty for the data measured under reverse bias. As demonstrated by the CV-results in figure 4.2 a), partial depletion occurs. This results in an increased voltage drop across the semiconductor, which in turn leads to an overestimation of the calculated dielectric field strength in the reverse bias section of the graph in figure 4.3. In forward direction, the calculation is reasonably accurate and the advantage of the wider band gap of SiO_2 becomes apparent. Compared to Al_2O_3 and SiN, the larger band offset of SiO_2 ensures low leakage current density up to an electric field strength of 4-5 MV/cm. In agreement with the literature values stated in figure 4.1 a), the SiN

samples show high breakdown field strength. However, high leakage current in the low field regime makes the material a poor choice. The latter is also true for the Al_2O_3. The premature breakdown of this sample can probably be attributed to the aluminum gate electrode. An in-depth discussion of its adverse effect will be given below.

The conclusion from the measurement is that SiO_2 represents the best choice regarding leakage current and offers a reasonably high breakdown field strength. The three regime model introduced in section 2.6.5 can be applied to the SiO_2 curves and one finds a field strength of 3-4 MV/cm as limit for reliable operation. This corresponds to 15-20 V maximum gate bias for a MOSFET with a 50 nm thick gate dielectric. The validity of the said limit will be supported and discussed in more detail during the course of this section. An effect of thermal annealing is not apparent from this measurement but will be discussed in more detail next.

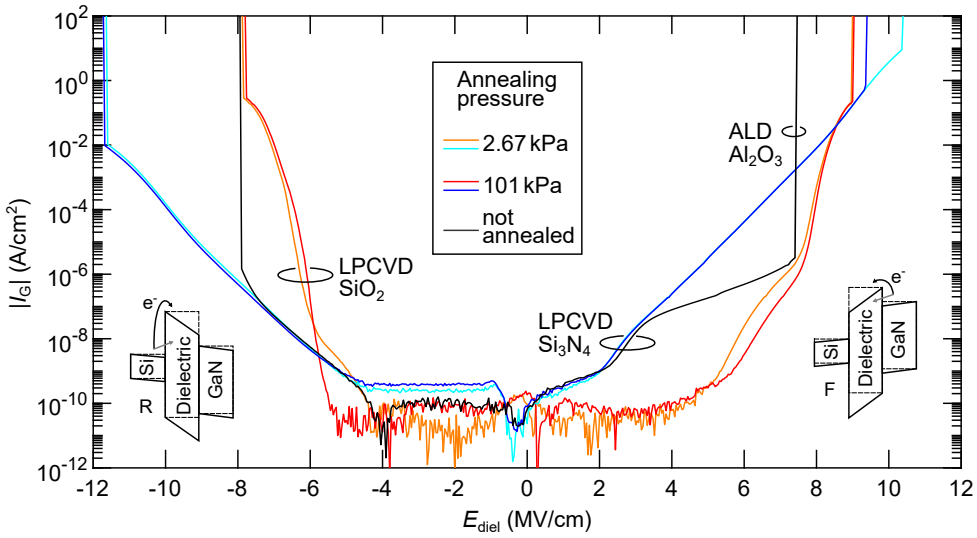

Figure 4.3: Absolute value of the gate leakage current for $5 \cdot 10^{-4}\,\mathrm{cm}^2$ sized MOS capacitors measured at 300 K. Gate-first process with poly Si gate for the SiO_2 and SiN samples and gate-last process with aluminum gate for the Al_2O_3 sample. Reproduced from [120], with the permission of the American Vacuum Society.

Apart from a well-founded decision regarding the dielectric material for later use in MOSFETs, the aim of this section is also to assess the benefit of a poly Si gate compared to the conventional metal alternative. The plot in figure 4.4 a) shows the gate leakage current for MOS capacitors with aluminum and poly Si gate in comparison and for different temperatures. The plot in b) illustrates the temperature dependence of the breakdown field strength for different samples. The results focus on the more relevant and more viable case of forward biasing and reveal clearly the advantage of a poly Si gate. The dielectric layers of both samples, presented in a), consist of SiO_2 and were deposited in the same run. They can thus be regarded as nominally identical. Any difference in the measurement outcome is due to post deposition annealing and the subsequently deposited gate electrode. In the low voltage regime, that is below ≈ 3 MV/cm, the leakage current density is comparable for all temperatures and for both gate types.

However, a slight trend towards higher current for elevated temperature can be observed. The breakdown voltage however, is generally lower for the aluminum gated device with a strong inclination to premature failure at temperatures above 400 K. The breakdown robustness of the poly Si gated device on the other hand, is practically not affected by temperature and breakdown occurs generally later. As demonstrated by a statistical evaluation, plotted in figure 4.4 b), two factors are relevant for the improved breakdown field strength, namely the poly Si gate electrode and the post deposition annealing in nitrogen ambient. The aluminum based gate-last process leaves the gate dielectric uncovered during several process steps, including the 900 °C contact formation procedure in a metal containing environment. This leads most likely to the incorporation of metal ions and other impurities, which inevitably compromise breakdown robustness. Another potentially adverse factor is the sputter deposition of the aluminum gate, which might degrade the Al-SiO_2 interface. The SiO_2-GaN interface is only marginally affected, which explains the comparable low leakage current for both choices of gate material. Concerning HEMT applications, Jauss et al. [129] found better reliability regarding temperature and longer lifetime for poly Si gates compared to their metal based counterparts. This is in agreement with the outcome of the experiment presented here.

A possible explanation for the higher breakdown field strength of the sample with post deposition annealing is a reduced amount of hydrogen in the dielectric layer. The LPCVD SiO_2 process is based on a gas mixture of nitrous oxide (N_2O) and dichlorosilane (H_2SiCl_2). The latter causes a hydrogenous process ambient, which inevitably leads to the incorporation of a certain amount of hydrogen in the deposited layer. If this layer is instantly capped by a relatively thick poly Si layer that also contains hydrogen, the hydrogen incorporated in the SiO_2 layer is mostly confined. The incorporated hydrogen generates traps and weakens the dielectric, leading to the observed reduction in breakdown robustness. If on the other hand, the SiO_2 is thermally annealed in nitrogen, prior to the deposition of the gate electrode, hydrogen can diffuse out of the SiO_2 and the electrical stability of the SiO_2 layer is improved.

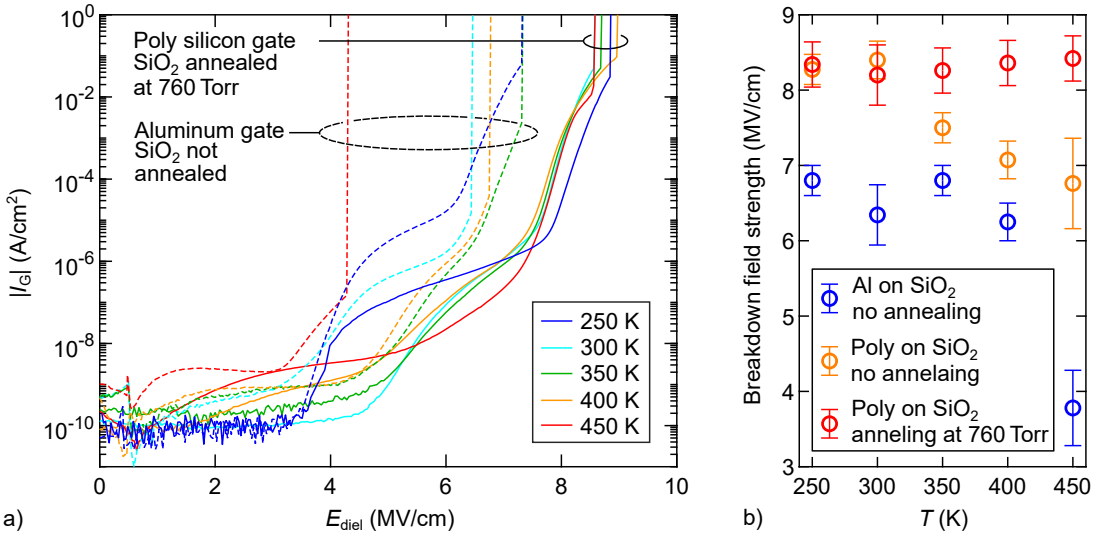

Figure 4.4: a) Absolute value of the gate leakage current for $5 \cdot 10^{-4}\,\mathrm{cm}^2$ sized MOS capacitors with aluminum and poly Si gate measured at different temperatures. b) Statistical evaluation of the temperature dependence of the breakdown field strength based on 8-16 samples. The annealing was performed for 1 h at 800 °C in N_2. Reproduced from [120], with the permission of the American Vacuum Society.

Evaluation of hysteresis determined from looped IV-curves: Apart from leakage current and breakdown voltage, hysteresis of the IV-curve is a relevant criterion in the optimization process of the gate structure. All curves in figures 4.3 and 4.4 show a more or less distinct point, at which the leakage current density increases strongly. This is in accordance with Bisi et al. [123] who identified two different regions: high field and low field. These regions coincide with the regions defined in section 2.6.5 where the high field region was separated into two different regimes. Focusing on low and moderate field strength, the point at which the gate current rises is clearly visible in the plots in figure 4.5 where the IV-hysteresis was examined by ramping the gate voltage, depending on the thickness of the dielectric layer, up to $\approx 80\,\%$ of the breakdown voltage and then back to zero. This was done four times consecutively. For the sake of clarity and since loop 2, 3 and 4 differ only marginally for all samples, only loops 1 and 2 are shown in figure 4.5. The measurement was performed from 0 to 35 V. Note that due to differences in layer thickness and flat band voltage, values on the field strength axis vary.

Two types of hysteresis were identified from this measurement. The first one is the difference between up and down sweep if the initial sweep is excluded. This difference is most pronounced in the transition area between low and high field regime at the point where the return sweep current has its zero crossing. The effect is relatively small and no significant distinction was found between the various dielectrics. The second hysteresis type that was identified, is a difference between the up curves of loop 1 and loop 2. This effect is larger and different for the various dielectrics. The smallest hysteresis of this type was found for the annealed SiO_2 samples with poly Si gate. A direct comparison of the results (fig. 4.5 b) and c)) shows that the effect was further reduced if the post

deposition annealing was performed at a higher ambient pressure. Since there is no indication that nitrogen interacts with SiO_2, a likely explanation is a repairing effect of the GaN surface by nitrogen incorporation [56]. This effect is apparently more pronounced if the ambient nitrogen pressure is higher, which increases diffusivity through the dielectric layer. The repairing of the interface is likely to diminish the amount of interface states, which in turn reduces charging effects and also the observed hysteresis phenomenon. A similar procedure is successfully employed for SiC devices [130–132]. The fact that the non-annealed sample with the same, although slightly thicker dielectric layer (fig. 4.5 a)), features a more prominent hysteresis, supports the assumption that the hysteresis originates not from the gate electrode, but the dielectric layer or more precisely the SiO_2-GaN interface.

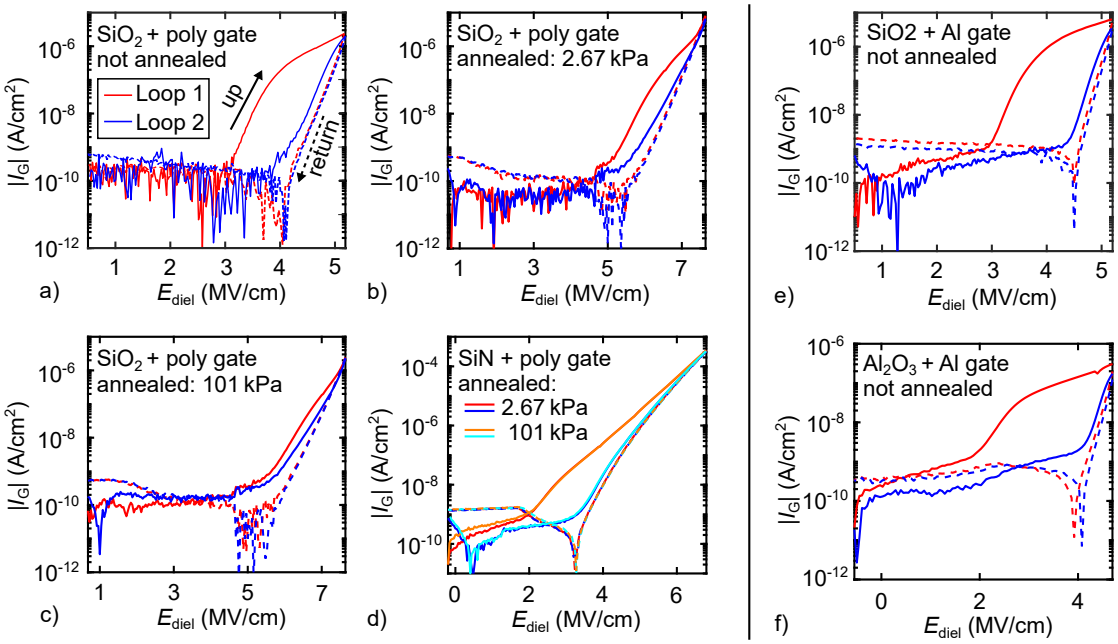

Figure 4.5: Absolute value of the gate leakage current density plotted against the dielectric field strength for two consecutive loops consisting of an up (solid line) and down sweep (dashed line). Plots a), b) and c) show data for SiO_2 samples with different post deposition annealing procedures. Plot d) combines the nearly identical results of the two differently annealed SiN samples. Separated to the right in e) and f) are the results for samples with aluminum gate. Reproduced from [120], with the permission of the American Vacuum Society.

A larger hysteresis, compared to annealed SiO_2 samples, is observed for the SiN samples presented in plot d) and no difference was found if the annealing pressure was changed. Note that both SiN samples are plotted in the same graph, which emphasizes the small difference between them. Since there was no effect observed for different annealing pressures on a wider range in figure 4.3, no effect was to be expected from the hysteresis measurements. The ineffectiveness of the nitrogen treatment for SiN samples can be explained by the low diffusion coefficient of nitrogen in SiN. Schmidt et al. [133] reported a diffusivity of $D = 6 \cdot 10^{-20} - 2 \cdot 10^{-22}\,\mathrm{cm^2/s}$ for a temperature of 800 °C, which is

several orders of magnitude lower than the value for nitrogen diffusion in SiO_2, reported by Kajihara et al. [134] as $D = 1.4 \cdot 10^{-11}$ to $1.2 \cdot 10^{-9}\,cm^2/s$. The lower hysteresis for the SiN samples compared to the not annealed SiO_2 sample is probably due to the greater abundance of nitrogen during the deposition and it might be possible that, close to the interface and to a certain degree, nitrogen atoms are exchanged between GaN and SiN. Furthermore, the SiN deposition temperature is only 775 °C compared to 880 °C for the SiO_2 deposition and thus degradation of the GaN surface is likely to be less severe.

The strongest hysteresis was found for the aluminum gated samples (fig. 4.5 e) and f)). However, the difference between the plots in figure 4.5 a) and e) is relatively small and the gradually reduction of the hysteresis from a) over b) to c) indicates that the annealing, and thus the SiO_2-GaN interface, is the relevant factor and that the impact of the aluminum gate is not significant. The even stronger hysteresis in the case of the Al_2O_3 sample in plot f) can, apart from material related effects, probably be attributed to a generally poorer interface quality. As described in section 4.1.1, the fabrication process required the deposition and removal of a sacrificial protection layer. These additional steps could be at least one reason for the strong hysteresis in this case.

The mentioned hysteresis is attributed to charging of interface and near surface states. However, the nature of these states is different for the two types of hysteresis. The current difference between up and down sweep is rather small but occurs each loop. This suggests that the responsible states are charged during the up sweep and discharged during the down sweep with a response time faster than the sweep rate, the latter being in the order of seconds. The second hysteresis type, responsible for the difference between the initial up sweep curve and any subsequent up sweep, originates from states and traps that are not reset if the gate bias returns to zero. Even a rest phase with $V_{GD} = 0\,V$ for several days did not result in a complete reset. To further examine the nature of these traps, a cyclic measurement procedure was conducted on the poly Si gated sample with 64 nm LPCVD SiO_2 without annealing step because its hysteresis is more pronounced than for annealed samples, making any changes better observable. The measurement cycle consisted of the following procedure, which was repeated for two loops and is schematically depicted in figure 4.6 a). The plots in b) and c) present the corresponding IV-curves. In a first ramp up from zero to 30 V, the initial up curve was measured with a subsequent return to zero volt. Following that, the bias was reversed and a down curve to -30 V was measured (not shown in the graph). At this point, charges incorporated or states filled during the up sweep, are removed or depopulated by holding this state for 1000 s. After returning back to zero volt, a second up curve is measured after which the bias is swept back to zero. This concludes loop A, which is directly succeeded by loop B consisting of the same procedure. Note that unlike in figure 4.5 a), where no reset procedure was applied, the initial and second up curves of loop A in figure 4.6 b) (solid red and orange) are practically identical in the high field region, which suggests that the initial interface condition was mostly restored by the 1000 s hold at -30 V. Since loop A ends at zero volt, the initial up curve of loop B shows the expected right shift as

no reset was performed. As loop B proceeds, bias is swept to -30 V and again held for 1000 s. This restores the interface condition and causes a shift back to the left for the second up curve in loop B, indicated by the magenta arrow in figure 4.6 b). The curve is only slightly below those of loop A, suggesting again an almost complete reset of the interface condition. The same procedure was also carried out without a hold phase at -30 V with the measurement results displayed in figure 4.6 c). The curves show that a procedure that lacks the hold period fails to reset the interface condition. The second up curve of loop A differs clearly from the first curve. However, it is above the initial up curve of loop B, which suggests that at least a partial reset did occur. This is supported by the fact that the second up curve of loop B also lies above the initial up curve of loop B and close to the second up curve of loop A (magenta arrow in fig. 4.6 c)). In essence, the left shift of the second up curve of loop B (magenta arrow) is more pronounced in b) than in c), which indicates a more complete interface reset for the procedure with hold phase compared to a procedure without hold phase. The results clearly indicate a time dependent depopulating and reloading effect that takes place at negative bias.

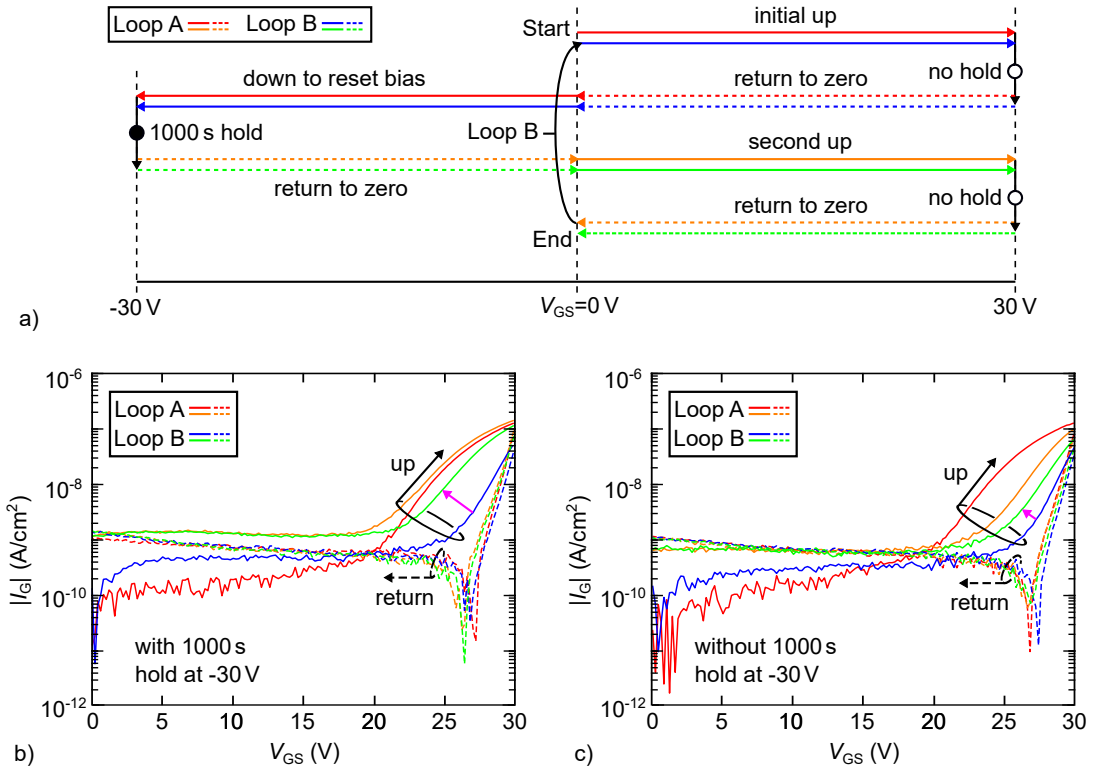

Figure 4.6: Interface reset procedure for a non-annealed sample with SiO_2 dielectric and poly Si gate-last process. a) Schematic of the sweeping procedure for interface reset. Each loop consists of two sections, initial and second, indicated in red and orange for loop A, and dark and light blue for loop B. b) And c) hysteresis measurement for the reset sweeping procedure. For the sake of clarity, only the positive side of the sweeps is depicted. Solid lines mark up sweeps and dashed lines represent return sweeps to zero volt. The magenta arrows in b) and c) indicate the left shift of the second up curve in loop B that occurred due to the reset procedure. Reproduced from [120], with the permission of the American Vacuum Society.

While this cyclic procedure offers an explanation for the difference between initial and subsequent up sweeps, one feature, common to all measurements with up and down sweep, needs yet to be addressed. This is the distinct spike during the reverse sweep, which represents a zero crossing of the gate current (cf. fig. 4.5). This zero crossing occurs at a bias far above the flat band voltage. In an ideal system, the current reversal point would coincide with the flat band voltage. Such behavior was also found by Bisi et al. [123] and indicates the introduction of charge into interface or near interface states. These states, some of them most likely also responsible for the hysteresis discussed above, are charged during the up sweep and start to discharge if the gate bias drops below a certain level. This supplies the observed negative gate current. Note that the current reversal point coincides closely with the onset of leakage current during the loop B. During loop A, states with long lifetime get saturated and thus are no longer relevant during subsequent loops. These states were identified as relatively stable by the sweeping procedure depicted in figure 4.6. States with short lifetime, however, seem to be filled and emptied during each loop.

Fowler-Nordheim leakage current mechanism through the gate dielectric: A theory that models the charge population in the gate system is schematically illustrated by band diagrams in figure 4.7 a) and supported by a measurement curve plotted in b). As introduced in section 2.6.5, three regimes of different dielectric field strength are defined. Starting at zero volts and increasing gate bias, shallow traps at the GaN-SiO_2 interface are filled as illustrated in the schematic A in figure 4.7 a). The measured current curve is basically horizontal and represents a displacement current [123] with no actual leakage through the dielectric. Parasitics such as cables, chuck and prober needle must be considered as well. As soon as regime II is approached, current starts to rise. The shape and magnitude of the leakage current curve shows only a weak dependence on temperature, which rules out Pool-Frenkel Emission (eq. (2.30)) as plausible conduction mechanism through the dielectric. The commonly observed conduction mechanism for MOS capacitors is Fowler-Nordheim Tunneling (eq. (2.31)). The magenta line in figure 4.7 b) indicates the theoretical Fowler-Nordheim (FN)-current, assuming an electron mass of $0.3\,m_\mathrm{e}$ in the dielectric [135] and a barrier height between GaN and SiO_2 of $\Phi_\mathrm{B} = 2.56\,\mathrm{eV}$ (fig. 4.1 a)). The theoretical curve fits the measurement only at the beginning and then starts to deviate. As shown in the schematic B in figure 4.7 a), electrons continue to fill shallow traps near the surface, but also start tunneling through the dielectric according to the FN-theory. A third path is the charging of deeper states located at the interface or in the bulk dielectric. The difference between measured and theoretical curve is explained by the inset in figure 4.7 b). Accumulated charge in interface and near surface states causes a compensating electric field E_comp, which reduces the effective field strength E_eff across the barrier and leads to a lower leakage current density than anticipated by the FN-theory. This charging effect can be avoided if the down sweep branch of the mea-

surement curve is used. Indicated by the dashed magenta line is the FN-theory curve, shifted to the right and calculated via

$$j_{\mathrm{FN_{shift}}} = \frac{q^2 E_{\mathrm{eff}}^2}{16\pi^2 \hbar \Phi_{\mathrm{B}}} \exp\left[\frac{-4\sqrt{2m^*_{\mathrm{diel}}}(q\Phi_{\mathrm{B}})^{3/2}}{3\hbar q E_{\mathrm{eff}}}\right] \tag{4.2}$$

where E_{eff} is modeled as

$$E_{\mathrm{eff}} = AE_{\mathrm{ext}} + B. \tag{4.3}$$

The factor $A < 1$ represents a bias dependent field reduction due to the charging of shallow traps, B denotes the overall offset due to fix charges incorporated into the dielectric. Fitting yielded reasonable values of $A = 0.9$ and $B = -0.38\,\mathrm{MV/cm}$ with the result being a good match across the complete regime II. To account for charging during the up sweep, an additional term needs to be added to equation (4.2).

$$j_{\mathrm{FN_{shift}}} = \frac{q^2 E_{\mathrm{eff}}^2}{16\pi^2 \hbar \Phi_{\mathrm{B}}} \exp\left[\frac{-4\sqrt{2m^*_{\mathrm{diel}}}(q\Phi_{\mathrm{B}})^{3/2}}{3\hbar q E_{\mathrm{eff}}}\right] + C_1 \exp\left[C_2 E_{\mathrm{eff}}\right]. \tag{4.4}$$

The added term represents an exponential trap distribution at the upper band edge (cf. sec. 2.6.3), which is charged during the up sweep. Using $C_1 = 8\text{e-}17\,\mathrm{A/cm^2}$ and $C_2 = 3.6\,\mathrm{cm/MV}$ the dotted green line in figure 4.7 b) is obtained, which fits the up sweep in regime II. the deviation in region I is due to the noise level. The last regime to be discussed is regime III. Note that none of the theories explains the sudden rise in current at the onset of regime III. This is due to additional current paths, generated as the dielectric is destroyed. This circumstance is indicated in the schematic D in figure 4.7 a). Such percolation paths and thermally induced damage eventually lead to fatal breakdown.

The conclusion from this analysis is that during operation field strength should not increase beyond regime I as this leads to a permanent change of the interface charge density and thus to a shift of parameters such as threshold voltage.

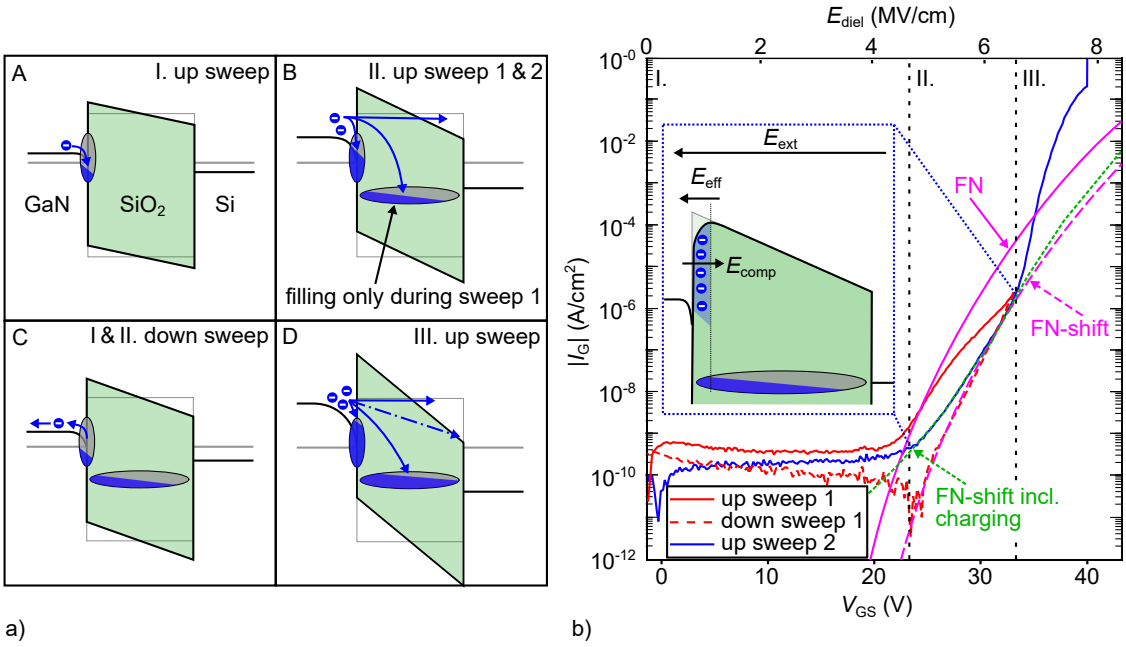

Figure 4.7: a) Band diagram of the gate structure under forward bias illustrating trap charging and current flow for various field strength. b) IV-curve a MOS capacitor corresponding to the sample presented in figure 4.5 b).

The effect of dielectric field strength lowering, due to interface charging, can also be seen from the plot in figure 4.8 a). Gate leakage current was measured for different sweep rates that were varied over five orders of magnitude and is plotted against the dielectric field strength. Note that the higher leakage current for fast sweep rates is due to a lower resolution for fast measurements. The breakdown field strength is practically not affected by the sweep rate but regime II leakage current is significantly higher for fast sweep rates with a gradual reduction if the sweep rate is reduced. This behavior strongly suggests that a certain time is needed to fill the deep oxide traps, which cause the above mentioned shift in the FN-current. In other words, the effective electric field in equation (4.4) is larger for faster sweep rates as the compensating charging of trap states cannot follow the increase in gate voltage. The opposite effect is observed for the SiN sample, where a slower sweep rate reduces breakdown field strength but has only a minor effect on regime II leakage current. The curves measured for the SiN sample are presented in figure 4.8 b) and indicate that, in agreement with the band parameters from fig. 4.1 a), charge incorporation at the GaN-SiN interface is more pronounced than it is the case for SiO_2. The lower band offset, i.e. the lower barrier, leads to higher leakage current in the low field regime. The current seems to flow through the dielectric and is likely to cause damage. According to figure 4.8 b), the damage is related to time, which is highly problematic for long time reliability. A later onset of gate leakage current and a breakdown voltage that is independent from the sweep rate are clear advantages of SiO_2 compared to SiN.

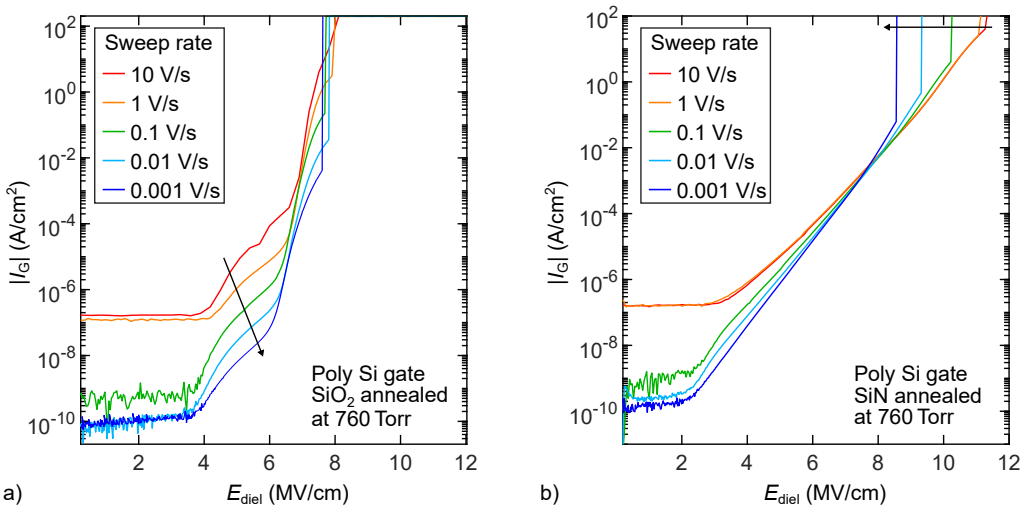

Figure 4.8: Absolute value of the gate leakage current density measured with different sweep rates for a structure with 50 nm SiO_2 in a) and 50 nm SiN in b). Note that the high leakage current density for fast sweep rates is due to a lower resolution of the measurement equipment in the fast sweeping configuration.

4.2 Trench MOS capacitors

Although the planar MOS capacitors, described in section 4.1, provide a relatively simple and useful way to examine the properties of gate dielectric and electrode, they are not accurate representatives of a trench gate structure. Therefore, trench MOS capacitors were fabricated and characterized in a similar manner as their planar counterparts. Silicon dioxide and poly silicon were used as dielectric and gate metal, respectively, and electrical characterization was focused on IV-breakdown curves. Although not implemented for the actual trench MOSFETs, a thick bottom oxide (TBOX) was added for one sample and its effect on the breakdown voltage was evaluated. Besides the fabrication process flow for trench MOS capacitors, section 4.2.1 provides a brief introduction to the TBOX concept and its fabrication procedure.

4.2.1 Description of the thick bottom oxide and the fabrication procedure of trench MOS capacitors

As described in section 4.1.2, the electric field strength limit of the gate dielectric must not be exceeded so that immediate or long term breakdown is avoided. A thicker dielectric can help to reduce field peaks, originating from corners and kinks in the gate geometry and reduces the field strength in general. This is especially useful for trench gate structures. The plot in figure 4.9 a) shows the simulated voltage drop across the gate dielectric, as well as the dielectric field strength, as function of the thickness of the said dielectric. The simulation is set up as illustrated in the schematic in figure 4.9 b) with a $10^{16}\,\mathrm{cm}^{-3}$ Si-doped drift layer of 15 µm thickness and a fixed gate to source voltage of -100 V while drain to source bias is 0 V. The dielectric field strength decreases faster than the voltage

drop across the dielectric layer increases. This means that, apart from mitigating field peaks in particular, a thicker gate dielectric reduces the field strength in general. The plot in figure 4.9 c) shows the potential and field strength along the cut line $\overline{AB}$ indicated in b) for three different thickness values of the dielectric layer. The high resistivity of the dielectric, compared to the depletion region, leads to a greater voltage drop. This is illustrated by the steeper slope of the potential function, indicated by the black lines in the green area. The direct consequence is a higher field strength in the dielectric (magenta lines in the green area). A thicker dielectric causes an overall larger voltage drop, but due to the stretch out over a longer distance, the actual electric field strength is reduced.

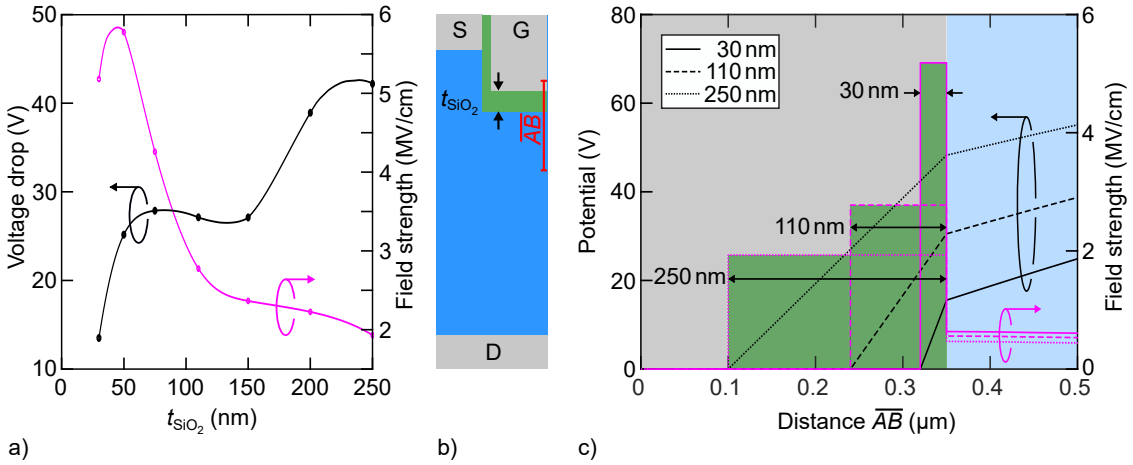

Figure 4.9: a) Dielectric field strength and voltage drop across the dielectric and the partially depleted drift layer for a 100 V potential difference between drain and gate. b) Schematic of the simulated structure. c) Potential and field strength along the cut line $\overline{AB}$ in b). The gray, green and blue shaded areas represent, the gate electrode, the dielectric and the drift layer, respectively. Three different dielectric layer thicknesses are plotted. The black lines represent the potential drop across the semiconductor and the dielectric layers with steepness depending on the dielectric layer thickness. The resulting field strength is plotted in magenta and constant across the dielectric layer.

One must keep in mind that a thicker dielectric also increases the threshold voltage, which usually limits the layer thickness to $\approx 100\,\text{nm}$. The solution is to keep the dielectric at the MOS channel thin while increasing its thickness at the trench bottom, where it experiences the most stress regarding field strength. This can be achieved by using a thick bottom oxide (TBOX). The process flow illustrated in figure 4.10 was used in this work to fabricate such a TBOX. Assuming a ready GaN trench, the first step is a conformal deposition of the dielectric with the desired thickness of the TBOX a). For this work, 300 nm LPCVD SiO_2 were used. For the next step, a layer of poly Si is deposited b). The layer thickness must be at least half the trench width so that the dent in the center is not to deep. Note that this also means that in order to keep the thickness of the poly Si within reasonable limits, a narrow trench is required. Otherwise the trench bottom would be revealed in the subsequent recess step c) where the poly Si is etched without any mask to obtain self alignment between the poly Si plug and the trench.

The TBOX is then structured by using time coupled wet etching in hydrofluoric acid. Subsequently, the poly Si plug is removed by using XeF_2 gas phase etching, which is highly selective and does not etch SiO_2 or GaN. The steps f) to h) are a) to c) repeated but with the dielectric layer thickness of 50 nm. This is the fabrication process of the actual gate structure. The gate dielectric is deposited, followed by the poly Si gate and once again a recess etching. A SEM cross section image of the resulting gate structure with TBOX is displayed in figure 5.3 a).

The recess gate is contacted by poly Si pads located at the ends of the trenches in the same way as done for the actual trench MOSFET, shown in figure 5.4 a). Backside contact formation and power metallization are performed as described in section 4.1.1 for planar MOS capacitors.

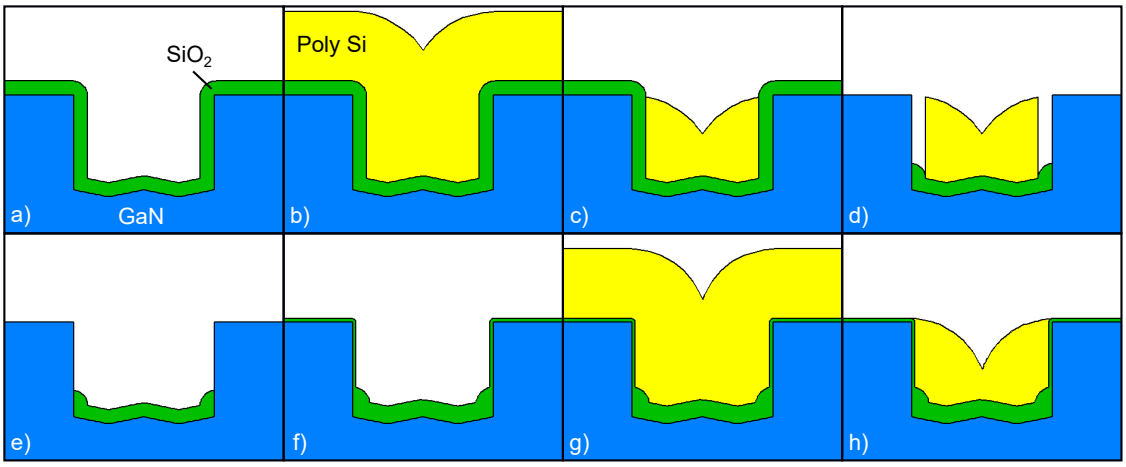

Figure 4.10: Schematic of the TBOX process flow used in this work. a) conformal deposition of the TBOX. b) deposition of a poly Si layer with thickness larger than half the trench width. c) recess etching of the poly Si layer. d) Isotropic and time coupled etching of the TBOX along the trench side wall. e) Removal of the remaining poly Si by using selective XeF_2 based gas phase etching. f) deposition of the actual gate dielectric, subsequent deposition g) and structuring h) of the poly Si gate.

4.2.2 Electrical characterization of trench MOS capacitors

Trench MOS capacitors were fabricated with and without TBOX and consisted of 10 parallel trenches that were oriented along either the a- or m-plane of the GaN crystal. Current density was calculated by using the combined area of trench sidewall and bottom (the latter only for devices without TBOX). Electrical characterization revealed substantial differences between the planar and trenched structures and trench orientation was found to have a noticeable effect. The plot in figure 4.11 a) shows IV-breakdown curves, measured at room temperature, for differently oriented devices with and without TBOX. The trench geometry is comparable to that of the trenches displayed in figure 3.18 b) and c). Structures with trenches oriented along the a-plane experience an earlier increase in leakage current and fatal dielectric breakdown. The reason is the unfavorable trench geometry with sharp corners at the trench bottom, as can be seen in the red framed

inset in figure 4.11 a). The smoother features of m-plane oriented trenches (green framed inset) reduce field stress on the dielectric and lead to a higher breakdown voltage. Note that the geometry of the m-plane trenches resembles that of the trench in figure 3.18 c) and not that in d). The reason for this is that both trench orientations were fabricated on the same wafer. To avoid over etching for the a-plane trench a compromise, with shorter etch time of 45 min, had to be made. Independent of the trench orientation, breakdown occurs generally earlier than for planar MOS capacitors. An improvement can be achieved by introducing the TBOX. As expected, the benefit for a-plane oriented trenches is more significant, yet their breakdown voltage lies still below that of their m-plane oriented counterparts. A likely reason for this is the sidewall surface roughness. As was illustrated in the SEM images 3.7 and 3.8, the a-plane sidewall features protruding corners, which are likely to cause field peaks and regions with reduced dielectric layer thickness. It should be noted that the breakdown voltage of planar MOS capacitors with identical gate dielectric and electrode was 40 to 45 V, and thus noticeable higher than for the trench structures, even with TBOX. Irregularities at the sidewall, non-conformal layer thickness and especially the ends of the trenches are likely culprits that cause the premature breakdown.

Another point worth mentioning is the increased gate leakage current in the low voltage region for devices with TBOX compared to those without. The reason for this is probably the twofold SiO_2 LPCVD procedure. Additional cleaning steps and the SiO_2 etching in hydrofluoric acid may also contribute to contamination and surface degradation. This should not be a problem for a finalized process flow in a production ready environment. However, since these requirements cannot be met during the course of this work and the TBOX is only an optional feature, which benefits mostly during the off-state, it was omitted in the process flow of the actual trench MOSFETs described in chapter 5. The plot in figure 4.11 b) shows the leakage current and breakdown field strength for a- and m-plane oriented trench MOS capacitors at 300 and 450 K. Note that in accordance with equation 2.31 for the Fowler-Nordheim current, no significant temperature dependence is observable.

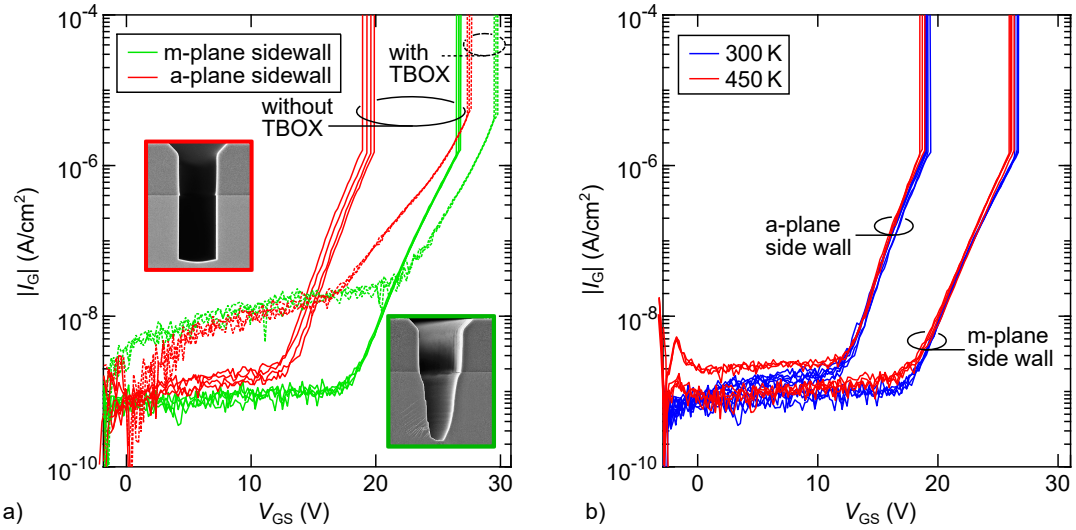

Figure 4.11: a) Room temperature IV-curves of trench MOS capacitors oriented along the a- and m-plane. Devices with and without TBOX were characterized. The inset SEM images show the geometry for trenches aligned along the a-plane (red) and m-plane (green). b) Temperature dependence of gate leakage current and dielectric breakdown voltage for differently oriented trench MOS capacitors without TBOX. Reproduced from [119], with the permission of the American Vacuum Society.

4.3 Impact of plasma related etch damage on leakage current and dielectric breakdown field strength

To evaluate the effect of intended and unintended surface pretreatment steps, MOS capacitors were fabricated on pristine and plasma treated surfaces. The process flow in figure 4.12 a) illustrates the surface treatment procedure, which was then followed by a standard MOS capacitor process flow as described in section 4.1.1, comprising a 50 nm LPCVD SiO_2 layer that was annealed for 1 h in 1 atm N_2 ambient at 800 °C.

The process starts with the deposition of a protecting LPCVD SiO_2 layer (fig. 4.12 a) (A)). This layer is lithographically structured and etched in buffered oxide etch (BOE) based on 7:1 hydrofluoric acid in H_2O in such a way (B), that one half of the wafer is exposed during the subsequent plasma etching (C). Following this, the remaining SiO_2 mask is removed in BOE (D) and substituted by a new one (F). Again the mask is structured only this time a 90° rotation is applied (G). During the following TMAH wet etching (H), part of the pristine surface and part of the plasma etched surface is exposed. After the removal of the second mask (I), the wafer features four quadrants Q1-4 that experienced different pretreatments. Q1 is pristine under the assumption that deposition and BOE removal of the SiO_2 mask did not alter the surface. Q2 was exposed to plasma etching without TMAH post treatment, while Q3 was exposed to plasma with subsequent TMAH treatment. Finally, Q4 was only TMAH etched without any exposure to plasma. Two wafers were fabricated, one with plasma conditions of the SF_6 GaN

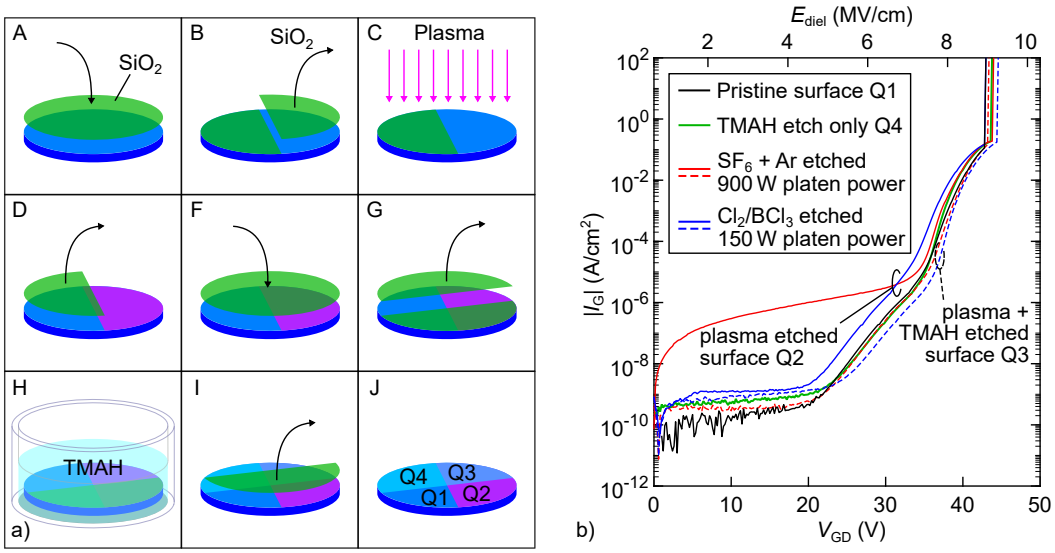

Figure 4.12: a) Process flow for the surface etch damage Experiment. b) Gate leakage current as function of gate-source bias and dielectric field strength for $5 \cdot 10^{-4}\,\mathrm{cm}^2$, planar MOS capacitors on differently treated GaN surfaces.

trench etching process and one with plasma conditions corresponding to a chlorine based trench etching procedure. Due to the volatility of the $GaCl_3$ etch product, the latter uses less physical etching and plasma induced damage is likely to be less severe than for the more aggressive etching based on SF_6 and argon. This presumption is confirmed by the results of the breakdown measurements presented in figure 4.12 b). The solid IV-curves correspond to the surface area Q2, which was exposed to plasma etching without TMAH post treatment. Breakdown voltage is comparable and seemingly not affected by the plasma etching procedure. This is to be expected, since LPCVD SiO_2 is amorphous and the bulk material, responsible for the breakdown voltage, should be unaffected by the GaN surface condition. However, the interface layer can affect the electron barrier and thus the gate leakage current density. This can be observed in the plot in figure 4.12 b). High plasma etching with high platen power is likely to cause impurity incorporation and crystal damage near the surface. This generates surface states and increases leakage current. The effect is only marginal for the sample that was subjected to the chlorine plasma with lower power. Interestingly, TMAH wet etching after the plasma treatment rebuilds pristine surface conditions, even for the heavily damaged SF_6 sample.

To evaluate possible correlation between the electrical properties and the surface roughness due to plasma etching, AFM scans were conducted on the SF_6 sample with the results presented in figure 4.13. By combining these scans with the IV-curves in figure 4.12 b), the following can be concluded. The RMS roughness of Q3, i.e. plasma+TMAH treatment, is similar to that of Q2, which was plasma etched but not exposed to TMAH. The wet etching leads to a coarser appearance as gradual leveling of the plasma generated topography takes place, but peak height and overall roughness remains comparable. Yet there is a significant difference in the leakage current density for MOS capacitors fabri-

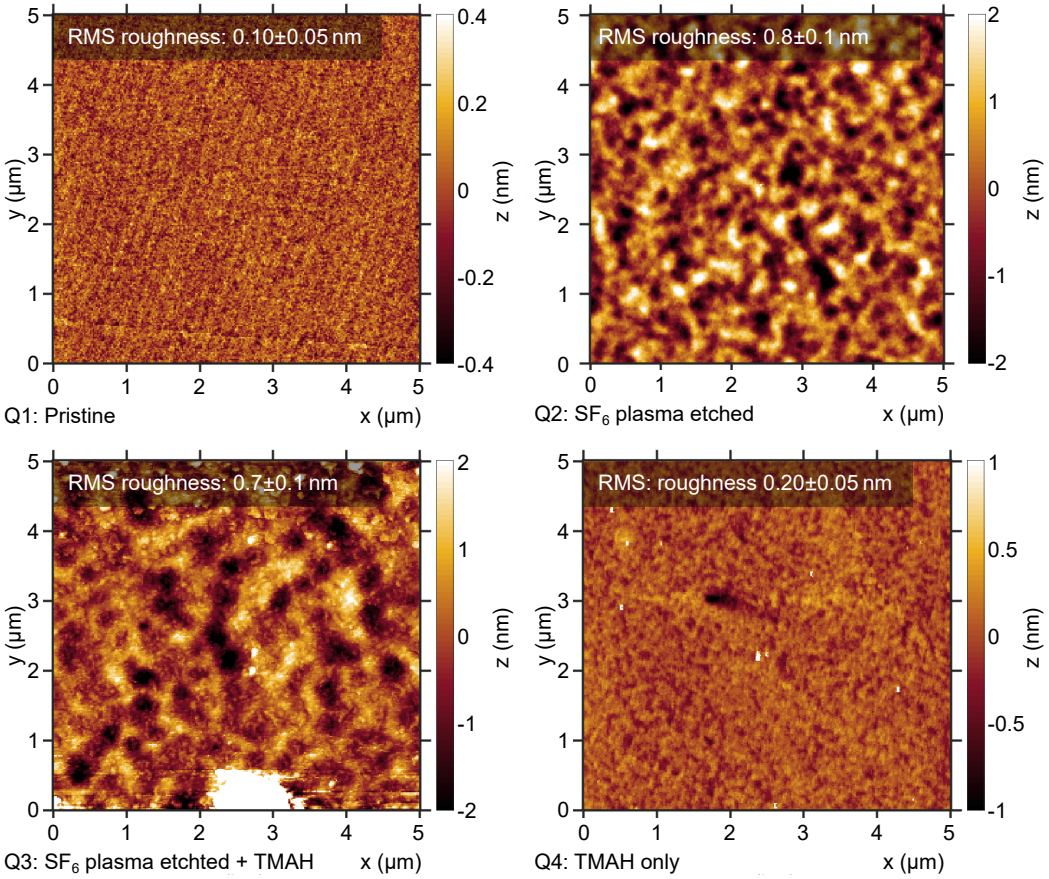

Figure 4.13: AFM measurements of differently treated Ga-face surfaces. The notation Q1-4 refers to the schematic in figure 4.12 a). The bright white spots in Q3 and Q4 are du to particle contamination.

cated on these surfaces. This suggests that surface roughness has no observable effect, neither on leakage current, nor on breakdown field strength. The same is true for a comparison of Q1 and Q3 (same for Q4 and Q3). In this case, roughness is different, yet the measured IV-curves for the MOS capacitors on the respective surfaces are nearly identical. This experiment answers the question stated at the beginning of section 3.2, regarding the effect of plasma- and wet etching on the GaN interface. As can be seen from the SEM images in figures 3.6 and 3.18, plasma induced damage is confined to the bottom region of the trench. A significant amount of GaN is removed via wet etching from the sidewall, which makes plasma damage at the actual MOS interface unlikely. The results in figure 4.12 b) show that leakage current and breakdown field strength of the dielectric are not affected if TMAH post treatment is applied. These are the two requirements at the trench bottom. Since no MOS channel forms in this area, a potential effect on the inversion carrier mobility is not relevant, at least not in the case of a trench MOSFET. However, regarding current spreading at the end of the MOS channel, carrier accumulation in the region of the trench bottom can have a relevant impact in terms of on-resistance. To examine the effect of plasma etching on a MOS interface, planar

MOSFETs were fabricated on a Q4-surface. The fabrication of these devices and the corresponding evaluations are presented in chapter 5.

5 Planar and trench GaN MOSFETs

Based on the process steps and findings discussed in chapters 3 and 4, lateral and trench MOSFETs were fabricated and characterized. The related procedures are described in this chapter. After a statement on the research objective, the process flow for both device types is described. This is followed by a discussion of the results from various electrical characterizations. The chapter concludes with a direct comparison of lateral and trench MOSFET. The content of this chapter includes, but is not limited to information that was already published [119].

5.1 Objectives for the fabricated MOSFETs

The main objective of this work is the fabrication and characterization of trench MOSFETs on native gallium nitride substrates, with the focus being the MOS-gate structure. In accordance with the findings regarding trench fabrication (cf. chapter 3) and MOS structure (cf. chapter 4), trench MOSFETs with metal-free gate structure were fabricated. Note that the MOS capacitors allowed no conclusion towards inversion channel carrier mobility and that gate dielectric and electrode were selected in accordance with their robustness regarding leakage current and breakdown field strength. In order to obtain information about the inversion channel performance, actual MOSFETs must be fabricated. The procedure can be separated into three major building blocks.

- Growth of epitaxial layers: Externally processed and described in section 5.2.1.
- Fabrication of the gate trench and its post treatment: Discussed in chapter 3.
- Development of the actual gate, including dielectric layer and gate electrode: Described in chapter 4.

Combining the findings regarding trench and MOS gate fabrication, a process flow for the trench MOSFET was set up and will be described in detail in section 5.2. Lateral MOSFETs, as illustrated in figure 2.15 b), were fabricated as well. This allowed a comparison between vertical and planar MOS interfaces and helps to put findings concerning the trench MOS inversion channel carrier mobility into perspective. Furthermore, the results for lateral MOSFETs can be used as performance indication for a VD-MOSFET. This allows, to a certain degree, a performance comparison between trench and VD-MOSFET.

As shown in figure 2.4, several resistance components are present in a trench MOSFET. Since for this work only the channel resistance is of interest, it is advisable to reduce the

other components as far a possible. Therefore, drift layer doping was chosen comparably high and drift layer thickness thin. Furthermore, no shielding structures were incorporated and breakdown measurements are not included in the characterization procedure. Device evaluation will focus on

- MOSFET transfer and output characteristic
- Hysteresis of the transfer curves
- Resistance components and device on-resistance
- Field effect channel mobility
- Threshold voltage stability

5.2 Fabrication procedure for trench MOSFETs and lateral MOSFETs

This section is a detailed description of the fabrication procedure for the trench MOSFETs. The lateral MOSFETs were fabricated in parallel on the same wafer and due to several similar or identical steps, their description is included. For the sake of clarity not all process parameters are mentioned, instead an exhaustive list of the process steps and parameters is provided in the appendix A.6. A schematic of the process flow for trench and lateral MOSFET is depicted in figures 5.1 and 5.2, respectively.

5.2.1 Epitaxial layer stack

All devices were fabricated without ion implantation and are based solely on epitaxial doping. The layer stack was fabricated externally at the Ferdinand Braun Institute in Berlin. The properties of the various layers are listed in table 5.1.

The first layer that is grown on top of the 500 µm Ga-face GaN substrate is an n-type buffer stack. For GaN epitaxy on foreign substrates, a highly elaborated buffer is required to achieve reasonable compatibility between GaN and lattice crystal. For epitaxial layers on native substrates, the buffer is less critical yet necessary to improve growth quality on the chemical mechanical polished substrate surface. Furthermore, it improves the electrical connection between drift layer and substrate as it acts as current spreading layer due to the higher doping concentration. Following the buffer stack, the lower doped drift layer is grown. The relatively high doping concentration, in conjunction with a thin layer thickness, ensures a low impact of the drift layer on the total on-resistance of the device. Contrary to the drift layer, the p-base layer was chosen thicker than necessary to increase the impact of channel resistance. The crucial point for this layer is the magnesium activation, which is achieved by in situ tempering. This has the advantage that

passivating hydrogen from the precursor gases in the epitaxial growth process, incorporated in the p-type GaN crystal, is removed effectively. Ex situ activation is less effective since subsequently grown layers, especially of n-type, were found to hamper hydrogen out diffusion [136]. After the activation procedure, the n-source layer stack is grown. A low temperature interlayer is added to reduce stress and lattice defect generation and to prevent magnesium diffusion from the p-base layer into the n-source layer. The n-layer stack is finalized with a highly doped capping, which facilitates achieving low-resistance ohmic source contacts.

Table 5.1: Specifications of the epitaxial layers and the GaN substrate.

Layer	Thickness (nm)	Carrier conc. (cm^{-3})	doping type	in-situ activation time at 880 °C
source cap 2	30 ± 5	1e19	n	-
source cap 1	200 ± 10	3e18	n	-
source	100 ± 10	3.5e18	n	500 s
p-base	500 ± 10	1e17	p	1000 s
n-drift	5000 ± 50	1e17	n	-
buffer 2	3000 ± 30	3e18	n	-
buffer 1	100 ± 10	3e18	n	-
n-substr.	$400\text{k} \pm 30\text{k}$	$>$ 1e18	n	-

5.2.2 Mesa and trench fabrication

The plasma and wet etching technique, used during the MOSFET fabrication procedure, was described in detail in chapter 3. Apart from the actual trench etching, mesa structures as illustrated in figure 5.1 b), were fabricated as well. The n-source mesa etching removes all n-type material above the p-base layer and thus creates isolated source and drain areas that are required for the lateral MOSFET (fig. 5.2 b)). The required etching depth is only 350 to 400 nm, enough to ensure a complete removal of the n-source layer. Afterwards, TMAH wet etching is applied to remove GaF_3 and to reduce surface roughness at the mesa sidewalls. Although this is irrelevant for the trench MOSFET, the lateral device relies on an accumulation and inversion channel at the n-source mesa sidewall, as can be seen in figure 5.2 b).

The p-mesa etch reaches into the drift layer and separates different devices from each other. The required etch depth is the same as for the actual gate trench. Therefore, both steps were combined. Wet etching post treatment, as described in section 3.2, is especially relevant after this etching step and is performed for 45 min in 25 % TMAH at 90 °C. The main reason is the improvement of the trench sidewall and geometry in the bottom region. In addition, step transitions between areas that where subjected to one or two mesa etch procedures become smoother. This circumstance is shown exemplarily in the SEM images b) and c) in figure 5.3.

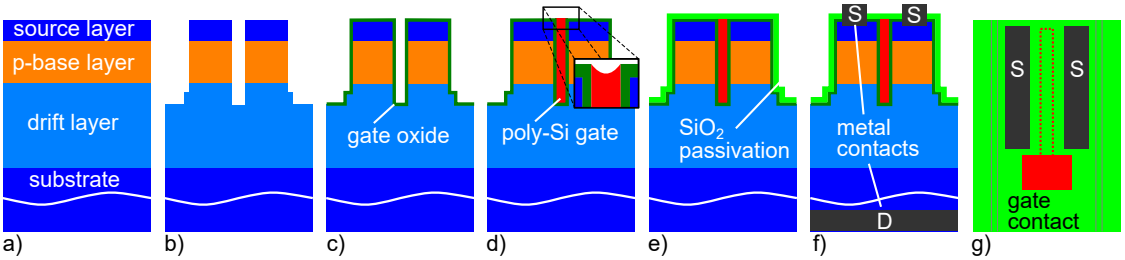

Figure 5.1: Schematic process flow for the trench MOSFET. a) Epitaxial layer stack. b) Topography after the p-mesa/trench etching procedure. c) Conformal deposition of the gate oxide layer. d) poly Si gate after recess etching. e) Deposition of the passivation layer, followed by contact formation f). g) Top view of the final device with the trench indicated by the red dashed line. Reproduced from [119], with the permission of the American Vacuum Society.

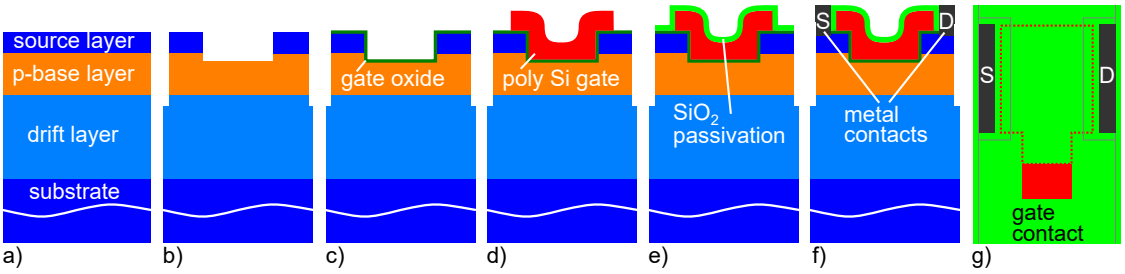

Figure 5.2: Schematic process flow for the lateral MOSFET. a) Epitaxial layer stack. b) Topography after n-source and p-mesa etching. c) Deposition of the conformal gate oxide layer. d) Structured gate poly Si. Note that no recess process is applied. Deposition of the passivation layer e) and formation of drain and source contacts f). Top view of the final device with the gate electrode indicated by the red dashed line.

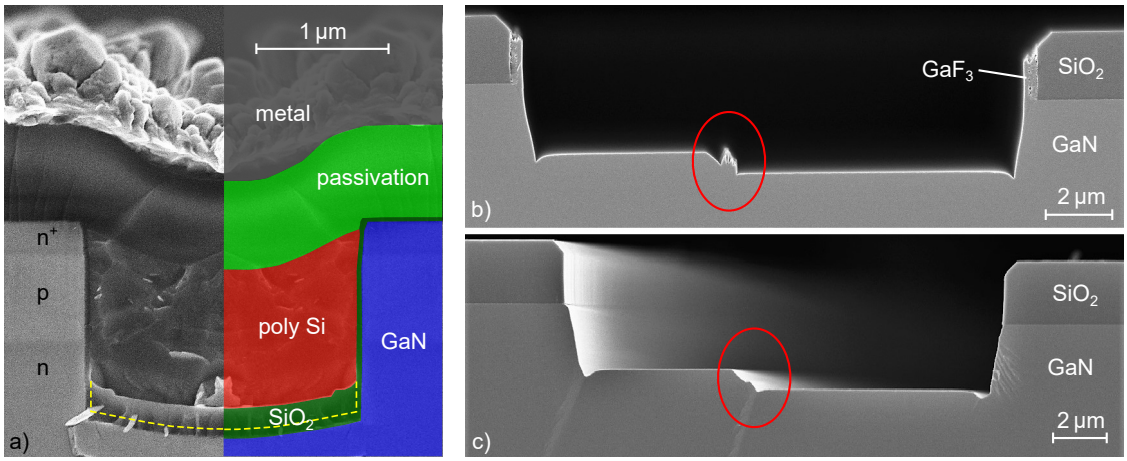

Figure 5.3: a) SEM cross section image of a trench MOSFET gate structure with thick bottom oxide layer. The yellow dashed line indicates the shape of the gate oxide layer for a standard device. b) SEM cross-section image of a mesa transition step after plasma etching and c) after wet etching post treatment. Reproduced from [119], with the permission of the American Vacuum Society.

5.2.3 MOS gate structure

The fabrication procedure is essentially the same as for the trench MOS capacitors without TBOX, which was described in section 4.2.1. The nominal thickness of the dielectric layer, consisting of LPCVD SiO_2, was 50 nm. Based on the findings from section 4.1.2, the dielectric was annealed with the same parameters, that is 1 h at 800 °C in 1 atm N_2 ambient and covered with a poly Si layer as gate electrode. The recessed gate was contacted at both ends of the five parallel trenches. Figure 5.4 a) shows a SEM top view image of such a trench MOSFET with an exemplary trench and the source contact area indicated in red and blue, respectively. For the lateral MOSFETs, no recess process is applied. Instead, the gate area is covered by photoresist during the recess etching step, resulting in a gate structure as depicted in figure 5.2 d). To avoid pressure from the metal probing tip during electrical characterization and to allow comfortable contacting for devices with short channel length, a remote gate electrode was fabricated (cf. fig. 5.2 g) and 5.4 b)).

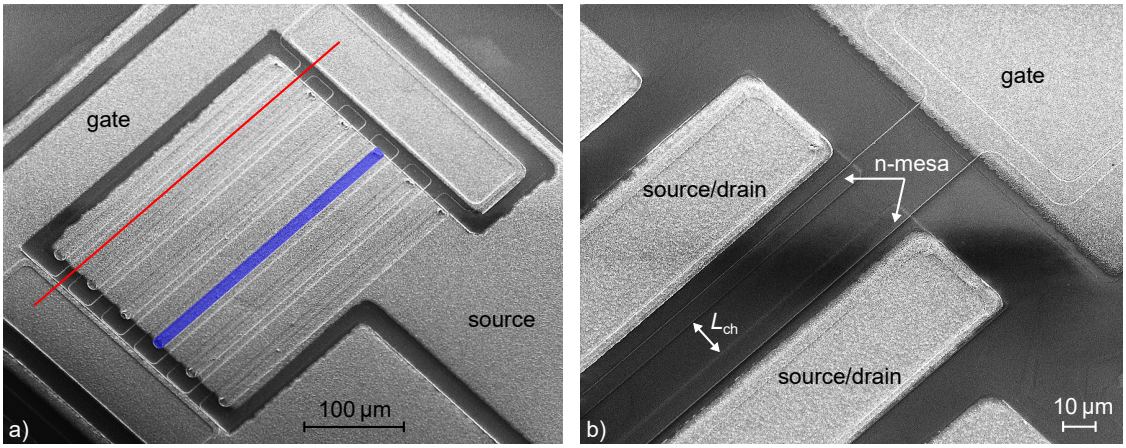

Figure 5.4: a) Inclined SEM top view image of a five finger trench MOSFET with the exemplary location of a trench in red and the source contact area in blue. b) SEM image of a lateral MOSFET with 15 µm channel length L_{ch}. Note that drain and source pad are ambiguous as both current flow directions are identical. Reproduced from [119], with the permission of the American Vacuum Society.

5.2.4 Contact formation

The deposition of the passivation layer concludes the metal-free front-end processing. Back-end processing starts with the creation of source (and drain for lateral MOSFETs) contact openings in the passivation layer. Following a lithography step, ICP SiO_2 soft etching is used. Compared to the trench etching mask, the passivation layer thickness is only 800 nm. The aspect ratio is much smaller and sidewall steepness, as well as broadening effects, are uncritical. The lower etching power allows a resist mask, which simplifies the process step. To avoid potentially harmful plasma damage on the GaN surface, the final 50 nm of passivation oxide are etched in BOE. After the creation of the

openings, a titanium/aluminum stack of 20/100 nm is sputtered onto the wafer. Since wet etching, especially with an titanium layer included, can be problematic for the small source contacts, a lift-off procedure, as illustrated in figure 5.5, is performed for the metal layer structuring. The photoresist, used for the lithography that designated the front side contact openings, remains on the wafer and the metal stack is sputtered on top of it (fig. 5.5 b)). With the first layer of resist covered by the titanium/aluminum stack, a second lithography step is applied with a mask inverse to the first one c). That is, only the openings in the passivation layer are covered with resist. Using ion bean etching, i.e. physical bombardment with argon atoms, the unprotected metal layer is removed d). Following this, the resist is stripped in a combination of wet- and plasma stripping, which removes metal residues located at the mesa sidewalls e), where they were shielded from the ion beam etching. The featureless wafer backside is subjected to the same sputtering procedure but no structuring steps are required. The contact is annealed with the standard procedure stated in the appendix A.6. After the annealing, additional openings are created in the passivation layer for the gate electrode. Again ICP SiO_2 soft etching is used. Since in this case the etching stops on the poly Si gate pads, no damage free wet etching is required. Following this, the power metallization layer, consisting of 800 nm aluminum, is sputtered onto the front and backside of the wafer and finally, the front side is structured using lithography and aluminum wet etching.

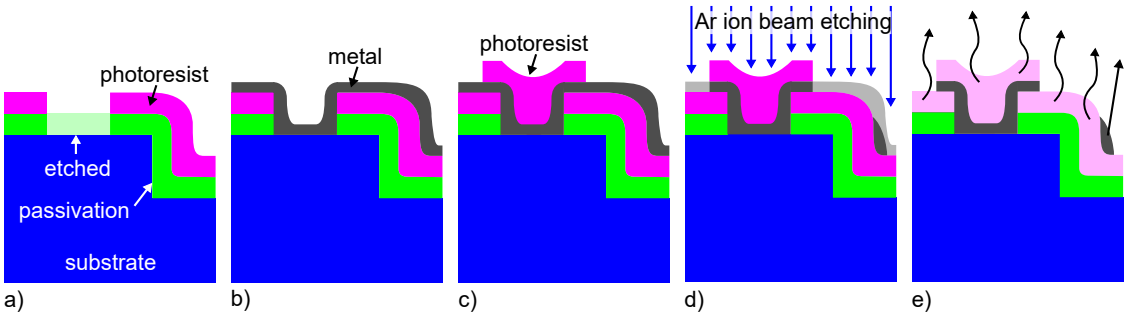

Figure 5.5: Schematic process flow of the lift-off procedure. a) Lithography and ICP SiO_2 plasma etching to generate openings in the passivation layer. b) Sputter deposition of the metal stack. c) Lithography with an inverse mask to cover the contact area followed by argon ion beam etching d) to remove the unprotected metal. e) Resist stripping removes metal remnants that were shaded by the mesa topography.

This concludes the fabrication process for trench and lateral MOSFETs. SEM top view images of a trench a) and planar b) MOSFET are presented in figure 5.4. The SEM cross section image in figure 5.3 a) shows the various layers for a device with thick bottom oxide in the trench. The yellow dashed line indicates the shape of the gate oxide for the standard configuration without TBOX. As discussed in detail in chapter 3, there is a significant difference between trenches that are orientated along the a- and m-plane, respectively. Trench MOSFETs were thus oriented in such a way that their trenches are parallel to either of the vertical crystal planes. They are labeled accordingly as a- or m-plane oriented and electrical results, discussed in section 5.3, refer to these labels.

Concerning the planar MOS channel, no measurable crystal related influence is to be expected. This can be concluded from SiC devices were only a small effect is to be observed, despite the impact from the off-axis cut. Nonetheless, lateral MOSFETs are oriented in such a way that the current flow direction through the planar MOS channel is either parallel to the a-direction $[\bar{1}2\bar{1}0]$ or the m-direction $[10\bar{1}0]$. Again, electrical results are labeled accordingly.

5.3 Electrical characterization of trench MOSFETs

All measurements were performed on trench MOSFETs with 16 µm pitch size and five parallel trenches of 210 µm length. Current density is normalized to the active area of the device $A = 1.92 \cdot 10^{-4}\,\mathrm{cm}^2$. Since both trench orientations were fabricated on the same wafer, wet etching conditions were the same as well. The geometry of the a-plane oriented trench thus resembles the one depicted in figure 3.18 b), while that for the m-plane trench resembles the one in figure 3.18 c).

5.3.1 Transfer characteristic of trench MOSFETs

The transfer characteristic was measured for a constant drain source bias of $V_{\mathrm{DS}} = 0.1\,\mathrm{V}$, which mimics real operation. A sweep rate of 1 V/s was used for gate-source voltages between -5 and 15 V, which allowed a reasonably high resolution of the leakage current. The maximum gate-source bias was set to a value just before the onset of measurable gate leakage current.

The transfer curves of two exemplary MOSFETs, with trenches oriented along the a- and m-plane, are depicted in figure 5.6. The measurement was performed as three consecutive loops at a temperature of 300 K. Both devices perform equally well with only minor differences in the transconductance. Excluding the first loop, loop to loop difference as well as hysteresis between up and down sweep are small. Since the latter is relevant for the calculation of the field effect mobility, it will be described in that context in more detail in section 5.3.4. The difference between loop one and two suggests that the interface condition is changed during the initial operation. A similar phenomenon was observed for the leakage current density of MOS capacitors in section 4.1.2. Although no gate leakage current beyond noise is observable for the trench MOSFETs, an effect on the drain current can be noticed. According to the statements in section 2.6.3, the general right shift of the transfer curve, after the initial loop suggests the incorporation of negative charge at the interface.

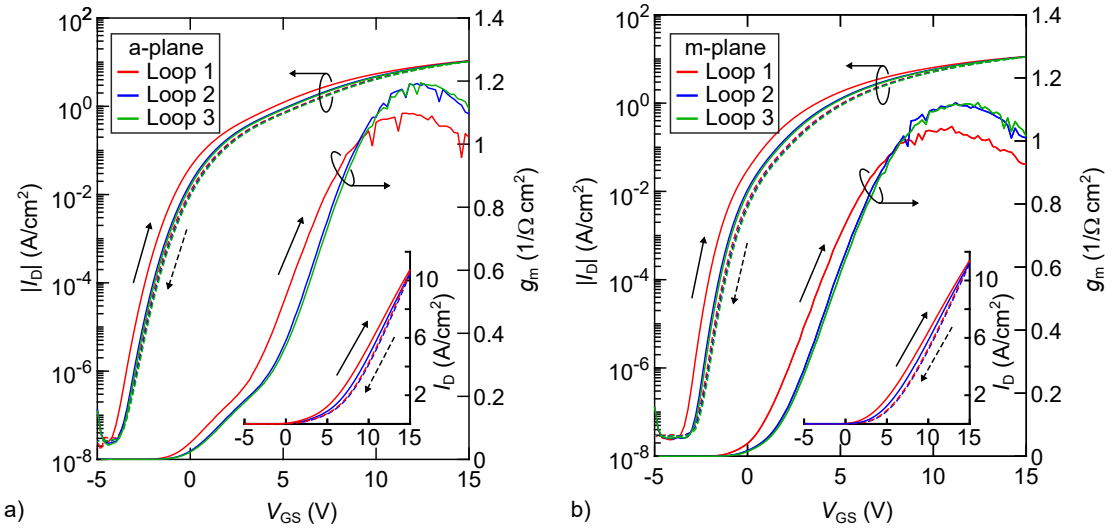

Figure 5.6: Room temperature transfer characteristic and transconductance of trench MOSFETs with trenches oriented along the a-plane a) and m-plane b). Three consecutive loops were measured with solid and dashed lines, representing up and down sweep, respectively. The inset shows loop one and two on a linear scale.

A more significant difference is observed if the devices are measured at different temperatures. The corresponding results are presented in figure 5.7. Again, both devices behave in a similar way, that is an increasing right shift for elevated temperatures and a decrease in drain current density. The current ratio at $V_{GS} = 15\,V$ is $I_{DS}(300K)/I_{DS}(450K) = 1.5 \pm 0.2$ for a-plane oriented devices and 1.2 ± 0.2 for m-plane oriented devices. The significantly steeper increase of drain current near the threshold voltage could be explained with reduced impact of donor like interface traps due to faster detrapping at higher temperature. A comparison of the measured transfer curves in figure 5.7 with the simulated counterpart in figure 2.17 c) supports this assumption. The lower drain current at $V_{GS} = 15\,V$, for curves measured at elevated temperature, is only partially caused by the said right shift. The main reason is a lower transconductance. As described in section 6.1.2, the bulk mobility should increase in this temperature regime. This emphasizes that the higher device resistance is due to a decrease in channel conductivity. Typically, higher temperature leads to faster detrapping and thus better channel mobility [137]. In this case however, it seems likely that an elevated temperature increases the amount of accessible acceptor like interface defects, especially near the conduction band edge. This causes a more negative interface if the defects get ionized and reduces the drain current in the regime of higher gate bias.

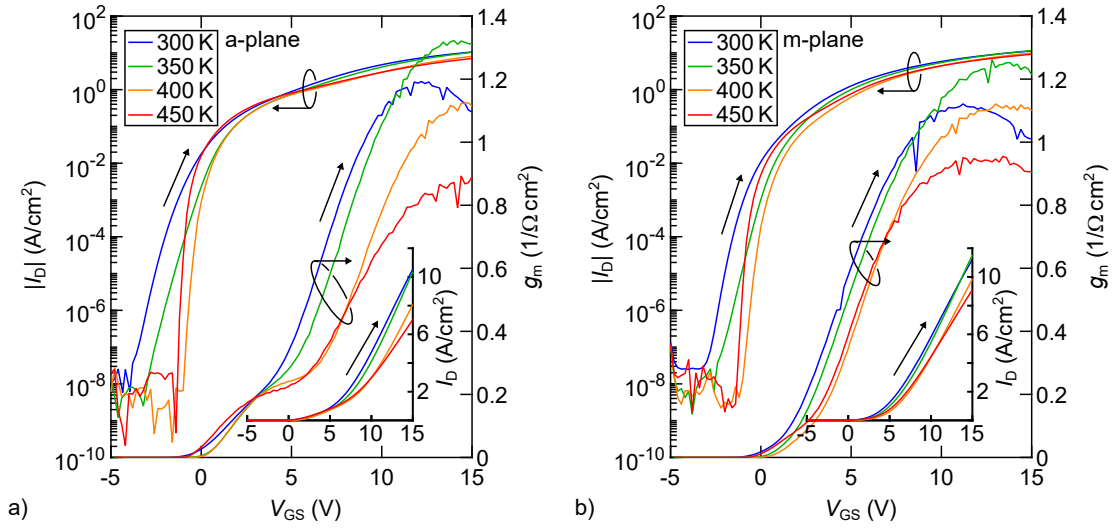

Figure 5.7: Temperature dependent transfer characteristic and transconductance of trench MOSFETs with trenches oriented along the a-plane a) and m-plane b). The insets show the transfer curves on a linear scale.

5.3.2 Threshold voltage evaluation of trench MOSFETs

Despite the right shift of the transfer curve at elevated temperature, the drain current density at zero, and even negative gate bias, is relatively high. Such an early onset of drain current flow is unusual for a MOS inversion channel, although Yoshino et al. [42] reported a similar phenomenon for a VD-MOSFET. Using the method of extrapolation in the linear region [109] to determine the threshold voltage from the room temperature transfer curves, $V_{\mathrm{th}} = 5 - 7\,\mathrm{V}$ is obtained. However, the logarithmic plot clearly shows a significant current flow at much lower gate source bias. There is no clearly defined way to determine V_{th} and no fix value will be stated for the devices in this work. However, the logarithmic transfer curves in figure 5.6 show a drain current onset between $V_{\mathrm{GS}} = -2$ and $0\,\mathrm{V}$. This is below the theoretical threshold voltage, which was calculated via

$$\begin{aligned} V_{\mathrm{th}} &= V_{\mathrm{FB}} + 2\Phi_{\mathrm{F}} + \frac{\sqrt{4\varepsilon_0\varepsilon_{\mathrm{GaN}} N_{\mathrm{A}}^{-} \Phi_{\mathrm{F}}}}{C_{\mathrm{ox}}^{*}} \quad \text{with the Fermi potential at the interface} \\ \Phi_{\mathrm{F}} &= \frac{k_{\mathrm{B}}T}{q} \ln\left(\frac{N_{\mathrm{A}}^{-}}{n_{\mathrm{i}}}\right) \end{aligned} \tag{5.1}$$

as $V_{\mathrm{th_{theory}}} = 3.7 \pm 0.6\,\mathrm{V}$, by using the literature value for the intrinsic carrier density $n_{\mathrm{i}} = 1.9 \cdot 10^{-4}\,\mathrm{cm}^{-3}$ [94] and flat band voltage $V_{\mathrm{FB}} = (-3.2 \pm 0.2)\,\mathrm{V}$ as well as the area specific oxide capacitance $C_{\mathrm{ox}}^{*} = (7.3 \cdot 10^{-4} \pm 7 \cdot 10^{-6}\,\mathrm{F/m^2}$ from the SiO_2 MOS capacitors described in section 4.1.2. Due to adverse effects from trench bottom and corners, these quantities were obtained from measurements performed on planar MOS capacitors. Since C_{ox}^{*} is measured in accumulation, it is mostly independent from the semiconductor and

the interface. Therefore, this approach is valid as long as the oxide thickness is identical for planar and trench structure. Due to the high conformity of LPCVD SiO_2 this criterion is fulfilled as well.

There are several explanations for the discrepancy between the measured onset of drain current and the theoretical threshold voltage. The first one is a thin layer of n-type material at the MOS interface, which could be created by diffusion of silicon [138] during the deposition and annealing process of the gate dielectric layer. The silicon acts as counter dopant to the magnesium in the p-base layer and reduces the hole concentration, this in turn reduces the threshold voltage (cf. eq. (5.1)). Depending on the amount of incorporated silicon, a conversion to intrinsic, or even n-type material, could be possible. The latter would lead to an accumulation channel and thus a parallel conduction path that is closed only at a significantly lower gate-source voltage that would be the case for an inversion channel alone. The second hypothesis assumes a similar effect due to hydrogen diffusion [139] during the SiO_2 deposition from the dichlorosilane precursor. Hydrogen passivates the incorporated magnesium and reduces the p-type character near the surface. Although no accumulation would occur, threshold voltage could be lowered significantly. Yet another explanation is the formation of a gallium rich surface layer due to nitrogen loss during high temperature process steps [140]. The formation of such a quasi conductive layer could have a consequence similar to the diffusion of silicon or hydrogen. The final hypothesis assumes a high density of positive charges at the interface and in the dielectric layer [84], which lead to a left shift of the transfer curve. This would be in agreement with the low flat band voltage observed for planar MOS capacitors in section 4.1.2. Since it is deemed the likeliest and most relevant factor, the following experiment was conducted to further examine the effect of interface charges as the reason for the low threshold voltage.

After the measurement of a reference transfer curve, a gate-source bias of -5 V was applied and drain-source bias was ramped up in 6 sec from 0 to $V_{\mathrm{DS_{load}}} = 1, 3, 5, 7$ and 9 V. After the ramp up to 1 V, a transfer curve was measured followed by a ramp up to 3 V and so on. The resulting transfer curves are plotted in figure 5.8 a) for $T = 300$ K and b) for $T = 450$ K. At room temperature, a clear right shift depending on $V_{\mathrm{DS_{load}}}$ is observed. Interestingly, the effect is not observed at high temperature. Although the shift did occur, the relaxation time for the interface to fall back to the default, i.e. more positive state, was too short for the effect to be detected via the subsequent transfer curve measurement. This rules out the diffusion and gallium related hypotheses as main reason, since their corresponding influence should be mostly unaffected by gate bias and temperature. The right shift due to higher temperature, mentioned in section 5.3.1, is still observable and independent from time.

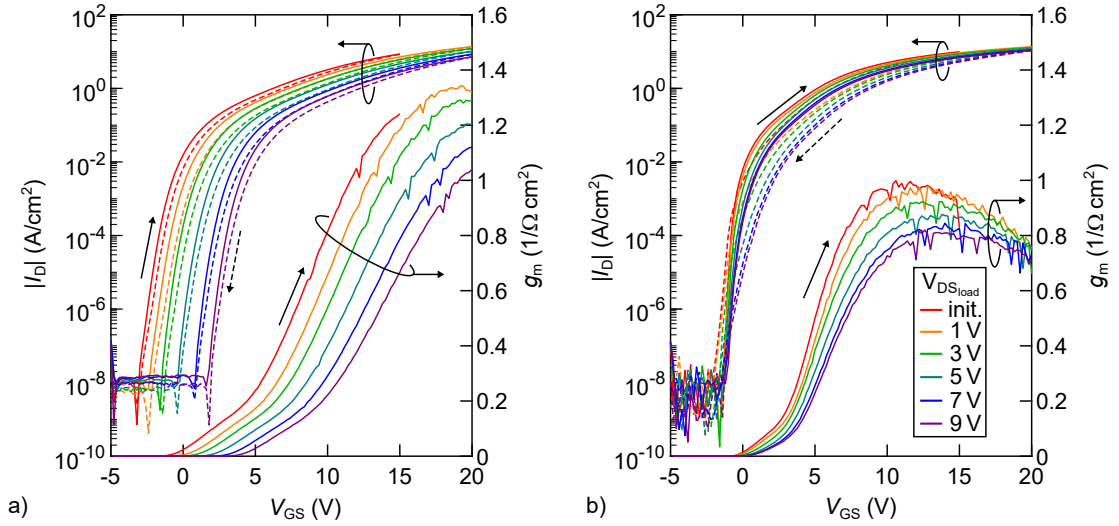

Figure 5.8: Transfer characteristic and transconductance of trench MOSFETs after different drain-source load voltages $V_{\mathrm{DS_{load}}}$ at $T = 300\,\mathrm{K}$ a) and $T = 450\,\mathrm{K}$ b). Note that the initial measurement was performed up to 15 V gate-source bias only. Reproduced from [119], with the permission of the American Vacuum Society.

The unstable character of the observed effect suggests a high number of acceptor like defect states at the interface. Their negative character, if ionized, shifts the transfer curve to the right. Their influence increases as gate bias rises and more acceptors get ionized. This leads to the observed drop in transconductance resulting in lower drain current density and their increasing influence with rising gate bias.

5.3.3 Output characteristic of trench MOSFETs

The output characteristic was measured by setting a fixed gate-source bias while sweeping V_{DS} from 0 to 10 V with 0.2 V/s. The resulting measurement curves are presented in figure 5.9. The plot in a) shows the median curves for a- and m-plane oriented devices in red and green, respectively. Linear and saturation region are clearly distinguishable for $V_{\mathrm{GS}} = 15\,\mathrm{V}$. Although a generally higher drain current is observed for m-plane oriented devices, the difference is not significant.

However, it should be noted that the curves for $V_{\mathrm{GS}} < 15\,\mathrm{V}$ deviate strongly from the theoretically expected shape. This is illustrated exemplary by the dotted line for $V_{\mathrm{GS}} = 12.5\,\mathrm{V}$. The pronounced linear behaviour indicates a parasitic current path that is triggered at a lower gate bias. As soon as the MOS channel is fully activated ($V_{\mathrm{GS}} = 15\,\mathrm{V}$) this path becomes negligible and the output characteristic looks as expected. A possible root cause for such a parasitic path could be the vertical corners at both ends of the trenches where inversion might occur earlier due to field crowding. Another possibility is the degraded MOS interface as described in section 5.3.2 which also might offer a current path at moderate gate bias.

The plot in b) shows the median curve for different temperatures again for a-plane orientation (dashed line) and m-plane orientation (solid line). As for the transfer characteristic, increasing temperature leads to reduced drain current. Temperature related current ratios at $V_{DS} = 10\,V$ are $I_{DS}(300K)/I_{DS}(450K) = 1.8 \pm 0.3$ and 1.5 ± 0.3 for a- and m-plane oriented devices, respectively.

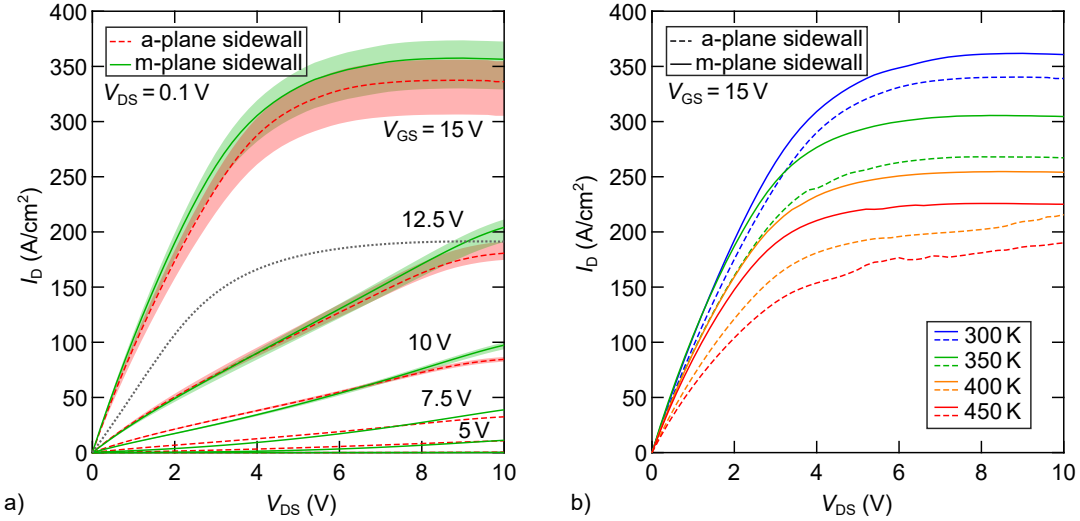

Figure 5.9: Output characteristic of trench MOSFETs oriented along the a-plane in red and along the m-plane in green. a) Median device from the wafer center area measured for different gate-source voltages at room temperature. The shaded area represents the fluctuation across the center region of the wafer. b) Median device for a- and m-plane orientation as dashed and solid lines, respectively, and measured at different temperatures. Reproduced from [119], with the permission of the American Vacuum Society.

5.3.4 Inversion channel field effect mobility of trench MOSFETs

A crucial quantity regarding channel conductivity is the carrier mobility. Due to several effects, mentioned in section 2.4.4 and also discussed in section 6.2, the carrier mobility in the MOS inversion channel can be significantly lower compared to that in bulk material. To examine the interface quality, the field effect mobility, introduced in section 2.4.4 is calculated. To determine the corrected drain current via equation (2.29), the various resistance components must be measured and calculated. The following components were taken into account:

- Source contact resistance $R_{\text{cont.S}}$
- Source feed resistance R_{source} (resistance between source contact and channel entry)
- Spreading resistance R_{spread} (resistance due to current crowding at the channel exit)
- Drift layer resistance R_{drift}
- Substrate resistance R_{substr}

- Backside drain contact resistance $R_{\text{cont.D}}$

All resistance components are measured and calculated in Ohm for the specific transistor type that is evaluated.

Source contact resistance: To determine this component, and to verify the quality of the source contact in general, transfer length module (TLM) measurements (cf. appendix A.5) were carried out. Inverse IV-curves for various pad distances D_{Pad} and different temperatures are plotted in figure 5.10 a) with the resulting resistance presented in b). As can be seen from the linearity of the inverse IV-curves in a), the contacts possess good ohmic behavior and the fit for various pad spacings in b) is good. The calculated sheet- and specific contact resistances along with the transfer lengths are presented in figure 5.11 a), b) and c), respectively. For the examined device, with a source contact area of 43 %, this refers to an absolute source contact resistance of $R_{\text{cont.S}} = (0.46 \pm 0.12)\,\Omega$ at room temperature. In the context of literature [74], this value can be regarded as good and the impact on device performance is expected to be marginal.

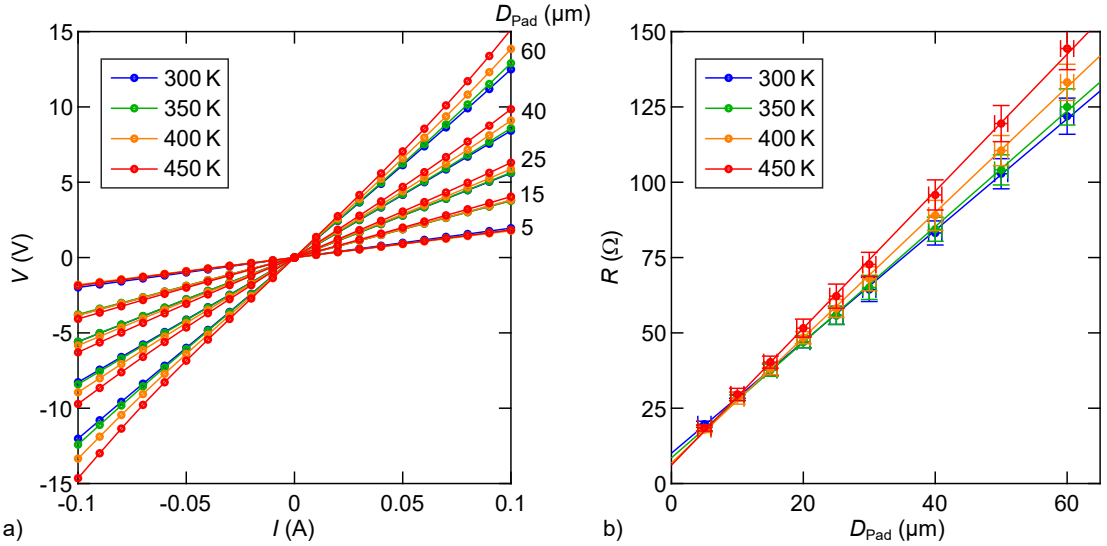

Figure 5.10: Temperature dependent TLM measurement results for the source contacts. a) Inverse IV-curve for different pad spacings D_{Pad}. b) Resulting pad to pad resistance and linear fit.

Source feed and spreading resistance: Feed and spreading resistance cannot be measured and are only accessible via TCAD simulation. Using the calibrated device setup described in chapter 6, the voltage drop between source contact and channel entry was used, in combination with the simulated drain current, to calculate $R_{\text{source}} = (0.8 \pm 0.2)\,\Omega$. A similar probing was performed between channel exit and a point in the drift layer where current density was several magnitudes below that at the channel exit. The obtained spreading resistance was $R_{\text{spread}} = (1.1 \pm 0.3)\,\Omega$. A close-up of the channel region displaying the absolute value of the current density on a logarithmic scale is depicted

in figure 5.12 a). The blue circles indicate the probing positions for R_{source} and R_{spread}. Note that the first probing site for R_{source} is at the source contact, which is not shown.

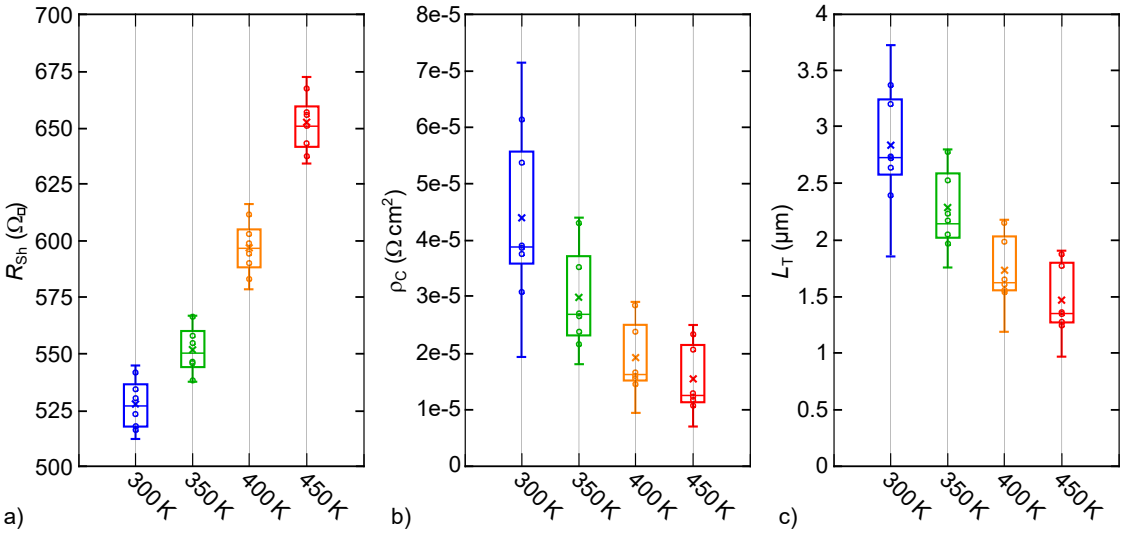

Figure 5.11: Summary of temperature dependent source contact properties. a) Sheet resistance, b) specific contact resistance and c) transfer length. Calculations are based on the formulas stated in the appendix A.5.

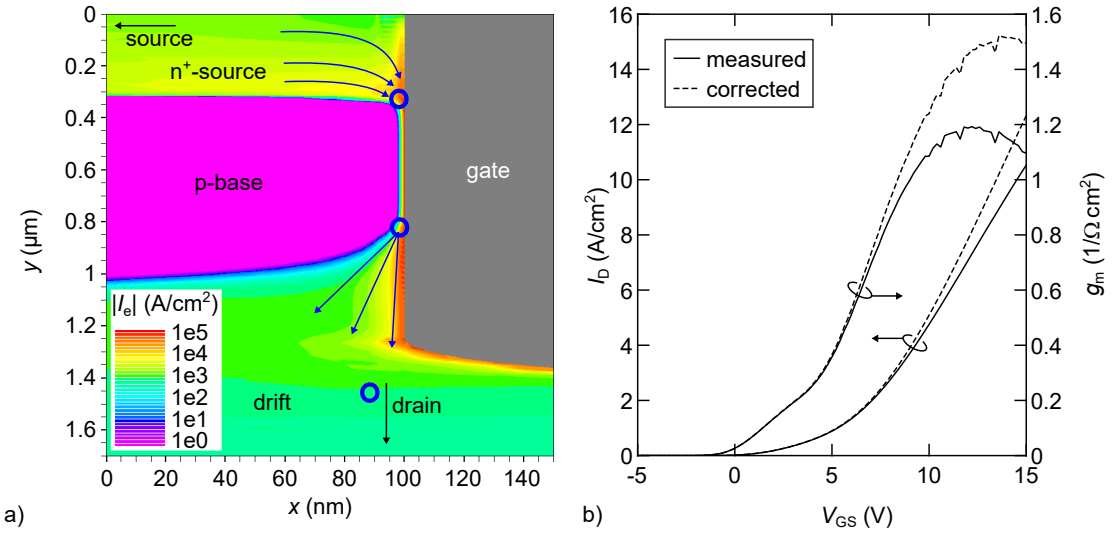

Figure 5.12: a) Contour plot of simulated electron current density in the channel region with the voltage probing sites indicated as blue circles. b) Exemplary trench MOSFET transfer characteristic and transconductance as measured and after correction for serial resistance.

Bulk and backside drain resistance: Instead of measuring drift layer, substrate and backside contact resistance separately, it is more accurate to determine all three components together, which will be denoted as R_{bulk}. This was done by measuring the resistance between a metal contact, located on the drift layer and the wafer backside contact. To mimic current spreading effects correctly, it is necessary to ensure that the

size of the metal pad is similar to the size of the actual trench MOSFET. In addition, the contact resistance $R_{\text{cont Drift}}$ of the said metal pad to the drift layer must be subtracted from the measured resistance. Due to a lower doping concentration of the drift layer, $R_{\text{cont Drift}}$ is bound to be higher than $R_{\text{cont S}}$. The specific drift layer contact resistance at room temperature, again obtained via TLM measurement, was found to be $\rho_{\text{cont Drict}} = (1.5 \cdot 10^{-4} \pm 4 \cdot 10^{-5})\,\Omega\,\text{cm}^2$. This is, as expected, considerably higher than for the n-source layer and equates to an absolute value of $R_{\text{cont Drift}} = (0.78 \pm 0.21)\,\Omega$ for the active device area. This results in a bulk resistance of $R_{\text{bulk}} = (4.8 \pm 0.2)\,\Omega$ for the trench MOSFET under consideration.

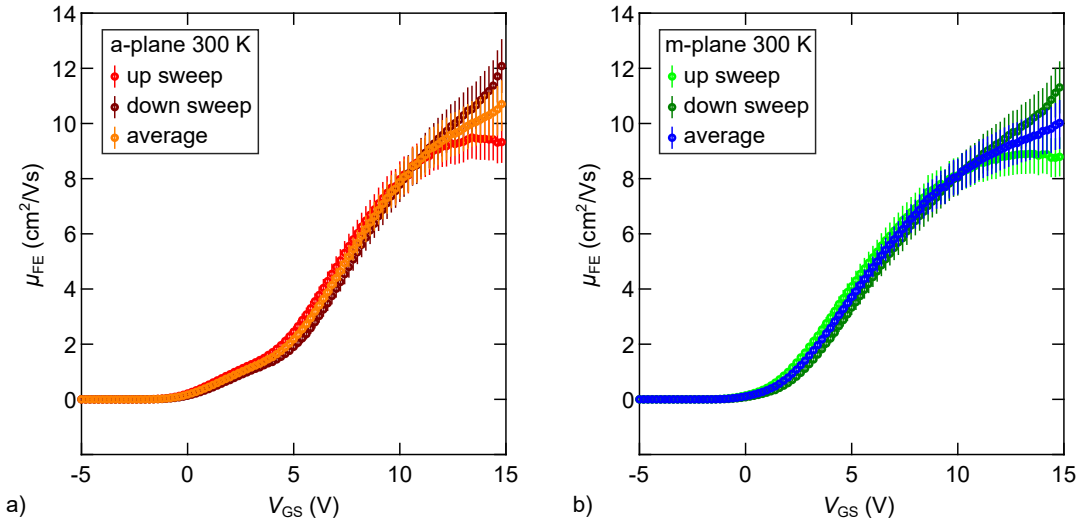

Figure 5.13: Gate bias dependent field effect mobility at room temperature for a- and m-plane oriented devices in a) and b), respectively. Values calculated from up and down sweep transfer curves were averaged.

Combining the various resistance components, the total serial resistance of the device adds up to $R_{\text{serial}} = (7.3 \pm 0.9)\,\Omega$. This equates to $\approx 15\,\%$ of the total device resistance and thus the measured drain current must be corrected in order to obtain a realistic value for the inversion channel carrier mobility. This however implies that R_{serial} is linear in V_{GS}. Such an assumption is reasonable since from all the presented resistance components, only R_{spread} might have a relevant dependence on the current density. Therefore, the impact on R_{serial} is small. The resulting effect due to channel current correction under the assumption of a linear R_{serial}, is displayed in figure 5.12 b). The field effect mobility was then calculated via equation (2.28) with the results displayed in figure 5.13 for two representative devices with a- and m-plane orientation in a) and b), respectively. Due to the hysteresis between up and down sweep, a different transconductance and thus a different mobility is obtained. This is best observed on a linear scale as displayed in the insets in figure 5.6. A likely explanation for the small, yet noticeable hysteresis is a change of interface charge density during the sweeping of the gate-source bias. An increasingly positive potential at the gate electrode leads to the incorporation of negative charges from the semiconductor into interface and near interface states. Furthermore, it shifts

the Fermi level upwards, which results in the ionization of acceptor like interface defects. These will also increase the negative interface charge density. The negative interface then hampers the formation of the inversion channel and reduces drain current. The result is an underestimation of carrier mobility due to an overestimation of carrier density. During the down sweep, trap discharging occurs, which is, at least in parts, significantly slower than the sweep rate [120]. This leads to a lower drain current compared to the up sweep, which causes the observed gap between up and down curve in figure 5.6. It also increases the slope of the transfer curve, i.e. the transconductance, and thus results in a higher field effect mobility. During the down sweep, channel mobility is overestimated. This can be seen in the plots in figure 5.13. To compensate both effects, the average of both mobility values was calculated. Its dependence on temperature is displayed in figure 5.14 a) for an m-plane oriented device with the peak mobility at $V_{GS} = 15\,V$ in b). A trend of decreasing mobility for increasing temperature is observed with the exception of the room temperature curve. This is in accordance with the transfer and transconductance curves displayed in figure 5.7.

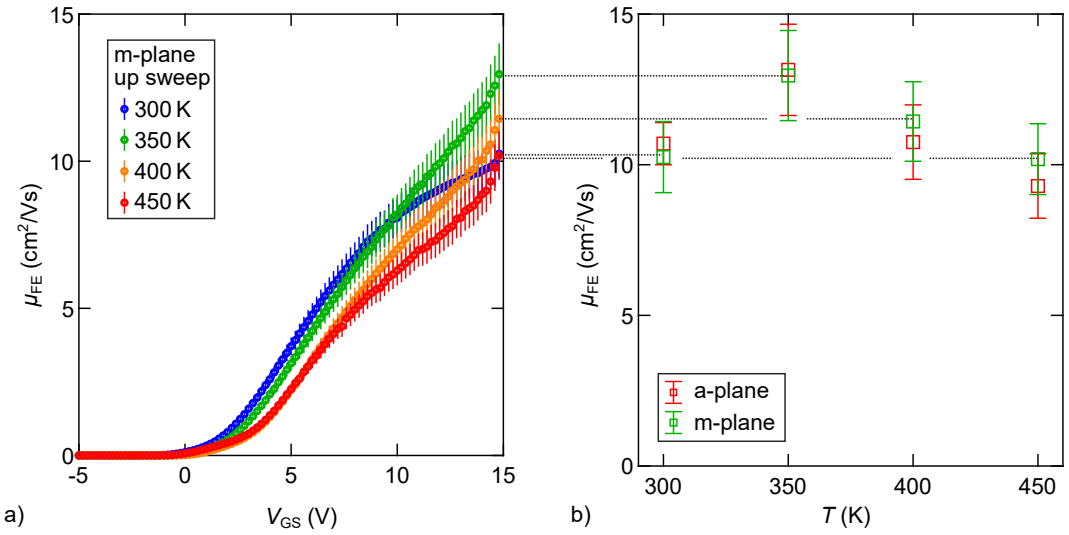

Figure 5.14: a) Gate bias dependent field effect mobility for a m-plane oriented device at different temperatures. The plot shows the average of up and down sweep values. b) Field effect mobility at $V_{GS} = 15\,V$ for a- and m-plane oriented devices at different temperatures. Again, the plot shows the average of up and down sweep values.

5.3.5 Area specific on-state resistance of trench MOSFETs

Another important device performance parameter is the area specific on-resistance $R_{DSon}\,A$. The calculation is relatively straight forward and was performed for channel resistance only as well as for the total device, the difference being the total serial resistance discussed in section 5.3.4. The results are presented in figure 5.15 a). Also displayed, are the hypothetical resistance values that were to be expected for a device with 3 µm pitch size. The values presented in a) correspond to the best performing devices, while the box plot in b) shows the channel resistance for a representative group of devices from the

wafer center region. The pitch reduction in b) corresponds to the average value of this group. The box plot shows that there is no significant difference between a- and m-plane oriented devices. If anything, the results show slightly more spreading in the case of m-plane devices, which can be attributed to a greater uncertainty for the corresponding trench geometry (cf. fig. 3.18 c)). The magenta markers indicate the on-resistance of the best performing m-plane device for $V_{GS} = 20\,V$, which is close to the point where gate leakage current becomes observable.

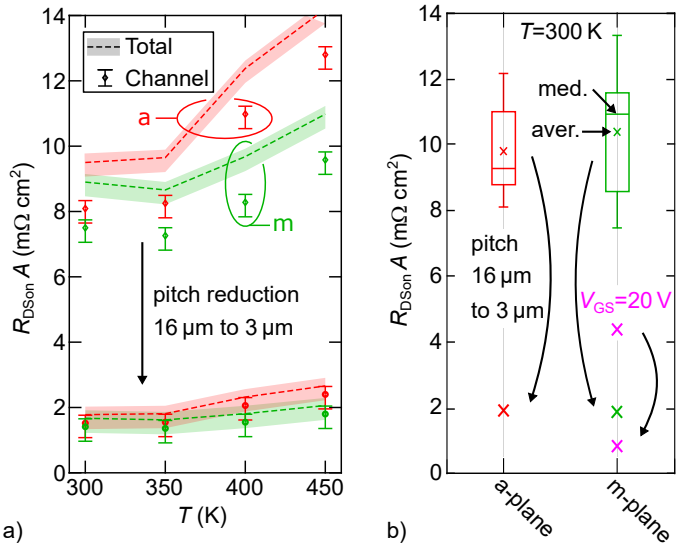

Figure 5.15: a) Area specific on-resistance for a- and m-plane oriented Trench MOSFETs, calculated for the channel only (data points) and for the total device (dashed line). The black arrow indicates the hypothetical values that were to be obtained if the cell pitch were reduced to 3 µm. b) Box plot for channel related $R_{DSon}A$ values of devices in the wafer center region, again the black arrows implicate a theoretical pitch reduction. The magenta data points represent the m-plane champion device for a gate-source bias of 20 V. All values were measured for $V_{GS} = 15\,V$ (except the champion device in magenta) and $V_{DS} = 0.1\,V$ for the active area $A = 1.92 \cdot 10^{-4}\,cm^2$. Reproduced from [119], with the permission of the American Vacuum Society.

5.3.6 Switching characteristic of trench MOSFETs

Although not considered in detail in this work, the switching performance of the trench MOSFETs was examined in a qualitative manner. Note that for an accurate characterization of the switching behavior, wafer-level measurements are not suitable because cables and chuck introduce stray capacitances and inductances. The on-resistance was measured for frequencies up to 100 kHz and the on- and off-switching time was extracted. To obtain these measures, the gate of the trench MOSFET was driven with a square wave signal V_{Gen} between -5 and 15 V and 50 % duty cycle. The MOSFET was connected in series with a 220 Ω resistance located between drain and a 1 V voltage supply. The voltage drop V_{MOSFET} across the transistor was measured and the transistor resistance calculated. The results are presented in figure 5.16.

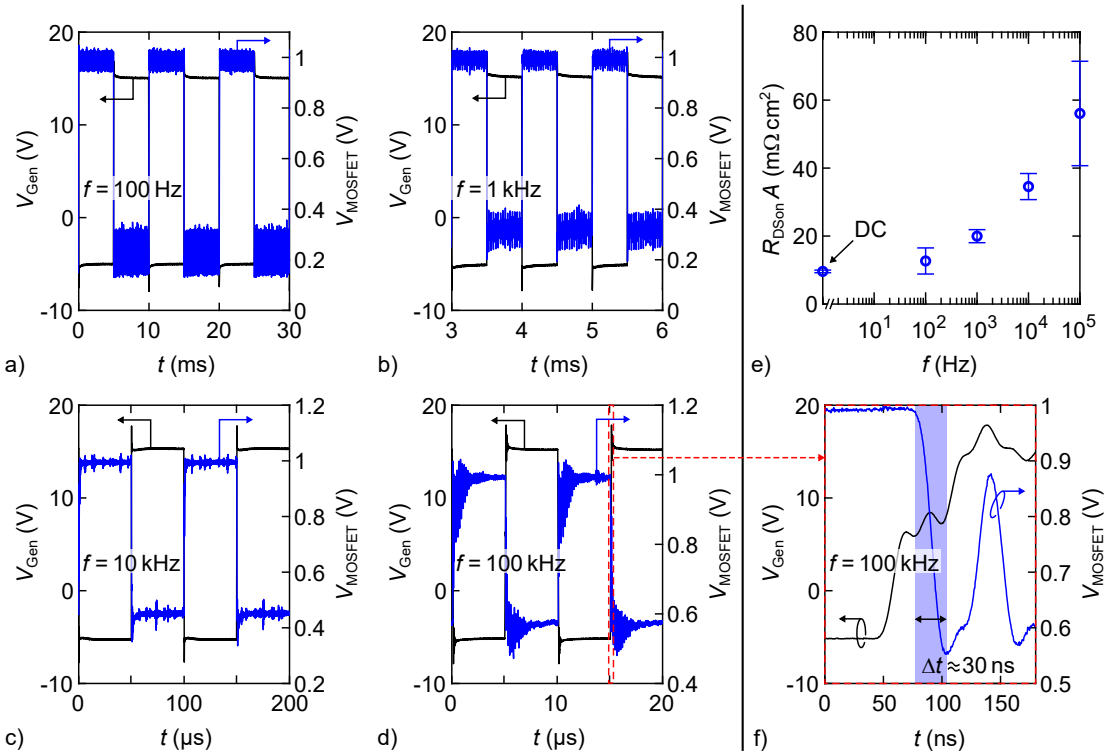

Figure 5.16: Signal of the function generator V_{Gen} (black) and voltage drop across an a-plane oriented MOSFET V_{MOSFET} (blue) for a signal frequency of 100 Hz a), 1 kHz b), 10 kHz c) and 100 kHz d). The calculated on-resistance, including the DC-resistance, at $V_{\mathrm{GS}} = 15\,\mathrm{V}$, is displayed in e). The plot in f) is a zoomed in image of the voltage flank during the switch on of the transistor.

The generator signal is monitored by a direct feed into an oscilloscope and appears reasonably clean, although, the closeup in figure 5.16 f) reveals a strongly distorted flank. The reason for this, is that the generator is operated at 200 % of its actual capability of 10 V peak to peak. To drive the GaN MOSFET, 20 V peak to peak are required. To achieve this, the output impedance was set to 50 Ω, which emulates, together with the internal impedance of 50 Ω, 25 Ω. The gate impedance of the MOSFET however, is much higher than 50 Ω, resulting in an actual output impedance of ≈ 50 Ω instead of 25 Ω and a practically doubled voltage output of the signal generator at the cost of signal quality. By using two independent power sources, the source contact of the MOSFET was set to -5 V which shifted the square wave signal to the above mentioned voltages between -5 and 15 V and achieved the required gate voltage to adequately drive the GaN MOSFET.

The on-wafer measurement set-up is not optimized for high frequency measurements and severe oscillations can be observed in the MOSFET signal. The oscillation at the signal plateaus originates from factors such as the measurement chuck, the probing needles and long coaxial cables. This effect seems to be reduced with increasing frequency. This is unusual behaviour and can probably be attributed to damping in the measurement set and the imperfect measurement conditions given by the setup. The second type of oscillation is only observable at high time resolution (fig. 5.16 d) and f)) and must be

attributed to the imperfections of the generator signal. Therefore a sound statement concerning the rise and fall time of the switching flank cannot be made. An estimation for the turn on and off time is $\approx 30\,\mathrm{ns}$. The same is true for the on-resistance, which was determined from the average voltage level during the on-state. The plot in figure 5.16 e) reveals, as expected, a rising on-resistance for increasing frequency.

The measurement demonstrates the switching capability of the fabricated devices in the kilohertz regime, which is the target range for inverter applications.

5.4 Electrical characterization of lateral MOSFETs

A similar set of characterizations was performed for the lateral MOSFETs. However, compared to their vertical counterparts, area specific quantities yield no useful information. Instead, drain source current is normalized to the gate width (cf. fig. 5.4 b)).

5.4.1 Transfer characteristic of lateral MOSFETs

In contrast to trench MOSFETs, a lateral MOSFET allows the variation of the gate length by lithography mask design, which is useful for the estimation of serial resistance. While the channel length of a trench MOSFET is limited by the thickness of the p-base layer, the length of a lateral channel can be $100\,\mu\mathrm{m}$ or more. The plot in figure 5.17 a) shows room temperature transfer curves at $V_{\mathrm{DS}} = 0.1\,\mathrm{V}$ for various channel lengths. The linear representation shows the expected decrease in drain current for increasing channel length L_{ch}. The threshold voltage is independent from L_{ch}. The plot in b) presents results of looped up- and down sweeps and a similar behavior as for the trench MOSFETs, described in section 5.3.1, is observed. Small hysteresis and only minor differences between loop two and three are found. The difference between the initial and subsequent loops suggests an interface that is comparable to that on the trench sidewall.

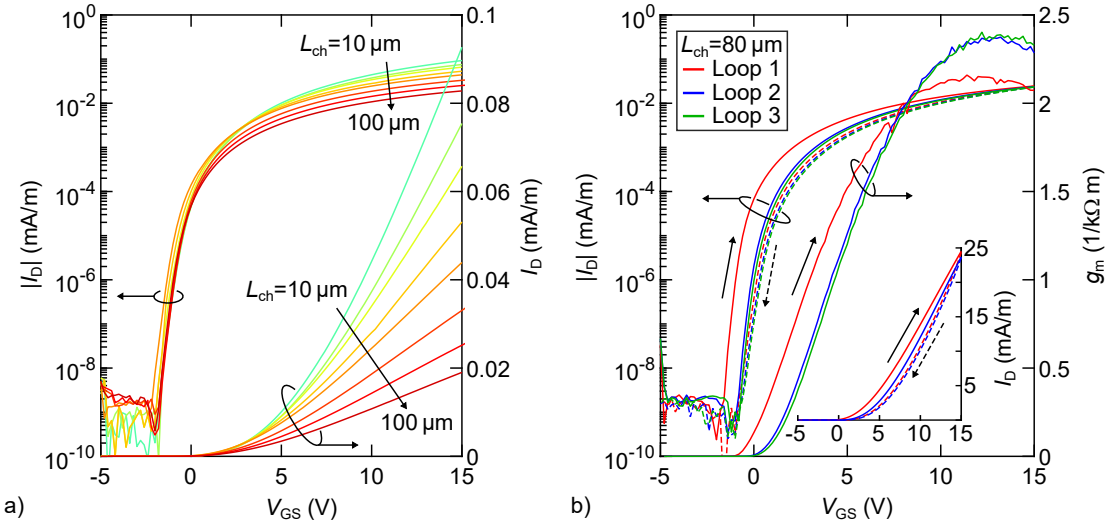

Figure 5.17: a) Room temperature transfer characteristic of lateral MOSFETs with different channel length L_{ch}. b) Room temperature transfer characteristic and transconductance of a lateral MOSFET with $L_{ch} = 80\,\mu m$. Three consecutive loops were measured with solid and dashed lines representing up- and down sweep, respectively. The inset shows loop one and two on a linear scale.

5.4.2 Serial resistance for lateral MOSFETs

Especially for devices with short channel length, a significant serial resistance is observed. The most obvious resistance component, apart from the channel itself, is again the source and drain contact resistance. Using the TLM related findings from section 5.3.4, its impact can be taken into account. In addition, the resistance at entry and exit of the inversion channel must be considered. The schematic in figure 5.18 a) illustrates the electron path from source to drain. The electrons must traverse several different regions. Once emitted by the source contact, they either enter a planar accumulation channel (1) followed by a vertical one (2), or travel through the n-source bulk material (3). The p-base layer can only be entered at the vertical inversion channel (4). The length of this channel depends on the over etch depth during the n-mesa process step, which is approximately 150 nm. Only at the end of this channel they can enter the planar inversion channel (5). The same sequence is then repeated in reverse at the drain side of the device. This results in a considerable serial resistance. Figure 5.18 b) shows the drain current as function of the channel length L_{ch} for different drain to source bias. Due to the mentioned serial resistance, the measured drain current deviates from the theoretically expected $1/L_{ch}$ dependence if the channel is not sufficiently long enough. Only for $L_{ch} \geq 50\,\mu m$, the serial resistance can be omitted.

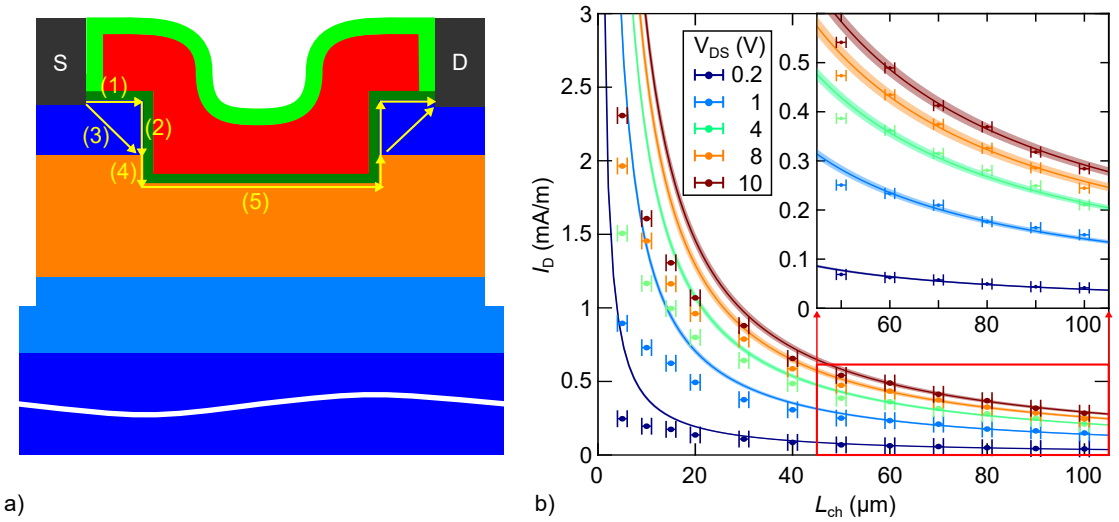

Figure 5.18: a) Schematic of the electron flow in a lateral MOSFET. The numbering refers to sections with different conduction mechanisms for the electrons. (1) conduction along a planar accumulation channel, (2) along a vertical accumulation channel, (3) through the n-source bulk material, (4) along a vertical inversion channel and (5) along a planar inversion channel. b) Drain current as function of L_{ch}. Solid lines represent the current without serial resistance, following a $1/L_{ch}$ relation. The error corridor corresponds to the uncertainty in L_{ch}. Measured values deviate significantly, depending on the channel length of the device. The inset is a zoom-in of the section with large L_{ch} where the serial resistance becomes negligible.

5.4.3 Inversion channel field effect mobility of lateral MOSFETs

In a similar manner as for the trench MOSFET in section 5.3.4, the field effect mobility was extracted for lateral MOSFETs with different orientation and various channel lengths. The room temperature peak mobility for different L_{ch} is displayed in the plot in figure 5.19 a). Again a significant difference was found between the values extracted from up- and down sweep transfer curves and as for the trench MOSFET, the average of both directions will be used. As expected, device orientation has no measurable impact. Due to the serial resistance, discussed in section 5.4.2, mobility drops noticeably for shorter L_{ch}. For devices with $L_{ch} \geq 50\,\mu m$ however, the mobility is constant as serial resistance becomes negligible. The same measurement was performed for different temperatures with the results displayed in figure 5.19 b). Again, there is no significant difference between devices with current flow long the a- or m-direction. Any deviations must be attributed to process- and measurement errors. A slight decrease of mobility with rising temperature is observed and is most likely due to a right shift of the transfer curve with increasing temperature, similar as observed for the trench MOSFET (cf. fig. 5.7). Interesting is the mobility difference for electrons in a planar inversion channel compared to electrons in a vertical one, with the former being a factor two to three higher. Even though the channel interface was subjected to TMAH treatment after the n-mesa plasma etching, surface quality is likely to remain in a somewhat degraded state. Although the experiment regarding plasma induced damage, described in section 4.3, suggested a

complete restoration of the GaN surface, this was only verified for leakage current and dielectric breakdown voltage. The impact on inversion channel carrier mobility cannot be assessed from a MOS capacitor. An impact despite TMAH treatment is likely the explanation for the carrier mobility to be lower than typically observed [43, 30]. Despite this fact, it outperforms the vertical channel, which suggests generally more favorable interface conditions compared to a trench sidewall.

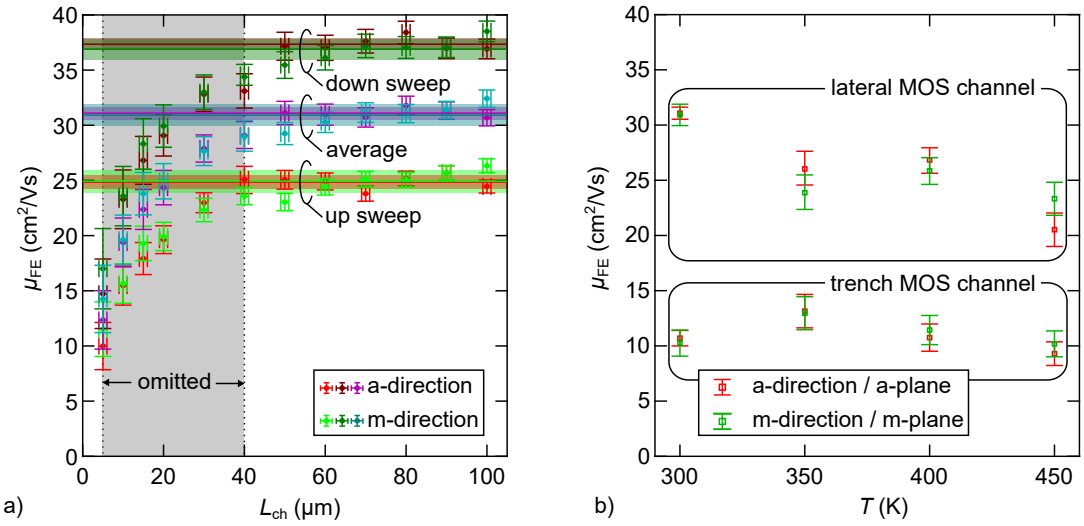

Figure 5.19: a) Peak field effect mobility of lateral MOSFETs with different channel lengths at 300 K. Red an green data points represent results from devices with current flow in a- and m-direction, respectively. Purple and blue are the corresponding average values for up- and down sweep measurements. Solid lines indicate the average for devices with $L_{ch} \geq 50\,\mu m$ with the shaded corridor referring to the standard deviation. Devices with $L_{ch} \leq 50\,\mu m$ were omitted due to large impact of serial resistance. b) Average mobility, as described in a), measured at different temperatures. Also displayed, are the results for the trench MOSFET (cf. fig. 5.14).

5.5 Field effect mobility for planar and vertical MOS inversion channels in the context of published results

The lateral MOSFET, as fabricated in this work, cannot be used as power switch due to the absence of a drift region and its planar nature. However, its channel is essentially the same as for a VD-MOSFET, which must be regarded as competitor to the trench MOSFET. Note that the channel for a VD-MOSFET in the common sense, is typically fabricated on a pristine surface and not on an etched one as is the case here. The obtained results are thus a conservative estimation of the channel performance as can be seen from the comparison with literature values presented in table 5.3. Although a holistic discussion of advantages and disadvantages, regarding the competitiveness of both devices, is beyond the scope of this work, a brief and qualitative comparison will be presented. The essential benefits of both devices, compared to each other, are listed in table 5.2.

Table 5.2: Benefits of VD- and trench MOSFET compared to each other.

VD-MOSFET	Trench MOSFET
superior inversion channel carrier mobility	smaller pitch size
cheaper fabrication due to the absence of a trench structure	better current spreading, no aperture effect
gate dielectric is less prone to failure due to the absence of a trench structure	

Note that this is not an absolute rating and the relevance of the various statements strongly depends on device application and fabrication. The trench MOSFET design has its justification and proved its value for silicon based power switches. The adoption took many years [75] but was eventually successful. A similar scenario is possible for the GaN trench MOSFET but will strongly depend on growing material understanding and the advances in fabrication technology emerging thereof. Table 5.3 lists a selection of published results concerning the inversion channel field effect mobility. This shows that a high carrier mobility is possible in vertical MOS channels and that the trench MOSFET is indeed a viable option.

Table 5.3: MOS inversion channel carrier field effect mobility for several published devices.

Device type	μ_{FE} (cm^2/Vs)	Gate dielectric	Comment	Ref.
Planar interface				
VD-MOSFET	7.1	ALD Al_2O_3	Ion implanted device, channel on unetched surface	[42]
LD-MOSFET	31	LPCVD SiO_2	Epitaxy only, channel on etched surface	This work
LD-MOSFET	28-36	ALD AlSiO	Ion implanted device, channel on unetched surface	[141]
Vertical interface				
Trench MOSFET	6.3	ALD Al_2O_3	fully vertical device	[142]
Trench MOSFET	10	ALD Al_2O_3	fully vertical device	[50]
Trench MOSFET	11	LPCVD SiO_2	fully vertical device	This work
Trench MOSFET	17.8	ALD SiO_2	quasi vertical device (GaN on Si)	[28]
Trench OG-FET	30	ALD Al_2O_3	fully vertical device with overgrown channel	[48]
Trench MOSFET	41	ALD SiO_2	quasi vertical device (GaN on Si)	[52]

The results of this work suggest, that the carrier mobility in a vertical MOS channel is generally lower than in a planar one. For the vertically oriented channel, the measured mobility was below the top values reported in literature [52]. To improve the mobility, the following three aspects must be considered and corresponding process steps need to be optimized in future experiments.

- The GaN surface quality after the wet etching: This concerns roughness, dangling bonds, impurity incorporation, contamination, as well as surface- and near surface states, in general.
- The GaN to dielectric interface during and after the deposition procedure: Process temperature, atmosphere composition and pressure are the key influence factors.
- The Interface improvement during annealing and post deposition treatments: Similar to the very effective nitric oxide anneal for SiC devices [130–132], a procedure for GaN might increase the channel mobility substantially.

Considering the metal-free processing and the intensive wet etching post treatment, negative impact due to impurity incorporation and contamination, at least for the vertical MOS interface, is deemed relatively low. Especially for the planar devices, but for the trench MOSFETs as well, surface roughness must be considered as a potential culprit. Its effect might be evaluated by fabricating lateral MOSFETs on a pristine c^+-surface, with the same deposition and annealing procedure as used for the devices in this work. A second effect that could have a negative impact on channel mobility, is the high process temperature during the deposition of the gate dielectric. Disintegration of the GaN surface at elevated temperature [143] with loss of nitrogen and the formation of a Ga-rich cap layer [140] is likely to have an adverse effect on carrier mobility due to increased coulomb scattering and carrier trapping. The high mobility values demonstrated by Khadar et al. [52] and Tanaka et al. [43] were achieved by using ALD SiO_2 at 300 °C and Tetraethyl orthosilicate SiO_2 at 350 °C, respectively. The significantly lower temperatures support the assumption that the 880 °C LPCVD SiO_2, although beneficial in terms of layer quality, might be harmful to the interface quality. The post deposition annealing showed promising effects concerning IV-hysteresis (cf. sec. 4.1.2) and a beneficial impact towards channel mobility, due to a reduction of interface defect density is likely. However, to what extend the interface is degraded during etching and deposition procedures, and how effective post deposition annealing is, needs to be determined by further experiments.

6 TCAD simulation of vertical MOS inversion channel carrier mobility

This chapter treats modeling and calibration of dopant ionization and carrier mobility as well as simulations of shielding structures. The calibration part was carried out in a way to support electrical measurements performed on devices fabricated in this work. The objective is to put the measured field effect mobility in context with the simulated inversion channel carrier mobility. The first part of the chapter describes the calibration of dopant ionization and carrier bulk mobility models with literature data. The results are then used as foundation in the second part, which is concerned with inversion carrier mobility. Using the multi component mobility model introduced in section 2.4.4, inversion carrier mobility is simulated and validated by fitting the outcome to real device transfer characteristics. For adequate comparison, all currents were normalized to the inversion channel width, i.e. A/cm. Interface defect and charge density were taken into account as well. The rest of the chapter is concerned with the simulation of shielding structures. Since implantation based p-type doping, necessary for effective shielding, was not included in the experimental part of this work, it was examined by means of TCAD simulation. Two different shielding structures are evaluated and compared in terms of shielding effectiveness and impact on the on-resistance. This final part of the chapter is based on information that was published in [144].

6.1 Calibration of doping ionization and carrier bulk mobility

This section describes the calibration of the impurity ionization model as well as the carrier bulk mobility and its dependence on said impurity concentration. Experimental data was used from literature [53, 90, 91, 93].

6.1.1 Calibration of doping ionization

Using equation (2.10) in combination with the relation for dopant depending ionization energy (2.9) and the assumption regarding impurity activation (2.6), the carrier concentration for p- and n-type doping can be fitted with five to eight parameters, depending on whether or not compensation is taken into account. The results for both cases are plotted as dashed and solid lines in figure 6.1 for holes a) and electrons b). The related parameter set is presented in table 6.1. Without compensation, the concentration of

the unintended species, i.e. compensating donors N_D in the case of p-type doping and acceptors N_A in the case of n-type doping, were assumed to be zero in equation (2.10). The respective fitting results are displayed as dashed lines in the plots in figure 6.1. A generally good agreement is achieved for electrons at moderate to high temperatures, if doping concentration is in the range of $10^{17}\,\mathrm{cm}^{-3}$. For low doping, the relative share of compensation centers is higher and their effect more pronounced. Omitting them leads to an overestimation of carrier concentration. This is also true for low temperature, where dopant freeze out occurs. Note that deviation is most prominent for low doping at low temperature, where both effects coincide. A similar scenario is observed for the hole concentration in p-type GaN. However, deviation is stronger and apparent at room temperature. To achieve a more accurate fit, compensation must be taken into account. Assuming a complementary impurity species of certain concentration allows the modeling of a steeper drop of carrier concentration for low temperature where compensation centers become relevant, as the actual dopants begin to freeze out. Due to the higher ionization energy of magnesium compared to silicon, the effect is more pronounced for holes, leading to a more pronounced freeze out effect in p-type GaN. The fitting results with compensation are displayed as solid lines in the plots in figure 6.1. For electrons, a significant improvement is achieved at low temperatures and low doping concentration is fitted more accurately as well. The fit on hole concentration is also improved, but a certain deviation is still apparent for the low doping concentration of $1.2 \cdot 10^{17}\,\mathrm{cm}^{-3}$. A higher relative amount of compensation centers in combination with a higher ionization energy for low doping concentration (cf. eq. (2.9)) prevents accurate fitting in this regime while maintaining consistency with data from higher doped samples.

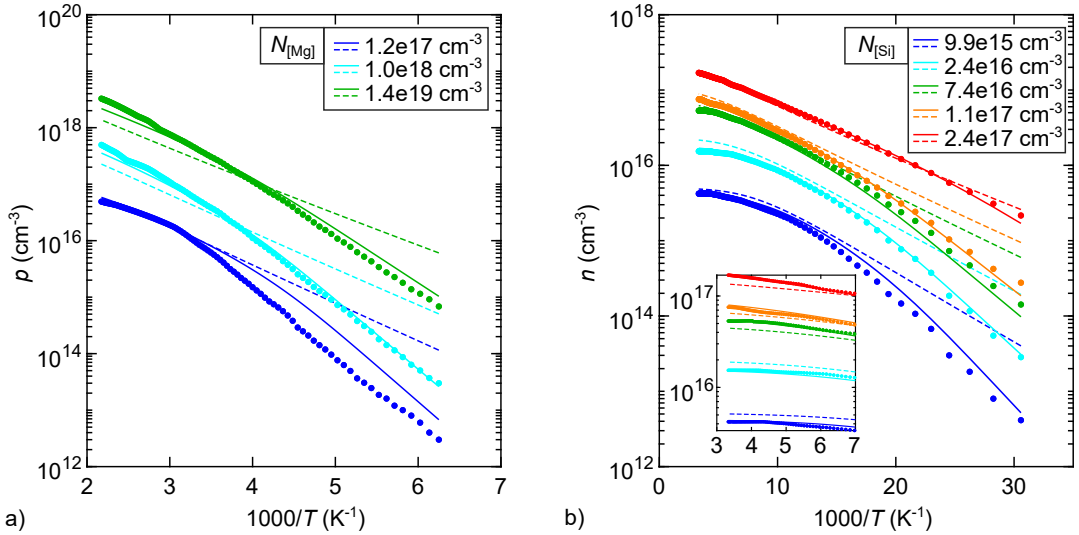

Figure 6.1: Arrhenius plot of the carrier density for various doping concentrations. Dots represent literature data from [93] for holes in a) and from [91] for electrons in b). Solid and dashed lines are the fitting results with and without compensation taken into account.

Summarizing the fitting procedure, it can be stated that the model achieves a generally good match for n-type material and is in good agreement for p-type material in the regime relevant for this work, which is room temperature and above, as well as impurity concentration in the range of $10^{18}\,\mathrm{cm}^{-3}$ and above.

Table 6.1: Fitting parameters for the calibration of dopant ionization.

	A_{EA} (eV)	B_{EA} (eV cm)	F_{A}	$N_{\mathrm{A_0}}$ (cm^{-3})	β_{A}	F_{Dcomp}	$N_{\mathrm{Dcomp_0}}$ (cm^{-3})	β_{Dcom}
p-type (w/o compensation)	0.25	3.55e-8	1	74e22	2.28	-	-	-
p-type (with compensation)	0.25	2.27e-8	1	4e22	2.52	0.04	13e21	0.1
	A_{ED} (eV)	B_{ED} (eV cm)	F_{D}	$N_{\mathrm{D_0}}$ (cm^{-3})	β_{D}	F_{Acomp}	$N_{\mathrm{Acomp_0}}$ (cm^{-3})	β_{Dcomp}
n-type (w/o compensation)	0.05	6.83e-8	0.65	62e19	4.24	-	-	-
n-type (with compensation)	0.03	2.50e-8	0.96	10^{19}	0.88	0.13	17e16	2.96

6.1.2 Calibration of carrier bulk mobility

Based on the fitted relation between impurity concentration and carrier density, and using equation (2.11), the bulk mobility was fitted to data from [90] for holes and [53] for electrons. This means equation (2.10) was inserted as $N_{\mathrm{A,D}}^{-;+}$ in the bulk mobility formula (2.11). The ionization parameters, that were determined before, were set to the values listed in table 6.1 with constraints that allow a 5 % change in either direction during the fitting procedure. This increases flexibility of the model but keeps the result consistent with the outcome obtained from the ionization fit. Compensation was included in the bulk mobility fitting.

The fitting results, corresponding to the parameter sets listed in table 6.2, are displayed as Arrhenius plot in figure 6.2 a) for holes and b) for electrons. In both cases, the model fails for high doping concentrations. The reason for this is most likely an overestimated concentration of free carriers, which in turn (cf. eq. (2.11)) leads to an underestimation of the bulk mobility. Due to a scarcity of data, the calibration for the impurity ionization was limited to $1.4 \cdot 10^{19}\,\mathrm{cm}^{-3}$ for magnesium and $2.4 \cdot 10^{17}\,\mathrm{cm}^{-3}$ for electrons. Narita et al. [91] and Kozodoy et al. [90], along with other groups [145–148], reported a decrease in hole density for impurity concentrations above $N_{[\mathrm{Mg}]} = 10^{20}\,\mathrm{cm}^{-3}$. According to Kozodoy et al. [90], the main reasons for this are a reduced degree of impurity incorporation along with a change in morphology and the generation of crystal defects. The latter leads to more compensation centers, which then lower free carrier concentration. A similar scenario is very likely in the case of n-type doping. The n-type model is focused on generally lower impurity concentrations, which explains the earlier onset of inconsistency

at impurity concentrations of $N_{[Si]} \approx 1e19\,cm^{-3}$ compared to $N_{[Mg]} \approx 1e20\,cm^{-3}$. These observations match the model inconsistency observed during the fitting. Considering data lower than the stated concentration limits, agreement for the bulk mobility is reasonably good at 400 K and below.

A significant discrepancy is apparent for electron mobility at elevated temperatures. Carrier mobility is underestimated for low doping concentration while it is overestimated for high doping concentration. At the same time, the model fits perfectly for all concentrations at room temperature ($2 \cdot 10^{19}\,cm^{-3}$ excluded). This circumstance is interesting in the way, that rather good agreement for the actual carrier concentration was achieved at elevated temperature and discrepancy was observed at lower temperature. This indicates that the used mobility model lacks the ability to adequately represent the high temperature regime. At the same time, consistency of the literature data is not flawless and partially prevents a matching simulation.

The conclusion of the fitting session is that good agreement is achieved for temperatures of 400 K and below, if the impurity concentration is less than $10^{18}\,cm^{-3}$ for silicon and less than $10^{20}\,cm^{-3}$ for magnesium. Device regions, where carrier mobility is relevant, are the p-base and drift layer, where impurity concentrations are well within the mentioned regime. Further simulation procedures concern the inversion channel carrier mobility, which will be based on the electron bulk mobility for material with an impurity concentration of $N_{[Mg]} \approx 1e18\,cm^{-3}$. Note that the inversion channel is a special case in the way that, apart from interface related mobility components, electrons move in p-type material. The assumption that is made for this simulation is that, concerning their effect on bulk mobility, magnesium and silicon impurities are treated equally. This means that the electron bulk mobility in the p-base layer is modeled, as illustrated in figure 6.2 b), based on the impurity concentration that is present in the p-base layer.

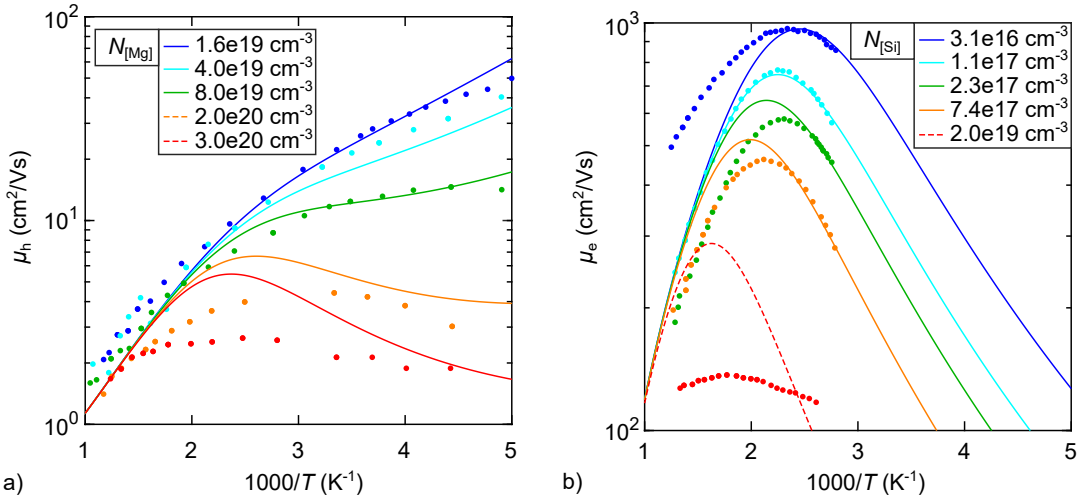

Figure 6.2: Bulk mobility fit based on equation (2.11) to data from [90] for holes in a) and to data from [53] for electrons in b). Note that the 2.0e19 cm^{-3} sample in b) was excluded from the fit and the dashed fit line is based on the parameter set obtained from a fit to the other concentrations.

Table 6.2: Fitting parameters for the calibration of the carrier bulk mobility and the adjusted parameters for dopant ionization.

	α	exp1	exp2	exp3	exp4	μ_{min} ($\mathrm{cm^2/Vs}$)	$\mu_{\mathrm{bp1,2}}$ ($\mathrm{cm^2/Vs}$)	$\mathrm{N_{ref}}$ ($\mathrm{cm^{-3}}$)
p-type	0.05	-3.43	-0.42	-9.31	1	0	28.47, 1.12	7.2e17
	A_{EA} (eV)	B_{EA} (eV cm)	F_{A}	$N_{\mathrm{A_0}}$ ($\mathrm{cm^{-3}}$)	β_{A}	F_{Dcomp}	$N_{\mathrm{Dcomp_0}}$ ($\mathrm{cm^{-3}}$)	β_{Acomp}
p-type	0.24	2.25e-8	1	3.7e22	2.41	0.04	1.2e22	0.1
	α	exp1	exp2	exp3	exp4	μ_{min} ($\mathrm{cm^2/Vs}$)	$\mu_{\mathrm{bp1,2}}$ ($\mathrm{cm^2/Vs}$)	$\mathrm{N_{ref}}$ ($\mathrm{cm^{-3}}$)
n-type	0.77	-2.98	-2.84	-6.48	0.51	0	2000, 2000	8.47e14
	A_{ED} (eV)	B_{ED} (eV cm)	F_{D}	$N_{\mathrm{D_0}}$ ($\mathrm{cm^{-3}}$)	β_{D}	F_{Acomp}	$N_{\mathrm{Acomp_0}}$ ($\mathrm{cm^{-3}}$)	β_{Acomp}
n-type	0.04	2.25e-8	0.97	1e19	0.9	0.13	1.7e17	3.02

6.2 Modeling of inversion channel carrier mobility

In addition to the field effect mobility, calculated in section 5.3.4, the inversion channel mobility was modeled using Silvaco TCAD software. The simulation was based on the setup described in the appendix A.7 and relied on the bulk mobility calibrated in section 6.1.2. The mobility model used for the simulation originates from the work of Uhnevionak et al. [96] and was introduced in section 2.4.4. The goal of the modeling procedure was the calibration of the inversion channel mobility model, as well as the MOS interface defect and charge density. To achieve this, transfer curves were simulated and fitted to measurement data of trench MOSFETs for different temperatures. Regarding the mobility model, one parameter set was used for all curves but defect density and interface charge density was adjusted for different temperatures. As can be seen from the plot in figure 6.4 b), coulomb scattering dominates the carrier mobility. According to findings of other groups [137, 108, 149, 150] , surface phonon scattering and surface roughness related mobility terms are comparably high at WBG MOS interfaces and their impact on the total carrier mobility is only weak. Bulk mobility was used as calibrated for a concentration of $10^{17}\,\mathrm{cm^{-3}}$ ionized acceptors in the p-base layer. This value was provided by the supplier of the epitaxial layer and results in a mobility in the range of hundreds of $\mathrm{cm^2/Vs}$. Its contribution to the final outcome is therefore only marginal.

The surface phonon mobility is modeled by

$$\mu_{\mathrm{sp}} = \left[\frac{SP_1}{E_\perp} + \frac{SP_2 \left(\frac{N_{\mathrm{A}}^-}{SP_3} \right)^\beta}{E_\perp^{1/3} \left(\frac{T}{300} \right)^\kappa} \right] \exp\left[\frac{D}{L_{\mathrm{crit}}} \right] \tag{6.1}$$

with fit parameters SP_{1-3}, β and κ. The lattice temperature is denoted by T, N_{A}^{-} is the density of ionized acceptors in the bulk material near the channel and $E_{\perp}$ is the electric field perpendicular to the flow direction of the carriers in said channel. The whole term goes to infinity for increasing distance D to the interface with the characteristic decay length $L_{\mathrm{crit}} = 10\,\mathrm{nm}$. This ensures that surface phonon related effects become irrelevant in the bulk material.

The surface roughness mobility is calculated as

$$\mu_{\mathrm{sr}} = \left[\frac{E_{\perp}^{2}}{\delta} + \frac{E_{\perp}^{3}}{\eta}\right]^{-1} \exp\left[\frac{D}{L_{\mathrm{crit}}}\right] \tag{6.2}$$

with fit parameters δ and η. Both terms 6.1 and 6.2 are adopted from [96].

The predominant factor is the coulomb scattering term. The voltage dependence of coulomb scattering related carrier mobility resembles the voltage dependence of the field effect mobility, which is increasing with rising gate bias. A similar dependence was found by Perez et al. for SiC [108, 149] and GaN [137]. The coulomb scattering term is modeled by three components combined via Matthiessen's rule. The components differ in their definition of CHG and read

$$\mu_{\mathrm{c}} = \frac{N_{\mathrm{Mob}}\left(\frac{T}{300}\right)^{N_{\mathrm{T}}}\left(1 + \left[\frac{n}{N_1\ CHG^{N_2}}\right]^{N_3}\right)}{CHG^{N_4}\exp\left(\frac{-D}{L_{\mathrm{crit}}}\right)\left[1 - \exp\left(-\left(\frac{E_{\perp}}{N_5}\right)^{N_6}\right)\right]} \tag{6.3}$$

with fit parameters $N_{\mathrm{Mob}}, N_{\mathrm{T}}$ and N_{1-6}. The inversion channel carrier density is denoted by n.

The distinctive CHG is given as

$$CHG_1 = \frac{N_{\mathrm{A}}^{+}}{NTD}, \quad CHG_2 = \frac{Q_{\mathrm{it}}^{+} + \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} D_{\mathrm{Don}}\,\mathrm{d}E}{NTT}, \quad CHG_3 = \frac{Q_{\mathrm{it}}^{-} + \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} D_{\mathrm{Acc}}\,\mathrm{d}E}{NTT} \tag{6.4}$$

with the p-base layer ionized acceptor concentration N_{A}^{+}, positive and negative interface charge density $Q_{\mathrm{it}}^{+,-}$ and acceptor and donor like defect density D_{Acc} and D_{Don} integrated from valence band edge to conduction band edge. NTD and NTT are fitting parameters. Note that while D_{Acc} and D_{Don} can both be present, positive and negative interface charge is exclusive. For the devices examined in this work, the interface characteristic is positive and Q_{it}^{-} is set to zero.

The simulation results were fitted to the transfer curves measured for an m-plane oriented device and are presented for $T = 300\,\mathrm{K}$ and $400\,\mathrm{K}$ in figure 6.3 a) and b). The plots feature up- and down sweep results on linear as well as logarithmic scale. This

allows a better judgment for the fitting quality. As can be seen from the 300 K fit in a), agreement is good both for low and high gate-source bias. Note that no leakage current was implemented in the simulation, which is the reason for the deviation below $V_{GS} = 2\,V$. The implemented interface defect and charge density, and the corresponding channel mobility with its various components, is displayed in figure 6.4. As discussed on a theoretical basis in section 2.6.3, the simulation yields a decreasing amount of ionized donors for increasing V_{GS}. To achieve good agreement between measurement and simulation, donor concentration had to be increased for higher temperature. The same is true for the density of acceptor like interface defect states. To achieve a general right shift, the positive interface charge density was continuously reduced for increasing temperature.

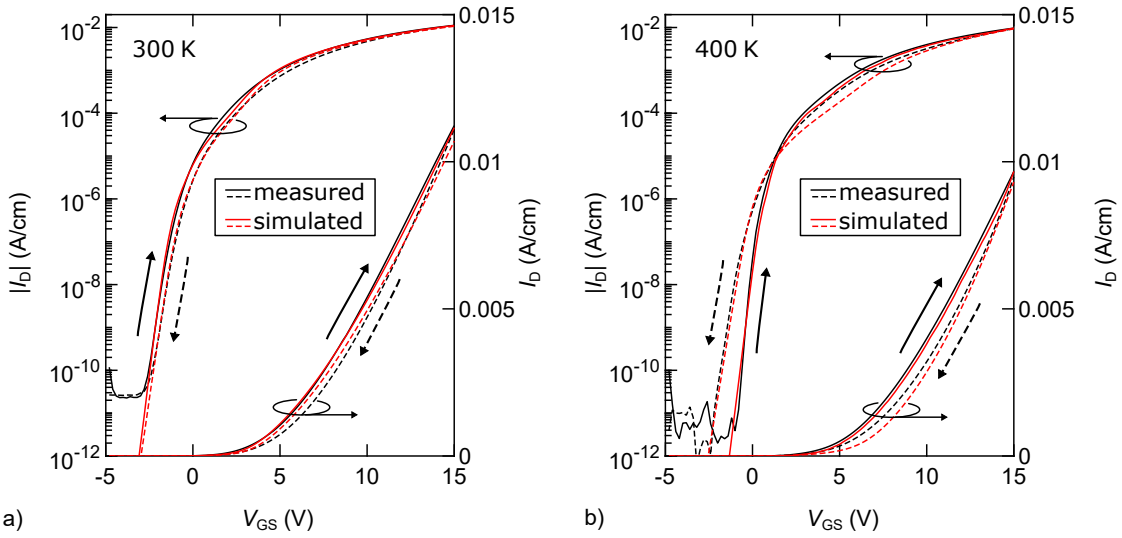

Figure 6.3: Measured and simulated transfer curves of a trench MOSFET in linear and logarithmic representation at 300 K a) and 400 K b). Solid and dashed lines represent up- and down sweep, respectively.

The simulation outcome for the total channel mobility was $\mu_{inv} \approx 4\,cm^2/Vs$, which is considerably lower than the field effect mobility calculated in section 5.3.4 but coincides with findings from Perez et al. [137] for GaN and is similar to the channel mobility of SiC inversion channels with high defect density [149]. Although the dependence is weak, the simulation yields decreasing channel mobility for increasing temperature. This is in agreement with the measurement results from section 5.3, but contradicts literature findings [137, 151]. The expected temperature dependence is found for $V_{GS} < 5\,V$ but is negated for higher gate bias as the effect of defects increases. The decrease of mobility originates from the higher defect density that was implemented for elevated temperatures. Although the simulation result deviates from the outcome of the electrical measurements, there is agreement regarding a high defect density at the MOS interface and an adverse effect on carrier mobility resulting thereof. Thoughts and suggestions concerning future work are provided in section 7.2.

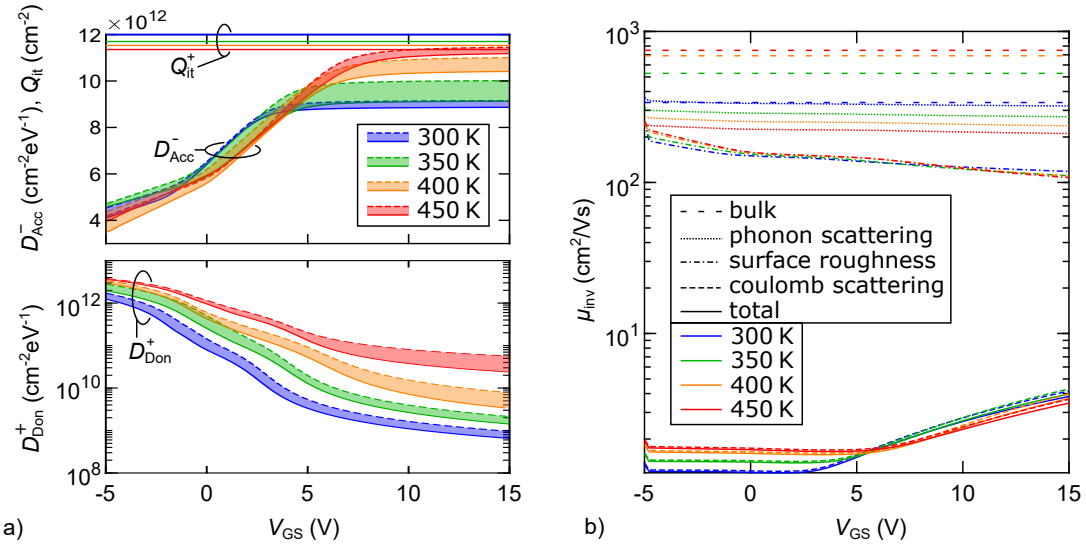

Figure 6.4: a) Modeled interface charge density together with ionized acceptor and donor like defect states as function of gate bias for different temperatures. b) Different components of the simulated inversion channel carrier density at the interface as function of the gate bias for different temperatures.

6.3 Simulation of shielding structures

This section contains simulations of different shielding structures but is restricted to shielding of the gate trench and the gate dielectric in the trench bottom in particular. Additional shielding is required at the chip border, were symmetry is broken. The shielding structures at the chip border are referred to as edge terminations and multiple different types exist. The basic principle however, is the same as for the shielding of the gate trench to which this section is limited. For information on edge terminations, it is referred to standard literature like [8, 76, 84]. To make the impact from the shielding structures more pronounced and thus better observable, the MOS channel carrier mobility was increased to $50\,\mathrm{cm}^2/\mathrm{Vs}$ for these simulations.

While chapter 4 was concerned with the dielectric field strength during on-state, this section simulates the off-state field strength in the dielectric and the semiconductor. Parameters and geometrical dimensions that were used for this simulation are stated in table 6.3

The dielectric field strength limit of approximately 3 to $4\,\mathrm{MeV/cm}$, identified as the end of the low field regime in chapter 4, must hold during the off-state as well. Typical potential differences between drain and gate during off-state range from hundreds of volts to kilovolts. Even though, most of this voltage drops across the depletion region of the drift layer, during the expansion of this depletion region, a high field strength builds up in the gate dielectric as well. This built-up can be suppressed by the introduction of a shielding structure. The plot in figure 6.5 b) shows the simulated maximum field

Table 6.3: Parameters for the simulation of shielding structures. *Parameters cannot be stated exactly since the p-region was implemented via an implantation simulation. Details can be found elsewhere [144].

Parameter	Value	Parameter	Value
Trench width	1.1 µm	Thickness source layer	300 nm
Trench depth	1.7 µm	Doping source layer	1e19 e^-/cm^3
Trench corner radius	200 nm	Thickness p-base layer	700 nm
Gate dielectric thickness	50 nm	Doping p-base layer	1e17 e^-/cm^3
Field plate width	1.55 µm	Thickness drift layer	15 µm
Field plate depth	3 µm	Doping drift layer	1e16 e^-/cm^3
Field plate corner radius	500 nm	Thickness spreading layer	300 nm
Field plate dielectric thickness	500 nm	Doping spreading layer	5e16 e^-/cm^3
Distance field plate to trench	900 nm	Doping p-shielding*	0.1-1e18 e^-/cm^3
p-implant region width*	1.6 µm		
p-implant region depth*	3 µm		
Distance p-implant region to trench*	900 nm		

strength in the gate dielectric for the structures depicted in a). If a shielding structure is present, the electric field is either deviated towards the field plate (type B) or reduced by a faster expansion of the depletion region due to the deeper and higher doped p-shielding region (type C). While the unshielded device would experience a dielectric field strength of more than 9 MV/cm at V_{DS} = 1200 V, proper shielding can reduce the exposure to below 4 MV/cm.

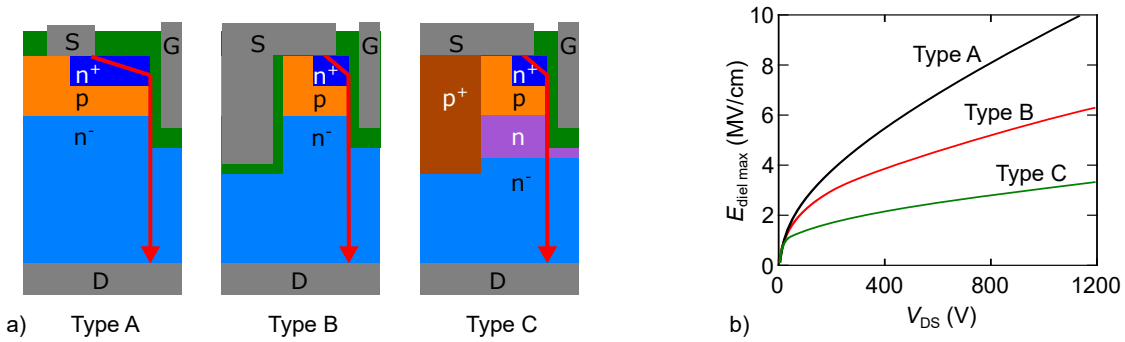

Figure 6.5: a) Schematics of a trench MOSFET half cell as reference without shielding type A, with field plate shielding type B and with shielding via p-type region type C, where an optional spreading layer with higher n-doping is added as well. The plot in b) shows the simulated maximum field strength in the gate dielectric for increasing V_{DS}.

A more in-depth examination of the field distribution is presented in figure 6.6 a) for V_{DS} = 1200 V and reveals the expected field peaks at the corners of the gate trench and field plate. While shielding results in a drastic reduction of these peaks and reduces the field strength overall, the inclusion of the above mentioned spreading layer impedes this effect. The reason is a slower expansion of the space charge region due to the higher carrier

concentration. However, the advantage of such an additional layer becomes apparent from the plot in figure 6.6 b) where the structure C_1 with spreading layer, features a lower on-resistance than structure C_2 without such a layer. This difference originates from the spreading resistance R_{spread} discussed in section 5.3.4 This creates a trade-off situation where geometry and doping concentration are the crucial parameters for optimization. Yet another aspect that must be taken into account for shielding structures is the increase of the cell pitch, which can have a severe effect on the on-state performance.

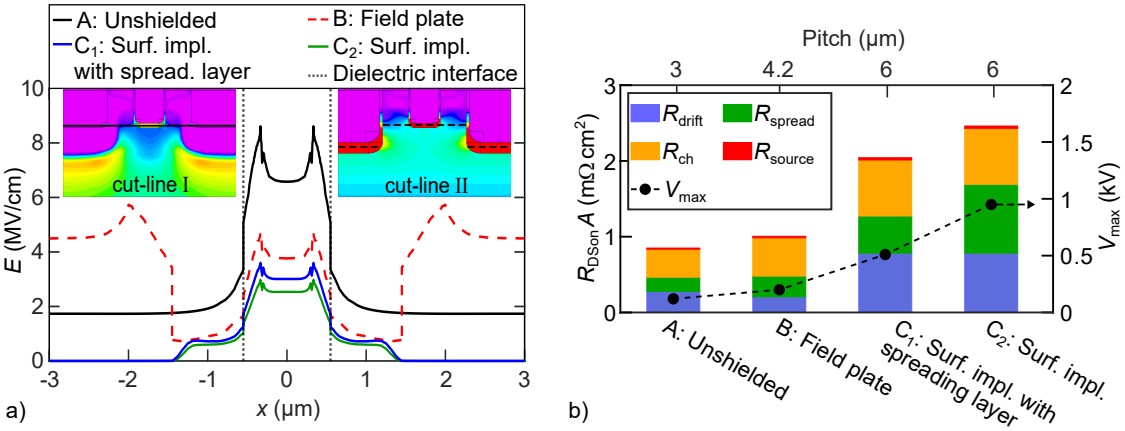

Figure 6.6: a) Electric field strength in the semiconductor and gate dielectric for $V_{\text{DS}} = 1200\,\text{V}$. The graph shows the field strength along the cut-line I for structures A and C and cut-line II for structure B. b) Corresponding resistance components (cf. 5.3.4) during on-state as well as the maximum blocking voltage V_{max} for a $3\,\text{MV/cm}$ limit regarding dielectric field strength. Note that source and drain contact resistances were omitted for the simulation.

Since the focus of this work is on the gate structure of the MOSFET, no such shielding structures were realized. However, the simulations provide a decent foundation for further investigation and optimization of shielding structures. They show that the trench MOSFET concept is susceptible to high field strength in the gate dielectric at the exposed trench bottom, which makes effective shielding mandatory. The shielding via an additional p-type region is the most effective solution but must be tailored specifically with respect to device geometry and application requirements.

7 Summary and outlook

7.1 Summary

During the course of this work, fully vertical trench MOSFETs have been fabricated on bulk GaN substrates. In contrast to the state-of-the-art technology, the devices are based on a chlorine- and metal-free trench gate process but showed competitive performance in terms of area specific on-resistance. All necessary doping originated from epitaxial layers and no ion implantation was required.

Using ICP etching, based on a gas mixture of SF_6 and Ar, deep trenches with aspect ratios of ≈ 1.8 were achieved without the use of chlorine chemistry. Due to the non-volatility of the etch product GaF_3, strong physical etching was required. Compared to chlorine etched structures, this leads to increased roughness and microtrenching. However, post treatment in alkaline solution resulted in trenches with vertical sidewalls, oriented along the vertical a- and m-planes of the GaN crystal with plasma induced roughness and microtrenching strongly reduced or eliminated. Orientation along the m-plane did lead to a smooth and nearly perfectly crystal aligned surface. Orientation along the a-plane, however, resulted in a more irregular surface. This difference is due to the fact that the produced facets did not originate from pure a-planes but rather consisted of m-plane facets that are inclined to each other at the hexagonal angle of 120 °, resulting in protruding pillars, which significantly increase the interface roughness. Another difference that originated from the trench orientation, is the shape of the trench bottom after the wet etching, with a smooth and concave appearance in the case of a-plane orientation and a pointy one for m-plane orientation. This shows that the trench geometry strongly depends on the actual orientation with respect to the GaN crystal and thus an effect on the MOS interface is possible since it is located on the trench sidewall. Independent from the orientation, by reducing the trench width to $\approx 1.5\,\mu m$, the impact of microtrenching for the final trenches was significantly reduced. The resulting trenches were comparable to those, which were fabricated by state-of-the-art chlorine based plasma etching and TMAH post treatment. The outcome shows the competitiveness of the chlorine-free process with state-of-the-art GaN etching and that it offers a viable alternative for process environments where chlorine chemistry is either not available or not acceptable due to contamination or safety restrictions.

To evaluate the plasma and wet etched GaN surface with respect to surface quality and electrical performance, planar and trench MOS capacitors were fabricated and leakage current and dielectric breakdown field strength were measured under various conditions.

AFM measurements showed that plasma etching increased roughness and high leakage current density was observed for MOS capacitors fabricated on such a surface. However, roughness itself could be dismissed as the relevant factor, since subsequent wet etching of the plasma etched surface preserved the higher roughness, but restored the leakage current to the level of the pristine surface. Concerning the material stack and process flow of the MOS structures, the outcome of the experiments suggested LPCVD SiO_2 in combination with a poly silicon gate electrode as the most promising variant. Compared to other dielectrics such as LPCVD Si_3N_4 or ALD Al_2O_3, and in contrast to gate structures with metal gate electrode, the LPCVD SiO_2-poly Si configuration showed superior performance regarding dielectric breakdown field strength, leakage current density and hysteresis. Especially for higher temperatures above 400 K, the poly Si gate emerged as the more robust choice, compared to its metal based counterpart.

Using this configuration and the chlorine-free trenching process, MOSFETs with planar and trench gate structure were fabricated and characterized. The area specific on-resistance of trench MOSFETs with 16 µm pitch size was in the range of $R_{\mathrm{DSon}} = 10\,\mathrm{m\Omega\,cm^2}$, which is comparable to state of the art devices. The switching capability of the fabricated devices was demonstrated for frequencies up to 100 kHz and switching times of ≈ 30 ns were measured. In addition, the inversion channel field effect mobility μ_{FE} was determined. Interestingly, no significant difference in field effect mobility was observed between a- and m-plane oriented devices despite clear distinctions in terms of surface condition. A likely reason for this phenomenon is a high interface defect density, which reduces the overall channel mobility and overshadows any distinction between the two crystal facets. Although no measurable difference was found between m- and a-plane oriented devices, the results showed that the mobility for a vertical interface in general ($\mu_{\mathrm{FE}} \approx 10\,\mathrm{cm^2/Vs}$) was noticeably lower than for a planar one where $\mu_{\mathrm{FE}} \approx 30\,\mathrm{cm^2/Vs}$ was obtained. However, both values are lower than it would be expected from literature findings, which indicates suboptimal conditions at the MOS interface with interface defects being the most likely reason.

An estimation of interface charge and defect density was made by fitting a TCAD model to the measured transfer characteristics of the trench MOSFETs. The outcome supported the assumption of a high defect and charge density at the GaN to SiO_2 interface and yielded a carrier mobility of $\mu_{\mathrm{inv}} = 4\,\mathrm{cm^2/Vs}$. The simulation also supports the presumption of a generally positive interface charge, which is the reason for an unexpectedly low threshold voltage of the fabricated MOSFETs. This interface charge and the interface quality in general, are the most pressing points to be addressed in future work. Although field shielding during the off-state was not part of this work, it is an essential aspect of the power MOSFET. Therefore, simulations for differently shielded trench MOSFETs were carried out. The results point out the necessity of shielding structures and provide a starting point for future experimental work.

7.2 Outlook

This section treats possible future work concerning aspects that were either not addressed in this work or did emerge as crucial points from the presented experiments. The focus should lie on measures to improve the MOS interface quality to achieve a stable and positive threshold voltage and to increase carrier mobility. The examination of threshold voltage shifting suggested a high density of interface charges and defects to be responsible for the low threshold voltage. To address this challenge, the deposition procedure of the dielectric layer and the subsequent annealing step must be optimized. Although the high temperature LPCVD method yielded dielectric layers of good quality, the effect on the GaN surface may well be a negative one and deposition at lower temperature needs to be considered as an alternative. The simulation set-up can be used to check and validate the progress beyond an increase in drain current and field effect mobility. By fitting the transfer curves of differently processed MOSFETs, a change in interface charge- and defect density can be monitored to a certain degree and can thus help to identify the most promising process changes and adaptions. The simulation of shielding structures can act as foundation for experimental work on this topic, which needs to be addressed in future work to achieve competitive blocking performance.

Although the chlorine-free etching method yields competitive results, it requires an elaborated mask system, which limits the minimum trench size. If chlorine based etching is available and tolerated in the process environment, it might lead to smaller trenches with a more favorable geometry and, due to less physical etching, to a reduction in plasma induced damage. Concerning the subsequent wet etching, the focus should lie on the m-plane oriented trench with its smooth and crystal plane oriented surface. However, the pointy shape of the trench bottom in this case will be critical with regard to dielectric field strength and a thick bottom oxide might be necessary. This leads to the penultimate point that needs to be addressed, which is active shielding. If a high blocking voltage of 600 V and above is to be realized without violating reliability and lifetime requirements, deep p-type regions must be introduced and drift layer thickness and doping concentration need to be optimized.

Lastly, the migration to 6 or 8 inch GaN-on-silicon wafers could help in optimizing and simplifying the process flow in general. Critical steps such as lithography, deposition and dry etching can be conducted under more stable conditions, leading to results that are better reproducible and can be easier controlled compared to processes on 2 inch substrates. By addressing these challenges, GaN trench MOSFETs can become competitive or superior to their SiC based counterparts in terms of cost and performance. This work provides a foundation for further development of metal-free gate structures of different GaN based devices and promotes the incorporation of GaN related fabrication steps into conventional process flows.

A Appendix

A.1 Chemical vapour deposition

One of the most important deposition methods in the semiconductor industry is chemical vapor deposition (CVD). The basic principle is the introduction of a gaseous precursor in combination with a diluting gas onto a heated substrate. Depending on the process, epitaxial, polycrystalline or amorphous layers can be deposited. The precursors are transported into the reaction chamber and onto the substrate surface where they get adsorbed. Then a chemical reaction takes place, during which a layer is gradually formed. Byproducts of the reaction are pumped out of the reaction chamber. Depending on the CVD type, process temperatures are in the range of 200-1600 °C and reactions take place at pressures between millitorr and several torr. Advantages of CVD compared to physical vapour deposition methods, such as molecular beam epitaxy or evaporation, are the following. Liquid or gaseous precursors allow an easier variation of stoichiometry and higher purity can be achieved. Deposition is typically more conformal and ultra high vacuum is not required. Disadvantageous are the usually hazardous and often expensive precursors that are used in CVD techniques. Common CVD types are plasma enhanced (PE)CVD, atmospheric pressure (AP)CVD and low pressure (LP)CVD. Table A.1 compares these methods and their respective traits. A typical technique, used for the deposition of metal related substances, is metal organic (MO)CVD, which utilizes organic molecules in the precursors to achieve better volatility of the metal containing compounds. This method if often used for epitaxial growth of III-V-compound semiconductors.

Since used in this work, LPCVD and PECVD will be discussed here. Both techniques can be used to deposit various types of thin layers, including the here relevant films of SiO_2 and Si_3N_4. Depending on process and film requirements, both methods have advantages and disadvantages. The low pressure during LPCVD processing allows a high mass transfer compared to the low deposition rate. This results in a highly conformal and uniform film characteristic. Furthermore, LPCVD layers feature high purity, low defect density and good thermal stability. However, the method requires high temperatures of 700-900 °C, which can be problematic for some materials due to decomposition or stress. This is the major difference to PECVD. The plasma assisted process allows precursor activation at significantly lower temperatures (250-350 °C) and in addition achieves typically a higher deposition rate. However, layer quality is not as good as for LPCVD and, due to a higher degree of gas incorporation, thermal stability is reduced. An

important point is also the poorer conformity of the deposited layer and less uniformity across the substrate.

Table A.1: Comparison of common CVD methods used for the deposition of thin Si_3N_4 and SiO_2 films.

	Atmospheric pressure CVD	Low pressure CVD	Plasma enhanced CVD
Temperature (°C)	300-500	500 - 900	100 - 400
Conformity	poor	high	poor
Film quality	good	excellent	poor
Typical reaction for SiN_x	-	$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H$	$SiH_4 + NH_3 \rightarrow SiN_x{:}H{+}3H_2$
Typical reaction for SiO_2	-	$SiCl_2H_2{+}2N_2O \rightarrow SiO_2 + 2HCl + 2N_2$	$SiH_4 + N_2O \rightarrow SiO_2 + 2H_2 + 2N_2$

A sub-method of CVD, briefly discussed here, is atomic layer deposition (ALD). The basic principle is the same as for CVD but a special property of the used precursor in combination with precisely tailored process conditions allows the deposition of mono layers and thus excellent control over the film thickness. The procedure consists of a four step cycle as illustrated in figure A.1. Similar as for the CVD process, in step one a precursor is introduced into the chamber and deposited on the substrate. The properties of the used precursor are such, that the bond energy between the first monolayer and the substrate is higher than the chemisorption bond energy to the second deposited layer. If pressure and temperature are chosen correctly, no further material is deposited on the first monolayer and excess precursor is purged out of the chamber during the second step. Step three is basically a repetition of step one but with a different precursor. Again, precursor and process conditions are tailored in a way that only one monolayer can be formed on the layer deposited during step one. Step four then purges excess material of the second precursor. This concludes one cycle and leaves one compound monolayer on the substrate. By repeating these steps, a specified number of layers can be deposited, which allows quasi perfect control over the final film thickness.

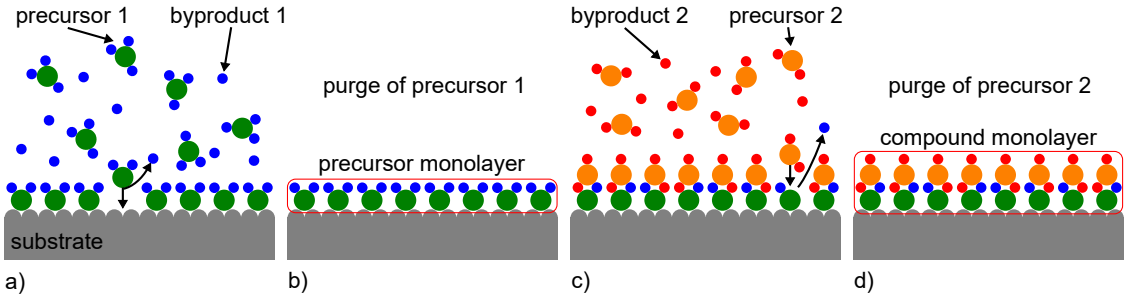

Figure A.1: Consecutice cycles of the ALD process. a) Introduction and reaction of precursor 1. b) Purge of byproducts and excess of precursor 1. c) Introduction and reaction of precursor 2. d) Purge of byproducts and excess of precursor 2.

A.2 Photolithography

Semiconductor device technology requires the fabrication of sub millimeter and sub micrometer structures. They must be fabricated in large numbers and with tolerances on the nanometer scale. To achieve this, the method of choice is a photolithography cycle as illustrated in figure A.2. The initial step of the cycle is the deposition of a photo sensitive resist onto the wafer or substrate. Typically, spin coating is used to achieve resist layer thicknesses ranging from 100 nm to several micrometers. Although alternatives like spray coating or doctor blading exist, spin coating is by far the most common technique. The resist is usually based on an organic solvent, which evaporates during the drying process. Remaining solvent, trapped in the dried layer, is removed by baking the resist on a hot plate.

In the next step, the resist layer is covered by a mask and then exposed to UV-light. Depending on the photoresist type, the exposure can have two different effects. For a so called positive resist, exposure to UV-light alters the chemical structure in such a way that the resist becomes soluble in the water based developer, while resist that was not exposed remains insoluble. For a negative resist it is the other way around. Exposure leads to a rearranging of the chemical bonds in the resist, which makes it not soluble in the developer, while resist that was not exposed is dissolved in the developer. In both cases, the image of the mask, positive or negative depending on the resist type used, is transferred onto the substrate.

The remaining resist acts as a protection layer during subsequent etching or implantation procedures. Apart from the desired structure size, this subsequent procedure essentially determines what resist layer thickness is necessary in the first place. After the etching or implantation process, the resist is removed either by dissolving in a so-called resist stripper solution or via oxygen plasma, which effectively removes the carbon based photoresist. The underlying layer should not be affected by the resist removal procedure and the method is chosen accordingly. This concludes the lithography cycle. Modern semiconductor devices need multiple of these cycles in order to create the required structures.

A.3 Atomic force microscopy

Atomic force microscopy (AFM) is used for surface characterization and can achieve atomic resolution. Due to its versatility, e.g. probing on conducting or non conducting surfaces and in different environments, e.g. submersed, under vacuum or in atmospheric ambient, it is used in multiple areas like physics, material science, biology and chemistry. AFM is based on the force interaction between the sample surface and an atomically sharp probing tip. As depicted in figure A.3 a), the tip is located on a cantilever and scanned over the sample surface via piezoelectric motors. Tip and cantilever are usually fabricated from one piece of silicon or silicon nitride in an etching process. The cantilever

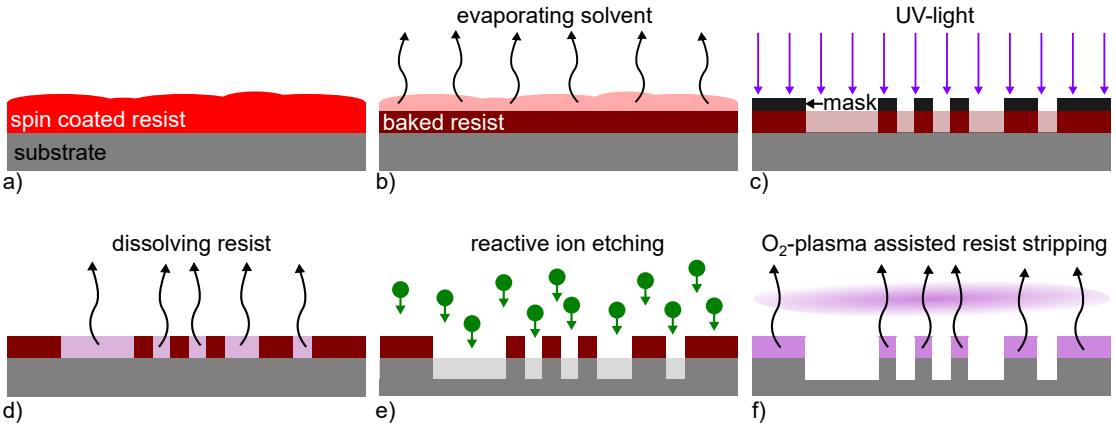

Figure A.2: Schematic depiction of a lithography cycle for positive photoresist. a) Resist deposition via spin coating. b) Resist baking. c) Exposure with UV-light. d) Dissolving of exposed resist in developer solution. e) Layer structuring. Reactive ion etching is depicted exemplary. f) Resist stripping, oxygen plasma is depicted exemplary.

length is in the range of tens to hundreds of micrometers with a spring constant in the range of 10 to 100 N/m. Surface topography is mimicked by the probing tip and changes in height are recorded by tracing a reflected laser beam with a segmented photo diode.

The forces that arise between tip and sample can be categorized into long and short range forces. The former are dominated by van der Waals interaction and include the electrostatic force along with chemical forces like the Stillinger–Weber potential and Tersoff potential [152]. The character of these forces is an attractive one, as is illustrated in figure A.3 b). As the tip gets closer to the surface repulsive short range forces, originating from coulomb interaction and overlap of electron orbitals, become relevant. By exploiting these forces, surface topography can be measured via three differed probing modes. Namely contact- tapping- and non-contact mode. During contact mode probing, the tip to sample distance is so small that occurring forces are exclusively repulsive. Scanning can take place in two different ways, constant height or constant force. Since no feed back loop is needed, constant height allows faster scanning speed but involves the risk of tip crashing, if surface topography is too large. If sample damage or contamination is to be avoided, non-contact probing is used. While oscillating at its resonance frequency, with an amplitude of a few nanometers, the cantilever is moved across the sample surface. Any change of the force acting on the tip, occurring due to surface topography, affects the resonance frequency. By using a feed back loop, the resonance frequency can be restored by changing the tip height. Thus, the surface topography is mimicked by recording the tip height adjustment. The tapping mode is similar to the non-contact mode but oscillation amplitudes are much larger so that the tip transverses a wider range of the force curve and short range forces can be detected as well.

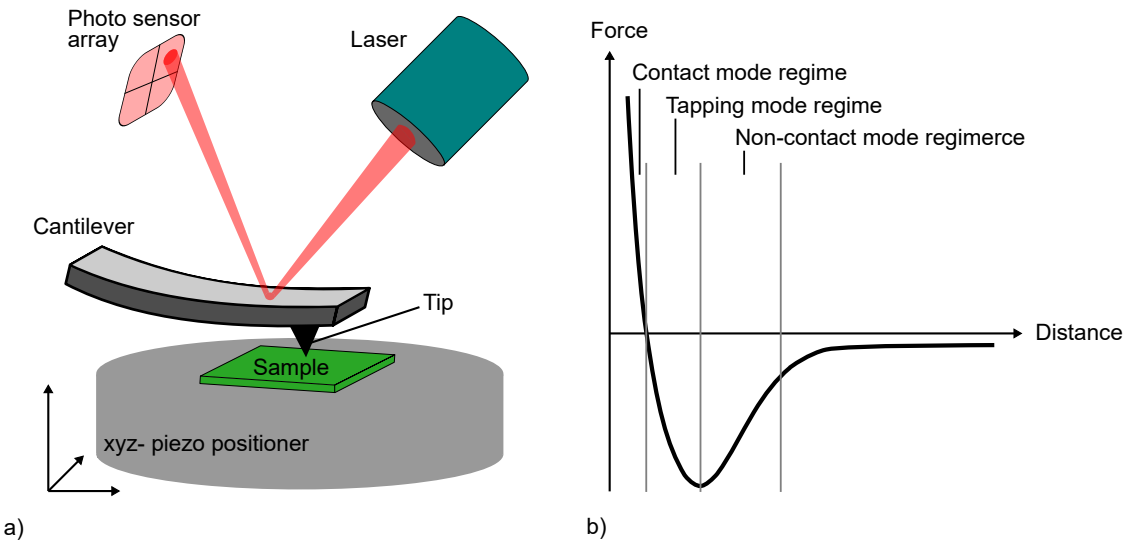

Figure A.3: a) Schematic AFM set up. b) Tip to surface force as function of distance. Also depicted are the distance regimes used for different measuring methods. Note that the transition between the regimes is continuous.

A.4 Scanning electron microscopy

Optical microscopy is an easy and quick option to observe sample features with small dimensions. There are, however, two drawbacks. The first one is the resolution limit, which is in the range of 200-1000 nm due to the wave length of the used light. This is in most cases insufficient for the characterization of modern semiconductor devices. The second drawback is the limitation to surface observation. Subsurface examination is usually not possible for optical microscopy, although infrared light can be used as see through technique.

A popular alternative to optical microscopy is electron microscopy. Due to the significantly smaller de Broglie wavelength of kilovolt electrons (10-30 pm), it is no limitation for resolution and magnifications of 500 000 and more can be achieved. For electron microscopy, diameter and quality of the electron probing beam are the resolution limiting criteria. Furthermore, it allows subsurface examination, for example crystalline structure or chemical composition. Both aspects, nanometer resolution and subsurface characterization, are of vital importance for semiconductor device characterization.

The most common type is scanning electron microscopy (SEM). Another common technique is transmission electron microscopy (TEM). Compared to SEM, TEM provides higher resolution but also requires much more elaborate equipment and special specimen preparation is needed. In most cases, regarding semiconductor device development, SEM resolution is sufficient and since used in this work, focus will be on this technique.

Figure A.4 a) shows the schematic SEM setup. A hot tungsten filament or field emission gun is typically the source of electrons, which are accelerated to energies in the range of 0.1 to 30 keV. Using electromagnetic coils as condenser lenses, the electron beam is collimated

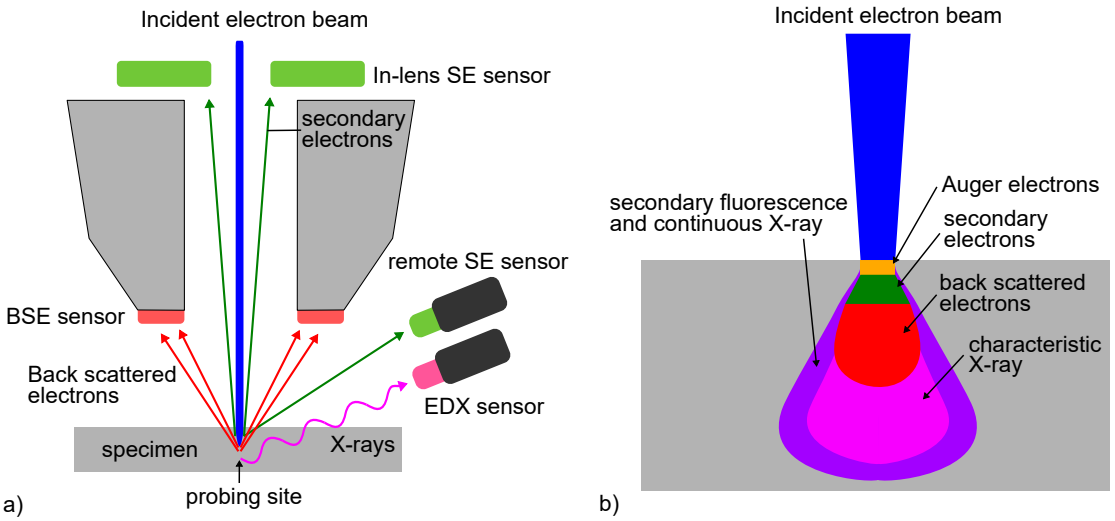

Figure A.4: a) Schematic SEM set up. b) Electron beam interaction with the specimen and detectable signals resulting thereof.

and scanned across the specimen surface. Unlike optical microscopy, electron microscopy requires high vacuum to avoid electron collision with air molecules. A set of various detectors is used to generate an image of the specimen surface and subsurface features. If the electron beam hits the specimen, multiple reactions take place. As illustrated in figure A.4 b), different types of electrons and radiation are generated at different penetration depths. In most cases, secondary electrons are used for the image generation. These electrons are emitted from a sample region $\approx$ 10-50 nm deep after inelastic collisions between primary beam electrons and sample material and thus provide surface related information. Depending on the position of the secondary electron (SE) sensor, high image resolution (In-lens) or higher topography contrast (remote) can be achieved. Another common detector type is the back scattered electron (BSE) sensor which can provide a certain degree of material contrast. A powerful method to perform elemental analysis is energy-dispersive X-ray spectroscopy (EDX). Using the characteristic X-ray spectrum emitted from the sample, a spatial distribution of elemental composition in terms of mass percentage can be measured.

A.5 Transfer length module measurement

The method of choice to determine the resistance of a metal-semiconductor contact, is the transfer length module (TLM) measurement. As illustrated by the inset in figure A.5 a), metal pads with different distances between them, are fabricated in the same way as the contacts of which the resistance is to be determined. The voltage drop between two pads with distance D_{Pad} is measured for a set current. The resulting curve is displayed in figure A.5 a). As shown in b), the respective resistance between two pads is calculated and extrapolated for a pad distance of $D_{\mathrm{Pad}} = 0$. The y-axis intersect of the plot corresponds to twice the contact resistance R_{C} of a measurement pad. The slope, i.e.

resistance per micrometer pad distance, times the pad width W_{Pad} is the sheet resistance R_{Sh} of the semiconductor layer that conducts the current. Depending on the quality of the contacts, ohmic behavior provided, the transfer length L_{T} must be taken into account. It is defined as the distance between contact edge and the point at which the current density has dropped to 1/e of the maximum density, which is found on the edge. According to [113], the transfer length is given as

$$L_{\mathrm{T}} = \sqrt{\frac{\rho_{\mathrm{C}}}{R_{\mathrm{Sh}}}} = \frac{R_{\mathrm{C}} W_{\mathrm{Pad}}}{R_{\mathrm{Sh}}} \quad \text{with the specific contact resistance} \quad \rho_{\mathrm{C}} = \frac{R_{\mathrm{C}}^2 W_{\mathrm{Pad}}^2}{R_{\mathrm{Sh}}}. \tag{A.1}$$

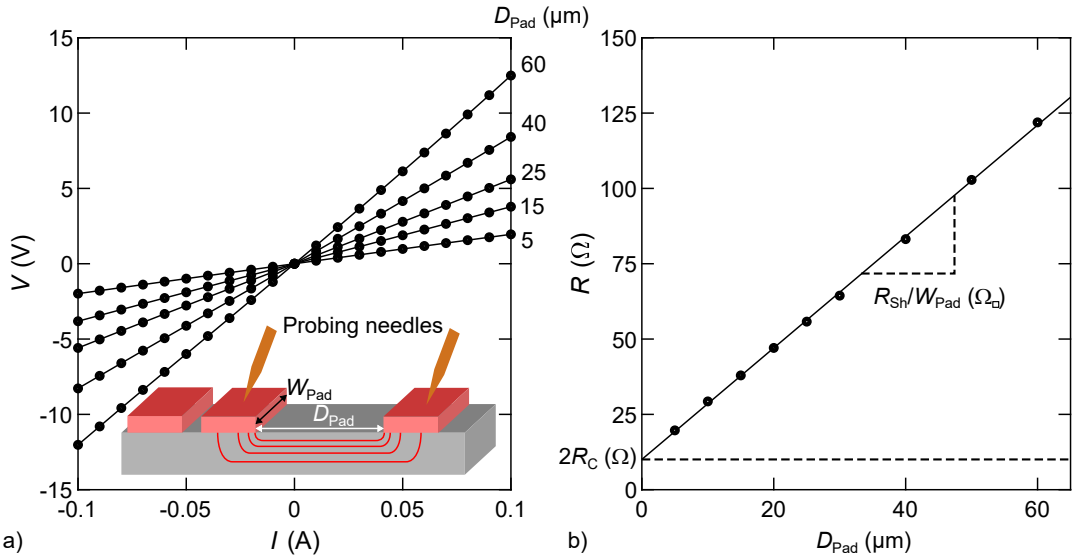

Figure A.5: a) Inverse IV-characteristic for different pad distances D_{Pad}. The inset shows the schematic of a TLM with the transfer length concept illustrated. b) Pad to pad resistance as function of pad distance D_{Pad}.

A.6 Process parameters

Table A.2: Part 1: Listing of process steps and corresponding parameters.

Process step and material	Parameters
Gate dielectric deposition, LPCVD SiO_2	$T = 880\,°C$; $p = 550\,mTorr$ (SiH_2Cl_2, N_2O); $d = 50\,nm$ at 5 nm/min
Gate dielectric deposition, LPCVD SiN	$T = 775\,°C$; $p = 250\,mTorr$ (SiH_2Cl_2, NH_3); $d = 50\,nm$ at 4 nm/min
Gate dielectric annealing	$T = 800\,°C$; $p = 1\,atm$ N_2 for 1 h
Gate contact deposition, n-type LPCVD poly Si	$T = 580\,°C$; $p = 350\,mTorr$ (SiH_4, 1:9 PH_3:H_2)
Gate contact annealing	$T = 900\,°C$; $p = 1\,atm$ N_2 for 1 h
Radio Corporation of America clean 1	NH_4OH:H_2O_2:DI-H_2O, 1:2:7
Radio Corporation of America clean 2	HCL::H_2O_2:DI-H_2O, 1:2:7
ICP aSi etching	$p = 5\,mTorr$ (C_4F_8, SF_6, He, H_2; 8, 20, 300, 8 sccm); 800/60 W coil/platen power; etch/pause 5/20 sec; $T_{chuck} = 10\,°C$; rate 25-27 nm/cycle
ICP aSi soft etching	$p = 25\,mTorr$ (SF_6, He; 20, 300 sccm); 1000/0 W coil/-platen power; continuous etch; $T_{chuck} = 10\,°C$; rate 10 nm/sec
ICP SiO_2 etching	$p = 5\,mTorr$ (C_4F_8, He, H_2; 15, 240, 10 sccm); 2000/715 W coil/platen power; etch/pause 3/12 sec; $T_{chuck} = 0\,°C$; rate 40-44 nm/cycle
ICP SiO_2 soft etching	$p = 5\,mTorr$ (C_4F_8, SF_6; 46 ,10 sccm); 400/150 W coil/-platen power; etch/pause 3/20 sec; $T_{chuck} = 0\,°C$; rate 10-11 nm/cycle
ICP GaN main etching	p =5-10 mTorr (Ar, SF_6; 10, 35 sccm); 1100/900 W coil/-platen power; continuous etch; $T_{chuck} = 10\,°C$; rate 900-1350 nm/min
ICP GaN soft etching	$p = 10\,mTorr$ (Ar, SF_6; 10 ,35 sccm); 550/250 W coil/-platen power; continuous etch; $T_{chuck} = 10\,°C$; rate 100 nm/min
Resist plasma stripping	$p = 1\,Torr$ (O_2; 500 sccm); 700 W power; 1 h continuous etch
Mask layer deposition, PECVD SiO_2	$T = 350\,°C$; $p = 1\,Torr$ (SiH_4, N_2O, Ar; 4, 50, 490 sccm); 75 W power d =1-3 µm at 70 nm/min

Table A.3: Part 2: Listing of process steps and corresponding parameters

Mask cap layer deposition, PECVD aSi	T = 350 °C; p = 1 Torr (SiH_4, Ar; 25, 490 sccm); 10 W power d =0.5-1.5 µm at 30 nm/min
GaN wet etch	T =25-90 °C; 25 % TMAH in H_2O or 33 % KOH in H_2O
SiO_2 wet etch	T = 25 °C; 7:1 BOE in H_2O plus ≈ 10 $\%_{vol}$ 99.9 % acetic acid
Ion beam metal etching	T = 5 °C; p = 30 Torr; etching angle 30 °; 200 mA beam current; etching ions Ar
Lithography procedure	Resist: Microchemicals AZ ECI 3012; spin coating speed: 4000 rpm; pre bake: 120 s at 90 °C; exposure time: 6 s; development: 60 s in Microchemicals AZ MIF 726
Aluminum wet etching	T = 60 °C; ultra sonic; (phosphoric acid ,nitric acid, acetic acid, H_2O; 73:3:3:21)

A.7 Device simulation using technology computer aided design software

To realistically model device related quantities like doping, carrier mobility and lastly the actual current flow, comprehensive knowledge of parameters and boundaries is necessary. Even in two dimensions, relations between different quantities are complex. They depend on multiple factors and usually iterative and numerical solving is required. Based on empirical models and fundamental physics, TCAD software simulates fabrication and operation of a semiconductor device. This helps saving costs and time during a device development process as potential benefits and drawbacks of certain designs and configurations can be anticipated. The extend to which device performance and behavior in general can be predicted depends on the soundness of the models and parameters on which the simulation is founded. The comprehensive understanding of silicon devices and the process related materials make the associated models and simulations very accurate and reliable. Models for gallium nitride are much less profound and lack comprehensiveness and accuracy. This is mainly due to insufficient understanding of the material and due to a scarcity of consistent data.

The initial step of the simulation procedure is the definition of the device geometry including dimension, form and material of the various regions, which comprise the device. The geometrical setup, used for the simulation of inversion channel carrier mobility, is depicted in figure A.6 a). The image shows one half cell, which is the smallest representative unit of the trench MOSFET. The boundaries to the left and right are defined so that they act as mirrors. Thus the simulation behaves in a way as if infinitely repeating half cells are placed next to each other. The simulation is two dimensional and assumes infinite expansion into the third dimension. Note that boundaries that occur in a real device are not taken into account. Each region, separated by black lines in figure A.6, can

be designed with a unique set of constraints for the underlying mesh, which is displayed in green. Important constraints are minimum and maximum values for width and height of the triangles as well as a maximum aspect ratio. To avoid simulation artifacts, it is important to match the local mesh density with the expected gradient for the simulated quantities. This means that areas with high field strength or current density as well as transition regimes from n- to p-type doping and interfaces in general, must be equipped with a finer mesh. To limit computational effort, higher mesh resolution should be confined to the areas where it is required. This is achieved by running specified refinement statements that increase, within the defined constraints, the mesh density in the specified areas. The result of such a refinement procedure is displayed in figure A.6 b), where especially the MOS inversion channel features a significantly finer mesh.

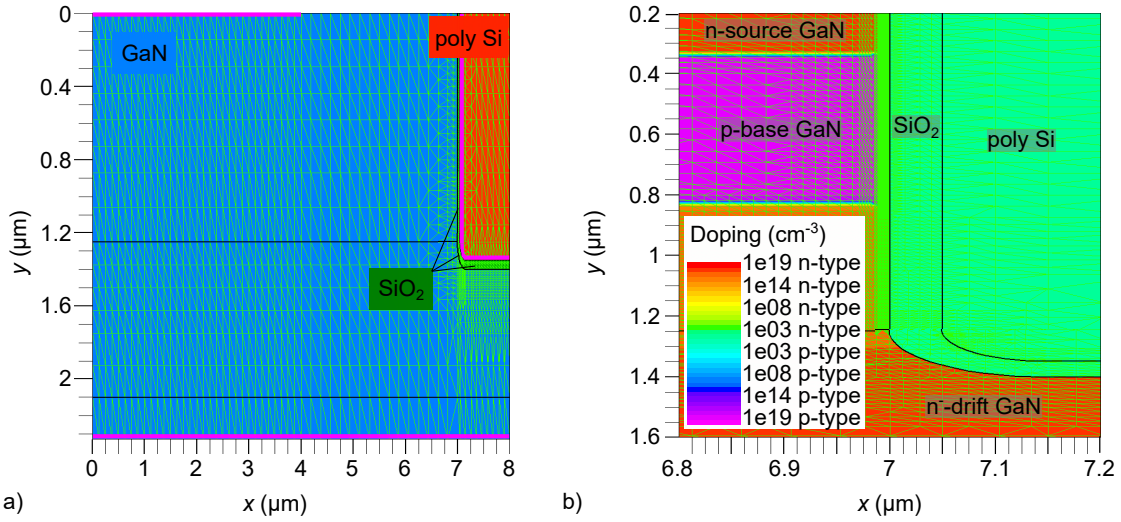

Figure A.6: a) Geometry setup for the carrier mobility simulation. Black lines separate different regions, magenta lines represent electrode interfaces. b) Close up of the channel region after mesh refinement. The contour plot displays the net doping concentration on a logarithmic scale.

After the mesh refinement, electrodes are defined for specific interface sections at the top and bottom of the device for source and drain, respectively (see fig. A.6 a)). The gate electrode is placed at the interface between poly Si and SiO_2.

So far the semiconductor region is defined as GaN with the respective material parameters but without any doping concentration. The Silvaco TCAD tool offers two ways to implement a doping profile. The first one is to simulate ion implantation in the device processing tool Athena. The second way is to specify the doping concentration manually in specific areas. The devices in this work were not subjected to ion implantation but feature only epitaxially doped layers. Therefore, the latter approach was choose. A designated area is defined as uniformly doped with a specified concentration and the transition area is modeled as a Gaussian distribution.

To resemble a real device, the interface conditions must be defined. The interface in this work was modeled with two different imperfections. The first one is a fixed oxide charge density, which is independent from any potential change. The second one is a set of four bands of defect states. Two are modeled with a tail distribution at the valence band for acceptor like states and at the conduction band for defects with donor like character. Two more are modeled as quasi continuous Gaussian distributions, again for acceptor and donor like character, respectively.

In addition to models for incomplete ionization of dopants (see sec. 2.4.3) and the carrier mobility (see sec. 2.4.4), physical relations regarding Shockley-Read-Hall recombination, Auger recombination and band gap narrowing were implemented.

The final part of the simulation code concerns the definition of probing locations and the actual problem solving.

A.8 Silvaco Atlas simulation code

This section contains the code for the transfer curve simulation from the inversion channel carrier mobility section. Note that the parameters are set to the values used for the room temperature transfer curve of the m-plane oriented trench MOSFET.

-Beginning of code

```
#GaN TrenchMOSFET Simulation for Kalibration
######Parameter definition#######################
##################################################
#Lattice tempeprature
set T=300
######Geometry############################
#all values in µm
#half pitch of device
set w_cell=8
#half width of the trench
set w_trench=1
#depth of the trench
set t_trench=1.4
#width of source contact
set w_source=1
#n-source thickness 0.33µm doping
set t_nsource=0.33
set nsource_n_conc=5e18
#p-base layer thickness 0.5um and doping
set t_base=$t_nsource+0.5
```

```
set base_p_conc=1e18
#driftlayer thickness 0.5um and doping
set t_drift=$t_base+0.5
set drift_n_conc=5e16
#border upper driftlayer section
set t_middle=1.5*$t_trench
#substrate thickness 1um and doping
set t_sub=$t_drift+1
set sub_n_conc=1e19
#thickness of gate dielectric
set t_oxide=0.05
#corner rounding of the trench
set r_corner=0.15
#total thicknes from source (top) to drain (bottom)
set t_cell=$t_sub
#position des Source Kontakts
set x_source_left=0
set x_source_right=4

######Doping#####################################
#refinment distance for doping transitions
set roll_1=0.15
set roll_2=0.05
#roll off for gaussian doping
set charac_nsource=0.02/1.52
set charac_pbase=0.05/1.52
set charac_drift=0.05/1.52
set charac_sub=0.02/1.52

######Model parmters#############################
# Boltzmann constant
set kBeV = 1.380649e-23/1.602176634e-19
# electron affinity
set AFFINITY=4.1
set PERMITIVITY=8.9
#(static, 300K)
#Gate Workfunction nPoly Gate
set WF=4.1

# band gap Parameters for BGN model:
#Parameters for temperature dependent Bandgap narrowing
```

```
#Using universal energy bandgap model
#Parameters from Sabui2016:
set EG300=3.458
set EGALPHA=9.09e-4
set EGBETA=830
#Dopingdependence is adopted from Sabui2016
#n-type:
#EC:
set BGNLINDANC=0.5750e-8
set BGNLINDND=1
set BGNLINDBNC=0
#EV:
set BGNLINDANV=1.61e-7
set BGNLINDBNV=1.072e-12

#Für p-Type ist es gerade anders herum
#p-type:
#EC:
set BGNLINDAPC=1.61e-7
set BGNLINDNA=1
set BGNLINDBPC=1.072e-12
#EV:
set BGNLINDAPV=0.5750e-8
set BGNLINDBPV=0

# conduction and valence band edge density of states at 300 K
#Parameters for effective density of states in con and val band
#Specifie NC300, NV300 and respective masse me and mh
#Valence band effective mass in m0 from Narita2019a
set mh=1.7
#Conduction band effective mass in m0 from Narita2019a
set me=0.22
#Valence ans conduction band density of states
set NC300=4.82e15*pow($me, 1.5)*pow(300, 1.5)
set NCF=1.5
set NV300=8.9e15*pow(300, 1.5)
set NVF=1.5
set NC = $NC300 * pow($T/300, $NCF)
set NV = $NV300 * pow($T/300, $NVF)
# Incomplete ioniztion parameters
#Parameters for Silvaco incomplete statement: GCB and GCVB
```

```
#Kalibrated on Narita2018 for n-type, Narita2020 and Kozodoy2000 for p-type.
set GCB=2
set AEDB=0.035
set BEDB=2.25e-8
#Calculation of ionization energy set EDB=$AEDB-$BEDB*pow($ND, 1/3)
set GVB=4
set AEAB=0.241
set BEAB=2.25e-8
#Calculation of ionization energy set EAB=$AEAB-$BEAB*pow($NA, 1/3)

#Parameters for Auger recombination from Sabui2016
set AUGN=3e-31
set AUGP=3e-31
#Shokley read hall recombination Zwei Varianten:
#standard model with parameters from Sabui2016:
#set TAUP0=2e-9
#set TAUN0=0.7e-9
#set ETRAP=0

#Parameter for Radiative recombination
set COPT=1.1e-10

#Impactionization Selberherr mit werten von BaligaBuch2017 == Sabui2016
set AN1=1.5e5
set AN2=1.5e5
set AP1=6.4e5
set AP2=6.4e5
set ANT=0
set APT=0
set MANT=1
set MAPT=1
set BN1=1.41e7
set BN2=1.41e7
set BP1=1.46e7
set BP2=1.46e7
set BNT=0
set BPT=0
set MBNT=1
set MBPT=1
set BETAN=1
set BETAP=1
```

```
#Interface charge (restricted to trench region)
set IntCharge=1.2e13

#Interface defects (restricted to trench region)
set NGD=2.37e12
set WGD=10000
set SIGGDE=1e-16
set SIGGDH=1e-16
#Acceptor like
set EGA=1
set NGA=1.66e12
set WGA=10000
set SIGGAE=1e-16
set SIGGAH=1e-16
#Tail distributionset
#Donor like
set NTD=6.38e12
set WTD=0.0444
set SIGTDE=1e-16
set SIGTDH=1e-16
#Acceptor like
set NTA=5.97e12
set WTA=0.0432
set SIGTAE=1e-16
set SIGTAH=1e-16
#Number of levels (continuous)
#Donor like
set NUMD=40
#Acceptor like
set NUMA=40
#---------------Set Alt CVT Model parameters

#mobility altcvt (parameter definition)
#Bulk Mobility section
set mumin=0.04
set mubp1=2000
set mubp2=2000
set alpha=0.774
set exp1=-2.98
set exp2=-2.836
```

```
set exp3=-6.479
set exp4=0.507
set ref=8.47e14
#Surface Roughness Mobility Parameter Section
set delta=2e14
#1.6e14
set eta=1.6e30
#Surface Phonon Mobility Parameter Section
set spb=1.0e6
set spc=1.077e4
set spn0=1
set beta=0.0284
set ktemp=1
#Coulomb Scattering Mobility Parameter Section
set coulobm_nmob=20
set coulobm_nct=1.34e18
set coulobm_ntt=4.47e10
set coulobm_ntd=2e15
set coulobm_np1=0.8
set coulobm_np2=0.3
set coulobm_nnu=1.176
set coulobm_e0n=2.0e5
set coulobm_ngam=2.0
set coulobm_nkt=1.0
set N_LCRIT =10e-7
set P_LCRIT =10e-7

#Variable calculation (geometry)
#####################################################
set x0_oxide=$w_cell-$w_trench
set x1_oxide=$w_cell
set x2_oxide=$x0_oxide+$r_corner
set y0_oxide=0
set y1_oxide=$t_trench
set y2_oxide=$y1_oxide-$r_corner
set x0_corner_oxide=$x2_oxide
set y0_corner_oxide=$y2_oxide

set x0_gate=$x0_oxide+$t_oxide
set x1_gate=$x1_oxide
set x2_gate=$x2_oxide
```

```
set y0_gate=$y0_oxide
set y1_gate=$y1_oxide-$t_oxide
set y2_gate=$y2_oxide
set x0_corner_gate=$x0_corner_oxide
set y0_corner_gate=$y0_corner_oxide


#Geometry section (generate device geometry)
#####################################################
go devedit

work.area left=0 top=0 right=$w_cell bottom=$t_cell
#-----------------------------------------------
#GaN region lower
region reg=1 mat=GaN points=" 0,$t_cell \
$w_cell,$t_cell \
$w_cell,$t_middle \
0,$t_middle \
0,$t_cell"
#-----------------------------------------------
#GaN region middle
region reg=2 mat=GaN points=" 0,$y2_oxide \
$w_cell,$y2_oxide \
$w_cell,$t_middle \
0,$t_middle \
0,$y2_oxide"
#-----------------------------------------------
#GaN region upper
region reg=3 mat=GaN points=" 0,0 \
$w_cell,0 \
$w_cell,$y2_oxide \
0,$y2_oxide \
0,0"
#-----------------------------------------------
#Gate oxide block
region reg=4 mat=oxide points=" $x0_oxide,$y0_oxide \
$x1_oxide,$y0_oxide \
$x1_oxide,$y1_oxide \
$x2_oxide,$y1_oxide \
$x2_oxide,$y2_oxide \
$x0_oxide,$y2_oxide \
```

```
$x0_oxide,$y0_oxide"
#-------------------------------------------------
#Gate oxide corner
region reg=5 mat=oxide  circle.center="$x0_corner_oxide,$y0_corner_oxide" \
circle.radius=$r_corner \
circle.number.of.edges=60 \
circle.start.angle=90 \
circle.end.angle=180
#-------------------------------------------------
#Gate electrode block
region reg=6 mat=titanium ELECTRODE.ID=1 workfun=$WF points=" \
$x0_gate,$y0_gate \
$x1_gate,$y0_gate \
$x1_gate,$y1_gate \
$x2_gate,$y1_gate \
$x2_gate,$y2_gate \
$x0_gate,$y2_gate \
$x0_gate,$y0_gate"
#-------------------------------------------------
#Gate electrode corner
region reg=7 mat=titanium ELECTRODE.ID=1 workfun=$WF circle.center= \
"$x0_corner_gate,$y0_corner_gate" \
circle.radius=$r_corner-$t_oxide \
circle.number.of.edges=60 \
circle.start.angle=90 \
circle.end.angle=180

#Set Meshing Parameters
#GaN region lower
constr.mesh region=1 default max.height=1 max.width=1 \
min.height=0.25 min.width=0.25
#GaN region middle
constr.mesh region=2 default max.height=0.2 max.width=0.2 \
min.height=0.02 min.width=0.02
#GaN region upper
constr.mesh region=3 default max.height=0.2 max.width=0.2 \
min.height=0.02 min.width=0.001
#Oxide block
constr.mesh region=4 default max.height=0.02 max.width=0.1 \
min.height=0.01 min.width=0.02
#Oxide corner
```

```
constr.mesh region=5 default max.height=0.1 max.width=0.1 \
min.height=0.02 min.width=0.02
#Gate electrode
constr.mesh region=6 default
#Gate electrode corner
constr.mesh region=7 default

base.mesh height=0.5 width=0.2
bound.cond when=automatic max.slope=28 max.ratio=10 rnd.unit=5e-05 \
line.straightening=2 align.points
imp.refine min.spacing=0.001
constr.mesh max.angle=90 max.ratio=10 max.height=2 max.width=1 \
min.height=0.002 min.width=0.002

constr.mesh under.region=4 depth=6*$t_oxide max.height=0.1 max.width=0.5
constr.mesh under.region=4 depth=3*$t_oxide max.height=0.02 max.width=0.2

Mesh Mode=MeshBuild

#save unrefined structure
struct outf=0_dev_temp_unrefined.str

#Mesh refinement section
#####################################################
#Refine channel region
refine mode=x x1=$x0_oxide-6*$t_oxide x2=$x0_gate \
y1=0 y2=$t_trench
refine mode=x x1=$x0_oxide-3*$t_oxide x2=$x0_gate \
y1=0 y2=$t_trench
refine mode=x x1=$x0_oxide-1.5*$t_oxide x2=$x0_gate \
y1=0 y2=$y2_oxide
refine mode=x x1=$x0_oxide-0.5*$t_oxide x2=$x0_gate \
y1=0 y2=$y2_oxide
refine mode=x x1=$x0_oxide-0.5*$t_oxide x2=$x0_gate \
y1=0 y2=$y2_oxide
refine mode=x x1=$x0_oxide-0.2625*$t_oxide x2=$x0_gate \
y1=0 y2=$y2_oxide
refine mode=x x1=$x0_oxide-0.23125*$t_oxide x2=$x0_gate \
y1=0 y2=$y2_oxide

#Refine spreading region
```

```
refine mode=x x1=$x0_oxide-12*$t_oxide x2=$x0_oxide-2*$t_oxide \
y1=$t_base y2=$t_middle
refine mode=x x1=$x0_oxide-2*$t_oxide x2=$x0_oxide-0*$t_oxide \
y1=$y2_oxide y2=$t_trench
refine mode=y x1=$x0_oxide-12*$t_oxide x2=$x0_oxide+6*$t_oxide \
y1=$t_trench+3*$t_oxide y2=$t_middle+6*$t_oxide

#Refine on doping borders

#Substrate to drift region
refine mode=y x1=0 x2=$w_cell \
y1=$t_drift-$roll_1 y2=$t_drift+$roll_1

#n Source to p-base region
refine mode=y x1=0 x2=$x0_oxide-6*$t_oxide \
y1=$t_nsource-$roll_1 y2=$t_nsource+$roll_1
refine mode=y x1=0 x2=$x0_oxide-3*$t_oxide \
y1=$t_nsource-$roll_2 y2=$t_nsource+$roll_2
refine mode=y x1=0 x2=$x0_oxide-0.5*$t_oxide \
y1=$t_nsource-$roll_2 y2=$t_nsource+$roll_2

#p-base to drift region
refine mode=y x1=0 x2=$x0_oxide-6*$t_oxide \
y1=$t_base-$roll_1 y2=$t_base+$roll_1
refine mode=y x1=0 x2=$x0_oxide-3*$t_oxide \
y1=$t_base-$roll_2 y2=$t_base+$roll_2
refine mode=y x1=0 x2=$x0_oxide-0.5*$t_oxide \
y1=$t_base-$roll_2 y2=$t_base+$roll_2



#save refined structure
struct outf=0_dev_temp_refined.str

#Atlas doping section (specifiy doping)
##################################################
go atlas simflags="-p 4"
#simflags="-80"
#go atlas
#Load devedit file
mesh inf=0_dev_temp_refined.str
```

```
electrode name=source x.min=$x_source_left x.max=$x_source_right \
y.min=0 y.max=0
electrode name=drain bottom
electrode number=1 name=gate
#electrode name=gate region=7

#add workfunction to polysilicon-dielectric interface
#contact name=source aluminum
#contact name=drain aluminum

#perform epitaxial doping in atlas

##Substrate region----------------
#uniform variant
#doping uniform n.type concentration=$sub_n_conc \
x.min=0 x.max=$w_cell y.min=$t_drift y.max=$t_cell
#gaussian variant
#roll-off correction
set ymin_Gauss=$t_drift
set ymax_Gauss=$t_cell
doping gaussian n.type concentration=$sub_n_conc \
characteristic=$charac_sub x.min=0 x.max=$w_cell \
y.min=$ymin_Gauss y.max=$ymax_Gauss

##n- drift region----------------
#uniform variant
#doping uniform n.type concentration=$drift_n_conc \
x.min=0 x.max=$w_cell y.min=$t_base y.max=$t_drift
#gaussian variant
#roll-off correction
set ymin_Gausd=$t_base
set ymax_Gausd=$t_drift
doping gaussian n.type concentration=$drift_n_conc \
characteristic=$charac_drift x.min=0 x.max=$w_cell \
y.min=$ymin_Gausd y.max=$ymax_Gausd

##p base region----------------
#uniform variant
#doping uniform p.type concentration=$base_p_conc \
x.min=0 x.max=$w_cell y.min=$t_nsource y.max=$t_base
```

```
#gaussian variant
#roll-off correction
set ymin_Gausp=$t_nsource
set ymax_Gausp=$t_base-0.05
#-0.176
doping gaussian p.type concentration=$base_p_conc \
characteristic=$charac_pbase x.min=0 x.max=$w_cell \
y.min=$ymin_Gausp y.max=$ymax_Gausp

##n+ source region----------------
#uniform variant
#doping uniform n.type concentration=$nsource_n_conc \
x.min=0 x.max=$w_cell y.min=0 y.max=$t_nsource
#gaussian variant
#roll-off correction
set ymin_Gausn=0
set ymax_Gausn=$t_nsource-0.01
doping gaussian n.type concentration=$nsource_n_conc \
characteristic=$charac_nsource x.min=0 x.max=$w_cell \
y.min=$ymin_Gausn y.max=$ymax_Gausn

#Atlas doping output
#uniform variant
struct outf=1_atlas_temp_dope.str

#electrode name=gate region=6
#electrode name=gate region=7
contact number=1 name=gate workfun=$WF

#Specify contacts
#electrode name=drain bottom
contact number=2 name=drain aluminum

#electrode name=source x.min=0 x.max=$x0_oxide y.min=0 y.max=0
contact number=3 name=source aluminum



#Interface-----------------------------------
set xmin=$w_cell-$w_trench-3*$t_oxide
set xmax=$w_cell
```

```
set ymin=0
set ymax=$t_trench+3*$t_oxide

INTERFACE QF=$IntCharge \
X.MIN=$xmin X.MAX=$xmax Y.MIN=$ymin Y.MAX=$ymax

INTDEFECTS continuous \
EGD=$EGD NGD=$NGD WGD=$WGD \
SIGGDE=$SIGGDE SIGGDH=$SIGGDH \
EGA=$EGA NGA=$NGA WGA=$WGA \
SIGGAE=$SIGGAE SIGGAH=$SIGGAH \
NTD=$NTD WTD=$WTD \
SIGTDE=$SIGTDE SIGTDH=$SIGTDH \
NTA=$NTA WTA=$WTA \
SIGTAE=$SIGTAE SIGTAH=$SIGTAH \
NUMD=$NUMD NUMA=$NUMA

#############################################################
#Material, Model, Mobility, Impact and Output section-------

#Material---------------------------------
Material \
permittivity=$PERMITIVITY affinity=$AFFINITY \
GCB=$GCB GVB=$GVB \
NC300=$NC300 NV300=$NV300 \
MV=$mh MC=$me \
A.EAB=$AEAB B.EAB=$BEAB A.EDB=$AEDB B.EDB=$BEDB \
EG300=$EG300 EGALPHA=$EGALPHA EGBETA=$EGBETA \
BGN.LIND.ANC=$BGNLINDANC \
BGN.LIND.ND=$BGNLINDND \
BGN.LIND.BNC=$BGNLINDBNC \
BGN.LIND.ANV=$BGNLINDANV \
BGN.LIND.BNV=$BGNLINDBNV \
BGN.LIND.APC=$BGNLINDAPC \
BGN.LIND.NA=$BGNLINDNA \
BGN.LIND.BPC=$BGNLINDBPC \
BGN.LIND.APV=$BGNLINDAPV \
BGN.LIND.BPV=$BGNLINDBPV \
AUGN=$AUGN AUGP=$AUGP \
COPT=$COPT \
N.SCH.MIN=$NSCHMIN \
```

```
P.SCH.MIN=$PSCHMIN \
N.SCH.MAX=$NSCHMAX \
P.SCH.MAX=$PSCHMAX \
N.SCH.GAMMA=$NSCHGAMMA \
P.SCH.GAMMA=$PSCHGAMMA \
N.SCH.NREF=$NSCHNREF \
P.SCH.NREF=$PSCHNREF

#Model---------------------------------
model temp=$T incomplete SCHSRH auger ni.fermi  BGN.LIND  print

#Mobility------------------------------
#alt cvt model with relative parameters
mobility \
altcvt.n ^altcvt.p \
alt.n.mumin=$mumin \
alt.n.mubp1=$mubp1 \
alt.n.mubp2=$mubp2 \
alt.n.alpha=$alpha \
alt.n.exp1=$exp1 \
alt.n.exp2=$exp2 \
alt.n.exp3=$exp3 \
alt.n.exp4=$exp4 \
alt.n.nref=$ref \
alt.p.mumin=$mumin \
alt.p.mubp1=$mubp1 \
alt.p.mubp2=$mubp2 \
alt.p.alpha=$alpha \
alt.p.exp1=$exp1 \
alt.p.exp2=$exp2 \
alt.p.exp3=$exp3 \
alt.p.exp4=$exp4 \
alt.p.nref=$ref \
alt.n.delta=$delta \
alt.n.eta=$eta \
alt.p.delta=$delta \
alt.p.eta=$eta \
alt.n.spb=$spb \
alt.n.spc=$spc \
alt.n.spn0=$spn0 \
alt.n.beta=$beta \
```

```
alt.n.ktemp=$ktemp \
alt.p.spb=$spb \
alt.p.spc=$spc \
alt.p.spn0=$spn0 \
alt.p.beta=$beta \
alt.p.ktemp=$ktemp \
coulomb.nmob=$coulobm_nmob \
coulomb.nct=$coulobm_nct \
coulomb.ntt=$coulobm_ntt \
coulomb.ntd=$coulobm_ntd \
coulomb.np1=$coulobm_np1 \
coulomb.np2=$coulobm_np2 \
coulomb.nnu=$coulobm_nnu \
coulomb.e0n=$coulobm_e0n \
coulomb.ngam=$coulobm_ngam \
coulomb.nkt=$coulobm_nkt \
coulomb.pmob=$coulobm_nmob \
coulomb.pct=$coulobm_nct \
coulomb.ptt=$coulobm_ntt \
coulomb.ptd=$coulobm_ntd \
coulomb.pp1=$coulobm_np1 \
coulomb.pp2=$coulobm_np2 \
coulomb.pnu=$coulobm_nnu \
coulomb.e0p=$coulobm_e0n \
coulomb.pgam=$coulobm_ngam \
coulomb.pkt=$coulobm_nkt \
N.LCRIT=$N_LCRIT \
P.LCRIT=$P_LCRIT \

#Methode--------------------------------
method newton itlimit=25 trap atrap=0.5 maxtrap=10

#Impact---------------------------------
IMPACT SELB AN1=$AN1 AN2=$AN2 AP1=$AP1 \
AP2=$AP2 A.NT=$ANT A.PT=$APT M.ANT=$MANT \
M.APT=$MAPT BN1=$BN1 BN2=$BN2 BP1=$BP1 \
BP2=$BP2 B.NT=$BNT B.PT=$BPT M.BNT=$MBNT \
M.BPT=$MBPT BETAN=$BETAN BETAP=$BETAP

#Output---------------------------------
output con.band val.band flowlines e.mob h.mob qss
```

```
#probing
#-------------------------------
#Probe at channel center (center in y-direction) at 3 points)
#distance from interface in µm
set xoff=-0.000
set xP1=$xoff+$x0_oxide
set xP2=$xoff+$x0_oxide-0.0007325
set xP3=$xoff+$x0_oxide-0.0015
set xP4=$xoff+$x0_oxide-0.0022
set xP5=$xoff+$x0_oxide-0.0029
#absolute y-coordinate of channel center
set yPDelta=0.68
set yP=0.58594
set yPu=$yP-$yPDelta
set yPl=$yP+$yPDelta

#current density
probe name=TotCurrentDens_1 J.total x=$xP1 y=$yP
probe name=TotCurrentDens_2 J.total x=$xP2 y=$yP
probe name=TotCurrentDens_3 J.total x=$xP3 y=$yP
probe name=TotCurrentDens_4 J.total x=$xP4 y=$yP
#Fperp
probe name=F_perp_1 field Dir=0 x=$xP1 y=$yP
probe name=F_perp_2 field Dir=0 x=$xP2 y=$yP
probe name=F_perp_3 field Dir=0 x=$xP3 y=$yP
probe name=F_perp_4 field Dir=0 x=$xP4 y=$yP
#Electron mobility paralell to channel
probe name=Nmobil_1 N.mob Dir=90 x=$xP1 y=$yP
probe name=Nmobil_2 N.mob Dir=90 x=$xP2 y=$yP
probe name=Nmobil_3 N.mob Dir=90 x=$xP3 y=$yP
probe name=Nmobil_4 N.mob Dir=90 x=$xP4 y=$yP
#Conductivity
probe name=NConduc_1 conductivity x=$xP1 y=$yP
probe name=NConduc_2 conductivity x=$xP2 y=$yP
probe name=NConduc_3 conductivity x=$xP3 y=$yP
probe name=NConduc_4 conductivity x=$xP4 y=$yP
#Carrier density (electrons)
probe name=Nelec_1 N.conc x=$xP1 y=$yP
probe name=Nelec_2 N.conc x=$xP2 y=$yP
probe name=Nelec_3 N.conc x=$xP3 y=$yP
```

```
probe name=Nelec_4 N.conc x=$xP4 y=$yP
#Fparalell upper and lower
probe name=F_paramiddle_1 field Dir=90 x=$xP1 y=$yP
probe name=F_paramiddle_2 field Dir=90 x=$xP2 y=$yP
probe name=F_paramiddle_3 field Dir=90 x=$xP3 y=$yP
probe name=F_paramiddle_4 field Dir=90 x=$xP4 y=$yP
#Probe Interface charges
probe name=Prob_DonContDensity DON.CINTTRAP x=$xP1 y=$yP
probe name=Prob_AccContDensity ACC.CINTTRAP x=$xP1 y=$yP
probe name=Prob_IntC INT.CHARGE x=$xP1 y=$yP

#solving section
#------------------------------
solve init
save outf=init.str
#log outf=transfer_15V_newMesh_0.log
solve vdrain=0
solve vdrain=0.1
solve vgate=0
solve vstep=-0.2 vfinal=-5 name=gate

log outf=QF_$"IntCharge"_GaussFacAcc_$"IntdefFacGaussAcc"_ \
GaussFacDon_$"IntdefFacGaussDon"_TailFacAcc_$"IntdefFacTailAcc"_ \
TailFacDon_$"IntdefFacTailDon"_fit.log

#up sweep
solve vstep=0.2 vfinal=15 name=gate
#down sweep
solve vstep=-0.2 vfinal=-5 name=gate

save outf=transfer_VG15V.str
log off
MODELS PRINT

quit
```

-End of code

List of Figures

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List of publications

- Journal: J. Vac. Sci. Technol. A, 38:043204, 2020. .
  K. Dannecker and J. Baringhaus.
  Fabrication of crystal plane oriented trenches in gallium nitride using SF6 + Ar dry etching and wet etching post-treatment
- Journal: J. Vac. Sci. Technol. B, 39(1):012201, 2021. doi:10.1116/6.0000440.
  K. Dannecker and J. Baringhaus.
  Gate engineering in metal insulator semiconductor capacitors on native gallium nitride substrates for applications with high lifetime requirements
- Journal: J. Vac. Sci. Technol. B, 39(3):032204, 2021. doi:10.1116/6.0000980.
  K. Dannecker and J. Baringhaus.
  Fully vertical gallium nitride trench MOSFETs fabricated with metal-free gate first process
- Journal: J. Comput. Electron. 20(5):1685-1693, 2021. doi:10.1007/s10825-021-01736-1.
  K. Dannecker and J. Baringhaus.
  Design and simulation of gallium nitride trench MOSFETs for applications with high lifetime demand
- Conference: MST Kongress, Berlin 2019.
  K. Dannecker and J. Baringhaus, C. Huber.
  Herstellung und Simulation von Gate-Trench-Komplexen in nativen Galliumnitrid-Substraten für Leistungs-Trench-MOSFETs mit Fokus auf der Verteilung des elektrischen Felds
- Conference: ISPlasma/IC-PLANTS, Nagoya (online) 2021.
  K. Dannecker and J. Baringhaus.
  Plasma induced damage on gallium nitride Ga-face surface

Bibliography

[1] Statistical review of world energy. Technical report, British Petroleum, 2020. URL: https://www.bp.com/en/global/corporate/energy-economics/statistical-review-of-world-energy.html.

[2] V. Smil. *Energy Transitions: Global and National Perspectives*. Praeger, 2 edition, 2016.

[3] H. Ritchie. Energy. *Our World in Data*, 2014. URL: https://ourworldindata.org/energy.

[4] A. Breitkopf. Weltweit erzeugte strommenge, 2019. URL: https://de.statista.com/statistik/daten/studie/166918/umfrage/stromerzeugung-weltweit-seit-1990/.

[5] Electricity production. Technical report, Enerdata, 2019. URL: https://yearbook.enerdata.net/electricity/world-electricity-production-statistics.html.

[6] World energy outlook 2019. Technical report, International Energy Agency, 2019. URL: https://www.iea.org/reports/global-ev-outlook-2020.

[7] Global EV outlook 2020. Technical report, International Energy Agency, 2020. URL: https://www.iea.org/reports/world-energy-outlook-2019.

[8] B. Baliga. *Gallium Nitride and Silicon Carbide Power Devices*. World Scientific, 2017. doi:10.1142/10027.

[9] T. Rodgers and J. Meindl. VMOS: high speed TTL compatible MOS logic. *IEEE J. Solid-State Circuits*, 9(5):239–250, 1974. doi:10.1109/JSSC.1974.1050509.

[10] N. Iwamuro and T. Laska. IGBT history, state-of-the-art, and future prospects. *IEEE Trans. Electron Devices*, 64(3):741–752, 2017. doi:10.1109/TED.2017.2654599.

[11] D. Kahng. *Silicon-Silicon Dioxide Surface Device*, pages 583–596. 1960. doi:10.1142/9789814503464_0076.

[12] B. Baliga. Enhancement- and depletion-mode vertical-channel m.o.s. gated thyristors. *Electron. Lett.*, 15:645–647(2), 1979. doi:10.1049/el:19790459.

[13] M. Nawaz. Predicting potential of 4H-SiC power devices over 10 kV. In *2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS)*, pages 1291–1296, 2013. doi:10.1109/PEDS.2013.6527218.

[14] J. Appels and H. Vaes. High voltage thin layer devices (RESURF devices). In *1979 International Electron Devices Meeting*. IRE, 1979. doi:10.1109/iedm.1979.189589.

[15] M. Sumitomo, J. Asai, H. Sakane, K. Arakawa, Y. Higuchi, and M. Matsui. Low loss IGBT with partially narrow mesa structure (PNM-IGBT). In *2012 24th International Symposium on Power Semiconductor Devices and ICs*, pages 17–20, 2012. doi:10.1109/ISPSD.2012.6229012.

[16] S. Balachandran, C. Li, P. Losee, I. Bhat, and T. Chow. 6 kV 4H-SiC BJTs with specific on-resistance below the unipolar limit using a selectively grown base contact process. In *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, pages 293–296, 2007. doi:10.1109/ISPSD.2007.4294990.

[17] M. Domeij, A. Konstantinov, A. Lindgren, C. Zaring, K. Gumaelius, and M. Reimark. Large area 1200 V SiC BJTs with β>100 and ρon<3 mωcm^2. In *Silicon Carbide and Related Materials 2011*, volume 717 of *Materials Science Forum*, pages 1123–1126. Trans Tech Publications Ltd, 2012. doi:10.4028/www.scientific.net/MSF.717-720.1123.

[18] Y. Tanaka, K. Yano, M. Okamoto, A. Takatsuka, K. Fukuda, M. Kasuga, K. Arai, and T. Yatsuo. Fabrication of 700v SiC-SIT with ultra-low on-resistance of 1.01mω-cm^2. *Mater. Sci. Forum*, 527-529:1219–1222, 2006. doi:10.4028/www.scientific.net/MSF.527-529.1219.

[19] P. Moens, F. Bogman, H. Ziad, H. De Vleeschouwer, J. Baele, M. Tack, G. Loechelt, G. Grivna, J. Parsey, Y. Wu, T. Quddus, and P. Zdebel. UltiMOS: A local charge-balanced trench-based 600 V super-junction device. In *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, pages 304–307, 2011. doi:10.1109/ISPSD.2011.5890851.

[20] J. Sakakibara, Y. Noda, T. Shibata, S. Nogami, T. Yamaoka, and H. Yamaguchi. 600 V-class super junction MOSFET with high aspect ratio p/n columns structure. In *2008 20th International Symposium on Power Semiconductor Devices and IC's*, pages 299–302, 2008. doi:10.1109/ISPSD.2008.4538958.

[21] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, and Y. Yokotsuji. High performance SiC trench devices with ultra-low ron. In *2011 International Electron Devices Meeting*, pages 26.5.1–26.5.3, 2011. doi:10.1109/IEDM.2011.6131619.

[22] A. Bolotnikov, P. Losee, K. Matocha, J. Glaser, J. Nasadoski, L. Wang, A. Elasser, S. Arthur, Z. Stum, P. Sandvik, Y. Sui, T. Johnson, J. Sabate, and L. Stevanovic. 3.3 kV SiC MOSFETs designed for low on-resistance and fast switching. In *2012 24th International Symposium on Power Semiconductor Devices and ICs*, pages 389–392, 2012. doi:10.1109/ISPSD.2012.6229103.

[23] R. Howell, S. Buchoff, S. Campen, T. McNutt, A. Ezisis, B. Nechay, C. Kirby, M. Sherwin, R. Clarke, and R. Singh. A 10-kv large-area 4H-SiC power DMOSFET with stable subthreshold behavior independent of temperature. *IEEE Trans. Electron Devices*, 55:1807 – 1815, 2008. doi:10.1109/TED.2008.928204.

[24] V. Veliadis, E. J. Stewart, H. Hearne, M. Snook, A. Lelis, and C. Scozzie. A 9 kV normally-on vertical-channel SiC JFET for unipolar operation. *IEEE Electron Device Lett.*, 31(5):470–472, 2010. doi:10.1109/LED.2010.2042030.

[25] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa. Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV. *Appl. Phys Express*, 7(2):021002, 2014. doi:10.7567/apex.7.021002.

[26] M. Sun, Y. Zhang, X. Gao, and T. Palacios. High-performance GaN vertical fin power transistors on bulk GaN substrates. *IEEE Electron Device Lett.*, 38(4):509–512, 2017. doi:10.1109/LED.2017.2670925.

[27] C. Gupta, C. Lund, S. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, and U. Mishra. In-situ oxide, GaN interlayer based vertical trench MOSFET (OG-FET) on bulk GaN substrates. *IEEE Electron Device Lett.*, 38:1–1, 2017. doi:10.1109/LED.2017.2649599.

[28] C. Liu, R. Khadar, and E. Matioli. GaN-on-Si quasi-vertical power MOSFETs. *IEEE Electron Device Lett.*, 39(1):71–74, 2018. doi:10.1109/LED.2017.2779445.

[29] C. Gupta, S. Chan, A. Agarwal, S. Keller, and U. Mishra. OG-FET: A high performance vertical GaN trench MOSFET; targeted towards highly efficient power conversion. 2017. URL: https://cast.ucmerced.edu/sites/cast.ucmerced.edu/files/public/documents/2017Posters/OG-FET.pdf.

[30] D. Ji, C. Gupta, S. Chan, A. Agarwal, W. Li, S. Keller, U. Mishra, and S. Chowdhury. Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices. In *2017 IEEE International Electron Devices Meeting (IEDM)*, pages 9.4.1–9.4.4, 2017. doi:10.1109/IEDM.2017.8268359.

[31] S. Sque. High-voltage GaN-HEMT devices, simulation and modelling. Conference tutorial, 2013. URL: https://www.stevesque.com/publications/Sque-GaN-ESSDERC-2013.pdf.

[32] A. Ben-Slimane and P. Chiu. GaN power 2021: Epitaxy, devices, applications & technology trends. Technical report, Yole Development, 2021.

[33] P. Martínez, E. Maset, E. Sanchis-Kilders, V. Esteve, J. Jordán, J. Ejea, and A. Ferreres. Unstable behaviour of normally-off GaN E-HEMT under short-circuit. *Semicond. Sci. Technol.*, 33(4):045006, 2018. doi:10.1088/1361-6641/aab078.

[34] T. Kachi. GaN power devices for automotive applications. In *2007 IEEE Compound Semiconductor Integrated Circuits Symposium*, pages 1–4, 2007. doi:10.1109/CSICS07.2007.6.

[35] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda. Gate injection transistor (GIT) a normally-off AlGaN/-GaN power transistor using conductivity modulation. *IEEE Trans. Electron Devices*, 54(12):3393–3399, 2007. doi:10.1109/TED.2007.908601.

[36] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. Khan. The 1.6 kV AlGaN/GaN HFETs. *IEEE Electron Device Lett.*, 27(9):716–718, 2006. doi:10.1109/LED.2006.881084.

[37] Y. Dora, A. Chakraborty, L. Mccarthy, S. Keller, S. Denbaars, and U. Mishra. High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates. *IEEE Electron Device Lett.*, 27(9):713–715, 2006. doi:10.1109/LED.2006.881020.

[38] Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai, N. Batta, M. Li, T. Ueda, T. Tanaka, and D. Ueda. 8300 V blocking voltage AlGaN/GaN power HFET with thick poly-AlN passivation. In *2007 IEEE International Electron Devices Meeting*, pages 861–864, Dec 2007. doi:10.1109/IEDM.2007.4419085.

[39] D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda. 1.7 kV/1.0 mΩcm2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure. In *2016 IEEE International Electron Devices Meeting (IEDM)*, pages 10.1.1–10.1.4, 2016. doi:10.1109/IEDM.2016.7838385.

[40] D. Ji, A. Agarwal, H. Li, W. Li, S. Keller, and S. Chowdhury. 880v/2.7m$\omega \cdot$ cm 2 MIS gate trench CAVET on bulk GaN substrates. *IEEE Electron Device Lett.*, PP:1–1, 2018. doi:10.1109/LED.2018.2828844.

[41] S. Chowdhury, B. Swenson, and U. Mishra. Enhancement and depletion mode AlGaN/GaN CAVET with Mg-ion-implanted GaN as current blocking layer. *IEEE Electron Device Lett.*, 29(6):543–545, 2008. doi:10.1109/LED.2008.922982.

[42] M. Yoshino, Y. Ando, M. Deki, T. Toyabe, K. Kuriyama, Y. Honda, T. Nishimura, H. Amano, T. Kachi, and T. Nakamura. Fully ion implanted normally-off GaN

DMOSFETs with ALD-Al_2O_3 gate dielectrics. *Materials*, 12:689, 2019. doi:10.3390/ma12050689.

[43] R. Tanaka, S. Takashima, K. Ueno, H. Matsuyama, and M. Edo. Demonstration of 1200 V / 1.4 mΩ cm^2 vertical GaN planar MOSFET fabricated by an all ion implantation process. *Jpn J Appl Phys*, 2019. doi:10.7567/1347-4065/ab6347.

[44] A. Nakagawa. Theoretical investigation of silicon limit characteristics of IGBT. In *2006 IEEE International Symposium on Power Semiconductor Devices and IC's*, pages 1–4, 2006. doi:10.1109/ISPSD.2006.1666057.

[45] H. Otake, S. Egami, H. Ohta, Y. Nanishi, and H. Takasu. GaN-based trench gate metal oxide semiconductor field effect transistors with over 100 cm^2/(v s) channel mobility. *Jpn J Appl Phys*, 46(No. 25):L599–L601, 2007. doi:10.1143/jjap.46.l599.

[46] E. Treidel, O. Hilt, M. Wolf, L. Schellhase, A. Thies, and J. Würfl. Vertical GaN n-channel MISFETs on ammonothermal GaN substrate: Temperature dependent dynamic switching characteristics. *Mater. Sci. Semicond. Process.*, 91:146 – 150, 2019. doi:10.1016/j.mssp.2018.11.018.

[47] T. Oka, T. Ina, Y. Ueno, and J. Nishii. 100 A vertical GaN trench MOSFETs with a current distribution layer. In *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 303–306, 2019. doi:10.1109/ISPSD.2019.8757621.

[48] W. Li, K. Nomoto, K. Lee, S. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, and H. Xing. Development of GaN vertical trench-MOSFET with MBE regrown channel. *IEEE Trans. Electron Devices*, 65(6):2558–2564, 2018. doi:10.1109/TED.2018.2829125.

[49] R. Li, Y. Cao, M. Chen, and R. Chu. 600 v/ 1.7 Ω normally-off GaN vertical trench metal–oxide–semiconductor field-effect transistor. *IEEE Electron Device Lett.*, 37(11):1466–1469, 2016. doi:10.1109/LED.2016.2614515.

[50] C. Gupta, S. Chan, C. Lund, A. Agarwal, O. Koksaldi, J. Liu, Y. Enatsu, S. Keller, and U. Mishra. Comparing electrical performance of GaN trench-gate MOSFETs with a-plane $(11\bar{2}0)$ and m-plane $(1\bar{1}00)$ sidewall channels. *Appl. Phys Express*, 9(12):121001, 2016. doi:10.7567/apex.9.121001.

[51] K. Mukherjee, M. Borga, M. Ruzzarin, C. De Santi, S. Stoffels, S. You, K. Geens, H. Liang, S. Decoutere, G. Meneghesso, E. Zanoni, and M. Meneghini. Analysis of threshold voltage instabilities in semi-vertical GaN-on-Si FETs. *Appl. Phys Express*, 13(2):024004, 2020. doi:10.35848/1882-0786/ab6ddd.

[52] R. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli. Fully vertical GaN-on-Si power MOSFETs. *IEEE Electron Device Lett.*, 40(3):443–446, 2019. doi:10.1109/LED.2019.2894177.

[53] S. Nakamura, T. Mukai, and M. Senoh. Si- and Ge-doped GaN films grown with GaN buffer layers. *Jpn J Appl Phys*, 31(Part 1, No. 9A):2883–2888, 1992. doi:10.1143/jjap.31.2883.

[54] B. Monemar., P. Paskov, G. Pozina, C. Hemmingsson, J. Bergman, T. Kawashima, H. Amano, I. Akasaki, T. Paskova, S. Figge, D. Hommel, and A. Usui. Evidence for two Mg related acceptors in GaN. *Phys. Rev. Lett.*, 102:235501, 2009. doi:10.1103/PhysRevLett.102.235501.

[55] J. Lyons, A. Janotti, and C. Van de Walle. Shedding light on doping of gallium nitride. *SPIE Newsroom*, 2012. doi:10.1117/2.1201206.004302.

[56] S. Pearton, R. Shul, and F. Ren. A review of dry etching of GaN and related materials. *MRS Internet J. Nitride Semicond. Res.*, 5(1):e11, 2000. doi:10.1557/S1092578300000119.

[57] S. Pearton, E. Douglas, R. Shul, and F. Ren. Plasma etching of wide bandgap and ultrawide bandgap semiconductors. *J. Vac. Sci. Technol. A*, 38(2):020802, 2020. arXiv:https://doi.org/10.1116/1.5131343, doi:10.1116/1.5131343.

[58] Y. Zhang, M. Sun, Z. Liu, D. Piedra, J. Hu, X. Gao, and T. Palacios. Trench formation and corner rounding in vertical GaN power devices. *Appl. Phys. Lett.*, 110(19):193506, 2017. arXiv:https://doi.org/10.1063/1.4983558, doi:10.1063/1.4983558.

[59] S. Zhou, B. Cao, and S. Liu. Dry etching characteristics of GaN using Cl_2/BCl_3 inductively coupled plasmas. *Appl. Surf. Sci.*, 257(3):905 – 910, 2010. doi:10.1016/j.apsusc.2010.07.088.

[60] F. Horikiri, N. Fukuhara, H. Ohta, N. Asai, Y. Narita, T. Yoshida, T. Mishima, M. Toguchi, K. Miwa, and T. Sato. Simple wet-etching technology for GaN using an electrodeless photo-assisted electrochemical reaction with a luminous array film as the UV source. *Appl. Phys Express*, 12(3):031003, 2019. doi:10.7567/1882-0786/ab043c.

[61] F. Horikiri, H. Ohta, N. Asai, Y. Narita, T. Yoshida, and T. Mishima. Excellent potential of photo-electrochemical etching for fabricating high-aspect-ratio deep trenches in gallium nitride. *Appl. Phys Express*, 11(9):091001, 2018. doi:10.7567/apex.11.091001.

[62] T. Sreenidhi, K. Baskar, A. DasGupta, and N. DasGupta. Reactive ion etching of GaN in SF_6 + Ar and SF_6 + N_2 plasma. *Semicond. Sci. Technol.*, 23(12):125019, 2008. doi:10.1088/0268-1242/23/12/125019.

[63] D. Li, M. Sumiya, S. Fuke, D. Yang, D. Que, Y. Suzuki, and Y. Fukuda. Selective etching of GaN polar surface in potassium hydroxide solution studied by x-ray photoelectron spectroscopy. *J. Appl. Phys.*, 90(8):4219–4223, 2001. doi:10.1063/1.1402966.

[64] Y. Lai, S. Hsu, H. Chang, S. Wu, C: Chen, L. Chen, and Y. Cheng. The study of wet etching on GaN surface by potassium hydroxide solution. *Res. Chem. Intermed.*, 43(6):3563–3572, 2017. doi:10.1007/s11164-016-2430-1.

[65] J. He, M. Feng, Y. Zhong, J. Wang, R. Zhou, H. Gao, Y. Zhou, Q. Sun, J. Liu, Y. Huang, S. Zhang, H. Wang, M. Ikeda, and C. Yang. On-wafer fabrication of cavity mirrors for InGaN-based laser diode grown on Si. In *Scientific Reports*, 2018. doi:10.1038/s41598-018-26305-8.

[66] K. Mukherjee, C. De Santi, M. Borga, S. You, K. Geens, B. Bakeroot, S. Decoutere, G. Meneghesso, E. Zanoni, and M. Meneghini. Use of bilayer gate insulator in GaN-on-Si vertical trench MOSFETs: Impact on performance and reliability. *Materials*, 13(21), 2020. doi:10.3390/ma13214740.

[67] Y. Zhang, A. Dadgar, and T. Palacios. Gallium nitride vertical power devices on foreign substrates: a review and outlook. *J. Phys. D: Appl. Phys.*, 51(27):273001, 2018. doi:10.1088/1361-6463/aac8aa.

[68] P. Hofmann, C. Röder, F. Habel, G. Leibiger, F. Beyer, G. Gärtner, S. Eichler, and T. Mikolajick. Silicon doping of HVPE GaN bulk-crystals avoiding tensile strain generation. *J. Phys. D: Appl. Phys.*, 49(7):075502, 2016. doi:10.1088/0022-3727/49/7/075502.

[69] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios. Large-area 1.2 kV GaN vertical power FinFETs with a record switching figure of merit. *IEEE Electron Device Lett.*, 40(1):75–78, 2019. doi:10.1109/LED.2018.2880306.

[70] J. Meyer, R. Liu, R. Schaller, H-P. Lee, and C. Bayram. Systematic study of shockley-read-hall and radiative recombination in GaN on Al_2O_3, freestanding GaN, and GaN on Si. *Journal of Physics: Photonics*, 2(3):035003, 2020. doi:10.1088/2515-7647/ab9072.

[71] T. Kachi. Vertical GaN power devices: current status and future prospects (Conference Presentation). In H. Fujioka, H. Morkoç, and U. Schwarz, editors, *Gallium Nitride Materials and Devices XIV*, volume 10918. International Society for Optics and Photonics, SPIE, 2019. doi:10.1117/12.2509733.

[72] P. Pampili and P. Parbrook. Doping of iii-nitride materials. *Mater. Sci. Semicond. Process.*, 62, 2016. doi:10.1016/j.mssp.2016.11.006.

[73] W. Lee, N. Parmar, and J. Choi. High work function MoO_2 and ReO_2 contacts for p-type Si and GaN by a room-temperature non-vacuum process. *Mater. Sci. Semicond. Process.*, 71:374 – 377, 2017. doi:10.1016/j.mssp.2017.08.034.

[74] G. Greco, F. Iucolano, and F. Roccaforte. Ohmic contacts to gallium nitride materials. *Appl. Surf. Sci.*, 383:324 – 345, 2016. doi:10.1016/j.apsusc.2016.04.016.

[75] R. Williams, M. Darwish, R. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi. The trench power MOSFET: Part i history, technology, and prospects. *IEEE Trans. Electron Devices*, 64(3):674–691, 2017. doi:10.1109/TED.2017.2653239.

[76] Josef Lutz. *Halbleiter-Leistungsbauelemente*. Springer, Berlin, Heidelberg, 2 edition, 2012. doi:10.1007/978-3-642-29796-0.

[77] F. Roccaforte, G. Greco, and P. Fiorenza. Processing issues in SiC and GaN power devices technology: The cases of 4H-SiC planar MOSFET and recessed hybrid GaN MISHEMT. *2018 International Semiconductor Conference (CAS)*, 2018. doi:10.1109/smicnd.2018.8539756.

[78] Y. Zhang. *GaN-based Vertical Power Devices*. PhD thesis, Massachusetts institute of technology, 2017.

[79] T. Moustakas and J. Pankove. *Gallium Nitride (GaN) I*, volume 50. Academic Press, 1 edition, 1997.

[80] T. Chow. Wide bandgap semiconductor power devices for energy efficient systems. In *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 402–405, 2015. doi:10.1109/WiPDA.2015.7369328.

[81] J. Tsao, S. Chowdhury, M. Hollis, D. Jena, N. Johnson, K. Jones, R. Kaplar, S. Rajan, C. Van de Walle, E. Bellotti, C. Chua, R. Collazo, M. Coltrin andJ. Cooper, K. Evans, S. Graham, T. Grotjohn, E. Heller, M. Higashiwaki, M. Islam, P. Juodawlkis, M. Khan, A. Koehler, J. Leach, U. Mishra, R. Nemanich, R. Pilawa-Podgurski, J. Shealy, Z. Sitar, M. Tadjer, A. Witulski, M. Wraback, and J. Simmons. Ultrawide-bandgap semiconductors: Research opportunities and challenges. *Adv. Electron. Mater.*, 4(1):1600501, 2018. arXiv:https://onlinelibrary.wiley.com/doi/pdf/10.1002/aelm.201600501, doi:10.1002/aelm.201600501.

[82] T. Hashimoto, E. Letts, and S. Hoff. Current status and future prospects of ammonothermal bulk GaN growth. *Sens. Mater.*, 25:155–164, 2013. doi:10.18494/SAM.2013.853.

[83] Y. Mori, M. Imanishi, K. Murakami, and M. Yoshimura. Recent progress of Na-flux method for GaN crystal growth. *Jpn J Appl Phys*, 58(SC):SC0803, 2019. doi:10.7567/1347-4065/ab112e.

[84] B. Baliga. *Fundamentals of Power Semiconductor Devices*. Springer US, 2008. doi:10.1007/978-0-387-47314-7.

[85] D. Caughey and R. Thomas. Carrier mobilities in silicon empirically related to doping and field. *Proc. IEEE*, 55(12):2192–2193, 1967. doi:10.1109/PROC.1967.6123.

[86] W. Goetz, N. Johnson, C. Chen, H. Liu, C. Kuo, and W. Imler. Activation energies of Si donors in GaN. *Appl. Phys. Lett.*, 68(22):3144–3146, 1996. arXiv:https://doi.org/10.1063/1.115805, doi:10.1063/1.115805.

[87] S. Rokuno and J. Suda. Design guidelines suppressing dynamic punch-through in GaN vertical MOSFETs by considering the poole-frenkel effect. *Appl. Phys Express*, 14(2):024001, 2021. doi:10.35848/1882-0786/abd960.

[88] M. Lades, W. Kaindl, N. Kaminski, E. Niemann, and G. Wachutka. Dynamics of incomplete ionized dopants and their impact on 4H/6H-SiC devices. *IEEE Trans. Electron Devices*, 46(3):598–604, 1999. doi:10.1109/16.748884.

[89] E. Abbasi and A. Orouji. High-blocking-voltage UMOSFETs with reformed electric field distribution. *J. Comput. Electron.*, 17(4):1584–1595, 2018. doi:10.1007/s10825-018-1239-0.

[90] P. Kozodoy, H. Xing, S. Denbaars, U. Mishra, A. Saxler, R. Perrin, S. Elhamri, and W. Mitchel. Heavy doping effects in Mg-doped GaN. *J. Appl. Phys.*, 87:1832 – 1835, 2000. doi:10.1063/1.372098.

[91] T. Narita, N. Ikarashi, K. Tomita, K. Kataoka, and T. Kachi. Wide range doping control and defect characterization of GaN layers with various Mg concentrations. *J. Appl. Phys.*, 124(16):165706, 2018. doi:10.1063/1.5045257.

[92] T. Narita, H. Yoshida, K. Tomita, K. Kataoka, H. Sakurai, M. Horita, M. Bockowski, N. Ikarashi, J. Suda, T. Kachi, and Y. Tokuda. Progress on and challenges of p-type formation for GaN power devices. *J. Appl. Phys.*, 128(9):090901, 2020. arXiv:https://doi.org/10.1063/5.0022198, doi:10.1063/5.0022198.

[93] T. Narita, K. Tomita, K. Kataoka, Y. Tokuda, T. Kogiso, H. Yoshida, N. Ikarashi, K. Iwata, M. Nagao, N. Sawada, M. Horita, J. Suda, and T. Kachi. Overview of carrier compensation in GaN layers grown by MOVPE: toward the application of vertical power devices. *Jpn J Appl Phys*, 59(SA):SA0804, 2019. doi:10.7567/1347-4065/ab4610.

[94] Semiconductors on nsm. URL: http://www.ioffe.ru/SVA/NSM/Semicond/.

[95] Chapter 9 - scattering by impurities. In V. Gantmakher and Y. Levinson, editors, *Carrier Scattering in Metals and Semiconductors*, volume 19 of *Modern*

Problems in Condensed Matter Sciences, pages 215–240. Elsevier, 1987. doi:10.1016/B978-0-444-87025-4.50014-8.

[96] V. Uhnevionak, A. Burenkov, C. Strenger, G. Ortiz, E. Bedel-Pereira, V. Mortet, F. Cristiano, A. Bauer, and P. Pichler. Comprehensive study of the electron scattering mechanisms in 4H-SiC MOSFETs. *IEEE Trans. Electron Devices*, 62(8):2562–2570, 2015. doi:10.1109/TED.2015.2447216.

[97] K. Nojiri. *Dry Etching Technology for Semiconductors*. Springer International Publishing, 1 edition, 2015. doi:10.1007/978-3-319-10295-5.

[98] S. Franssila. *Introduction to Microfabrication*. John Wiley & Sons, Ltd, 2 edition, 2010. doi:10.1002/9781119990413.

[99] M. Devre. Advances in GaN dry etching process capabilities. 2004. URL: https://www.semanticscholar.org/paper/Advances-in-GaN-Dry-Etching-Process-Capabilities-Devre/cebcf959ac40abb75687c819434f5a836f6dfdaf.

[100] S. Pearton, R. Cammy, and R. Fan. *Gallium Nitride Processing for Electronics, Sensors and Spintronics*. Springer-Verlag London, 2006. doi:10.1007/1-84628-359-0.

[101] M. Sato and Y. Arita. Control of etching-product-dependent shape and selectivity in gate polysilicon reactive ion etching. *J. Vac. Sci. Technol. B*, 16(3):1038–1042, 1998. doi:10.1116/1.590064.

[102] R. Tauber S. Wolf. *Silicon Processing for the Vlsi Era: Process Technology*. Lattice Press, 1st edition, 2015.

[103] C. Vartuli S. Pearton C. Abernathy J. MacKenzie F. Ren J. Zolper H. Cho, D. Hays. Wet chemical etching survey of III-nitrides. *MRS Proceedings*, 483:265, 1997. doi:10.1557/PROC-483-265.

[104] D. Zhuang and J. Edgar. Wet etching of GaN, AlN, and SiC: a review. *Mater. Sci. Eng. R Rep.*, 48(1):1 – 46, 2005. doi:10.1016/j.mser.2004.11.002.

[105] Y. Jung, S. Jang, K. Baik, H. Kim, and J. Kim. Chemical etching behavior of non-polar GaN sidewalls. *J. Cryst. Growth*, 456:108 – 112, 2016. Proceeding of the 9th International Workshop on Bulk Nitride Semiconductors. doi:10.1016/j.jcrysgro.2016.08.039.

[106] S. Sze and K. Ng. *Physics of Semiconductor Devices*. John Wiley & Sons, Ltd, 2006. doi:10.1002/9780470068328.

[107] N. Truyen, N. Taoka, A. Ohta, K. Makihara, H. Yamada, T. Takahashi, M. Ikeda, M. Shimizu, and S. Miyazaki. High thermal stability of abrupt SiO_2/GaN interface

with low interface state density. *Jpn J Appl Phys*, 57(4S):04FG11, 2018. doi:10.7567/jjap.57.04fg11.

[108] A. Pérez-Tomás, P. Brosselard, P. Godignon, J. Millán, N. Mestres, M. Jennings, J. Covington, and P. Mawby. Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors. *J. Appl. Phys.*, 100(11):114508, 2006. arXiv:https://aip.scitation.org/doi/pdf/10.1063/1.2395597, doi:10.1063/1.2395597.

[109] A. Ortiz-Conde, F. Garcia Sanchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.*, 42(4):583 – 596, 2002. doi:10.1016/S0026-2714(02)00027-6.

[110] E. Lim and R. Ismail. Conduction mechanism of valence change resistive switching memory: A survey. *Electronics*, 4:586–613, 2015. doi:10.3390/electronics4030586.

[111] F. Chiu. A review on conduction mechanisms in dielectric films. *Adv. Mater. Sci. Eng.*, 2014:1–18, 2014. doi:10.1155/2014/578168.

[112] R. Perera, A. Ikeda, R. Hattori, and Y. Kuroki. Trap assisted leakage current conduction in thin silicon oxynitride films grown by rapid thermal oxidation combined microwave excited plasma nitridation. *Microelectron. Eng.*, 65(4):357 – 370, 2003. doi:10.1016/S0167-9317(02)01025-0.

[113] D. Schroder. *Semiconductor Material and Device Characterization*. John Wiley & Sons, Ltd, 2005. doi:10.1002/0471749095.

[114] K. Dannecker and J. Baringhaus. Fabrication of crystal plane oriented trenches in gallium nitride using SF_6 + Ar dry etching and wet etching post-treatment. *J. Vac. Sci. Technol. A*, 38:043204, 2020. doi:10.1116/6.0000120.

[115] M. Watanabe, D. Shaw, and G. Collins. Reduction of microtrenching and island formation in oxide plasma etching by employing electron beam charge neutralization. *Appl. Phys. Lett.*, 79, 2001. doi:10.1063/1.1413726.

[116] R. Hoekstra, M. Kushner, V. Sukharev, and P. Schoenborn. Microtrenching resulting from specular reflection during chlorine etching of silicon. *J. Vac. Sci. Technol. B*, 16:2102, 1998. doi:10.1116/1.590135.

[117] D. Kunder and E. Bär. Comparison of different methods for simulating the effect of specular ion reflection on microtrenching during dry etching of polysilicon. *Microelectron. Eng.*, 85(5):992 – 995, 2008. Proceedings of the Micro- and Nano-Engineering 2007 Conference. doi:10.1016/j.mee.2008.01.038.

[118] D. Ruixue, Y. Yintang, and H. Ru. Microtrenching effect of SiC ICP etching in SF_6/O_2 plasma. *J. Semicond.*, 30(1):016001, 2009. doi:10.1088/1674-4926/30/1/016001.

[119] K. Dannecker and J. Baringhaus. Fully vertical gallium nitride trench MOSFETs fabricated with metal-free gate first process. *J. Vac. Sci. Technol. B*, 39(3):032204, 2021. doi:10.1116/6.0000980.

[120] K. Dannecker and J. Baringhaus. Gate engineering in metal insulator semiconductor capacitors on native gallium nitride substrates for applications with high lifetime requirements. *J. Vac. Sci. Technol. B*, 39(1):012201, 2021. doi:10.1116/6.0000440.

[121] J. Robertson and B. Falabretti. Band offsets of high k gate oxides on III-V semiconductors. *J. Appl. Phys.*, 100(1):014111, 2006. URL: https://doi.org/10.1063/1.2213170, arXiv:https://doi.org/10.1063/1.2213170, doi:10.1063/1.2213170.

[122] D. Gaskill, C. Brandt, and R. Nemanich, editors. *III-Nitride, SiC, and Diamond Materials for Electronic Devices*, volume 423. Material Research Society Symposium Proceedings, 1996.

[123] D. Bisi, S. Chan, X. Liu, R. Yeluri, S. Keller, M. Meneghini, G. Meneghesso, E. Zanoni, and U. Mishra. On trapping mechanisms at oxide-traps in Al_2O_3/GaN metal-oxide-semiconductor capacitors. *Appl. Phys. Lett.*, 108(11):112104, 2016. arXiv:https://doi.org/10.1063/1.4944466, doi:10.1063/1.4944466.

[124] Z. Yatabe, Y. Hori, W. Ma, J. Asubar, M. Akazawa, T. Sato, and T. Hashizume. Characterization of electronic states at insulator/AlGaN interfaces for improved insulated gate and surface passivation structures of GaN-based transistors. *Japanese Journal of Applied Physics*, 53(10):100213, sep 2014. URL: https://doi.org/10.7567%2Fjjap.53.100213, doi:10.7567/jjap.53.100213.

[125] J. Pushkar and E. Rymaszewski. Embedded thin film capacitors - theoretical limits. *Advanced Packaging, IEEE Transactions on*, 25:454 – 458, 09 2002. doi:10.1109/TADVP.2002.806800.

[126] S. Habermehl, R. Apodaca, and R. Kaplar. On dielectric breakdown in silicon-rich silicon nitride thin films. *Appl. Phys. Lett.*, 94(1):012905, 2009. doi:10.1063/1.3065477.

[127] K. Ito, D. Kikuta, T. Narita, K. Kataoka, N. Isomura, K. Kitazumi, and T. Mori. Band offset of al1-xSixOymixed oxide on GaN evaluated by hard x-ray photoelectron spectroscopy. *Japanese Journal of Applied Physics*, 56(4S):04CG07, mar 2017. URL: https://doi.org/10.7567%2Fjjap.56.04cg07, doi:10.7567/jjap.56.04cg07.

[128] Y. Hori, C. Mizue, and T. Hashizume. Process conditions for improvement of electrical properties of Al_2O_3/n-GaN structures prepared by atomic layer deposition. *Jpn J Appl Phys*, 49(8):080201, 2010. doi:10.1143/jjap.49.080201.

[129] S. Jauss, S. Schwaiger, W. Daves, and O. Ambacher. Poly-silicon CMOS compatible gate module for AlGaN/GaN-on-silicon MIS-HEMTs for power electronics applications. In *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 83–86, 2016. doi:10.1109/ISPSD.2016.7520783.

[130] Y. Hironori, N. Takashi, and . Tsunenobu. Generation of very fast states by nitridation of the SiO2/SiC interface. *Journal of Applied Physics*, 112(2):024520, 2012. doi:10.1063/1.4740068.

[131] S. Dhar, S. Pantelides, L. Feldman, S. Wang, T. Isaacs-Smith, and J. Williams. Interface passivation of silicon dioxide layers on silicon carbide. In *2005 International Semiconductor Device Research Symposium*, pages 236–237, 2005. doi:10.1109/ISDRS.2005.1596071.

[132] G. Chung, C. Tin, J. Williams, K. McDonald, R. Chanana, R. Weller, S. Pantelides, L. Feldman, O. Holland, M. Das, and J. Palmour. Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide. *IEEE Electron Device Letters*, 22(4):176–178, 2001. doi:10.1109/55.915604.

[133] H. Schmidt, M. Gupta, and M. Bruns. Nitrogen diffusion in amorphous silicon nitride isotope multilayers probed by neutron reflectometry. *Phys. Rev. Lett.*, 96:055901, 2006. doi:10.1103/PhysRevLett.96.055901.

[134] K. Kajihara, M. Hirano, Y. Takimoto, L. Skuja, and H. Hosono. Diffusion of nitrogen molecules in amorphous SiO_2. *Appl. Phys. Lett.*, 91(7):071904, 2007. arXiv:https://doi.org/10.1063/1.2770796, doi:10.1063/1.2770796.

[135] D. Koenig, M. Rennau, and M. Henker. Direct tunneling effective mass of electrons determined by intrinsic charge-up process. *Solid-State Electron.*, 51:650–654, 2007. doi:10.1016/j.sse.2007.03.009.

[136] T. Narita, K. Tomita, S. Yamada, and T. Kachi. Quantitative investigation of the lateral diffusion of hydrogen in p-type GaN layers having NPN structures. *Appl. Phys Express*, 12(1):011006, 2018. doi:10.7567/1882-0786/aaf418.

[137] A. Pérez-Tomás, M. Placidi, X. Perpiñà, A. Constant, P. Godignon, X. Jordà, P. Brosselard, and J. Millán. GaN metal-oxide-semiconductor field-effect transistor inversion channel mobility modeling. *J. Appl. Phys.*, 105(11):114510, 2009. arXiv:https://doi.org/10.1063/1.3140614, doi:10.1063/1.3140614.

[138] R. Jakiela, A. Barcz, E. Dumiszewska, and A. Jagoda. Si diffusion in epitaxial GaN. *Phys. Status Solidi C*, 3(6):1416–1419, 2006. doi:10.1002/pssc.200565112.

[139] R. Czernecki, E. Grzanka, R. Jakiela, S. Grzanka, C. Skierbiszewski, H. Turski, P. Perlin, T. Suski, K. Donimirski, and M. Leszczynski. Hydrogen diffusion in GaN:Mg and GaN:Si. *J. Alloys Compd.*, 747:354 – 358, 2018. doi:10.1016/j.jallcom.2018.02.270.

[140] H. Azusa, E. Katsuyoshi, H. Ken, and D. Hiroshi. Surface treatments toward obtaining clean GaN(0001) from commercial hydride vapor phase epitaxy and metal-organic chemical vapor deposition substrates in ultrahigh vacuum. *Appl. Surf. Sci.*, 256(14):4745–4756, 2010. doi:10.1016/j.apsusc.2010.03.001.

[141] K. Ito, K. Tomita, D. Kikuta, M. Horita, and T. Narita. Analysis of channel mobility in GaN-based metal-oxide-semiconductor field-effect transistors. *Journal of Applied Physics*, 129(8):084502, 2021. arXiv:https://doi.org/10.1063/5.0040700, doi:10.1063/5.0040700.

[142] E. Treidel, O. Hilt, V. Hoffmann, F. Brunner, N. Bickel, A. Thies, K. Tetzner, H. Gargouri, C. Huber, K. Donimirski, and J. Würfl. On the conduction properties of vertical GaN n-channel trench MISFETs. *IEEE J. Electron Devices Soc.*, pages 1–1, 2021. doi:10.1109/JEDS.2021.3056697.

[143] C. Miskys, M. Kelly, O. Ambacher, and M. Stutzmann. Freestanding GaN-substrates and devices. *Phys. Status Solidi C*, 0:1627 – 1650, 2003. doi:10.1002/pssc.200303140.

[144] K. Dannecker and J. Baringhaus. Design and simulation of gallium nitride trench MOSFETs for applications with high lifetime demand. *J. Comput. Electron.*, 20(5):1685–1693, July 2021. doi:10.1007/s10825-021-01736-1.

[145] A. Castiglia, J. Carlin, and N. Grandjean. Role of stable and metastable Mg-H complexes in p-type GaN for cw blue laser diodes. *Appl. Phys. Lett.*, 98(21):213505, 2011. arXiv:https://doi.org/10.1063/1.3593964, doi:10.1063/1.3593964.

[146] L. Romano, M. Kneissl, J. Northrup, C. Van de Walle, and D. Treat. Influence of microstructure on the carrier concentration of Mg-doped GaN films. *Appl. Phys. Lett.*, 79(17):2734–2736, 2001. arXiv:https://doi.org/10.1063/1.1413222, doi:10.1063/1.1413222.

[147] U. Kaufmann, P. Schlotter, H. Obloh, K. Köhler, and M. Maier. Hole conductivity and compensation in epitaxial GaN:Mg layers. *Phys. Rev. B*, 62:10867–10872, 2000. doi:10.1103/PhysRevB.62.10867.

[148] H. Obloh, K. Bachem, U. Kaufmann, M. Kunzer, M. Maier, A. Ramakrishnan, and P. Schlotter. Self-compensation in Mg doped p-type GaN grown by MOCVD. *J. Cryst. Growth*, 195(1):270 – 273, 1998. doi:10.1016/S0022-0248(98)00578-8.

[149] A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán. A field-effect electron mobility model for SiC MOSFETs including high density of traps at the interface. *Microelectron. Eng.*, 83(3):440 – 445, 2006. doi:10.1016/j.mee.2005.11.007.

[150] P. Fiorenza, G. Greco, F. Iucolano, A. Patti, and F. Roccaforte. Channel mobility in GaN hybrid MOS-HEMT using SiO_2 as gate insulator. *IEEE Trans. Electron Devices*, PP:1–7, 2017. doi:10.1109/TED.2017.2699786.

[151] A. Perez-Tomas, M. Placidi, N. Baron, S. Chenot, Y. Cordier, J. Moreno, J. Millan, and P. Godignon. 2DEG HEMT mobility vs inversion channel MOSFET mobility. *Mater. Sci. Forum*, 645-648:1207–1210, 2010. doi:10.4028/www.scientific.net/MSF.645-648.1207.

[152] F. Giessibl. Advances in atomic force microscopy. *Rev. Mod. Phys.*, 75:949–983, 2003. doi:10.1103/RevModPhys.75.949.

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Declaration of Academic Integrity

I hereby confirm, that this is my own work and that all content that was contributed by other persons than myself is labeled as such.

Renningen, ...

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