A contribution to turning-ON behavior of high voltage optically and electrically triggered thyristors

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A contribution to turning-ON behavior of high voltage optically and electrically triggered thyristors

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In summer, 2003; I worked with Dr. Franz-Josef Niedernostheide in the field of Light Triggered Thyristors at Infineon Tech. AG, Munich. This exposure to industrial problems in developing high power Light Triggered Thyristors helped me to engender an interesting mini-project and a master thesis on the latest problems of Light Triggered Thyristor development.

This successful cooperation with the colleagues of Infineon Tech. AG and the invaluable experience of Prof. Dieter Silber in the field of thyristors motivated me to continue my research in the field of high voltage bipolar power devices, a part of which is the basis of my present PhD thesis.

I would like to thank my ex-colleagues from Infineon Tech AG, Dr. Hans-Joachim Schulze, Dr. Franz-Josef Niedernostheide and Mr. Uwe Kellner Werdehausen for the financial support, many interesting and fruitful discussions and providing me with necessary simulation, measurement results. I would also like to thank my colleagues in University of Bremen, Mr. Saeed Milady, M.Sc, Mr. Uma Maheshwara Reddy, M.Sc and Ms. Salwa Basurra, M.Sc for helping in maintaining a friendly and healthy working atmosphere and countless discussions which were a significant part of our learning process.

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Contents

Contents

Contents

1 Introduction

Thyristors are electrical switches which turn-on by a trigger pulse. The turn-on trigger pulse can be either electrical (Electrical Triggered Thyristors, ETTs) or optical (Light Triggered Thyristors, LTTs). Thyristors can be turned-off by forced commutation (applying a negative voltage), by applying a negative gate current pulse (Gate Turn-off Thyristors, GTOs) or by applying a negative gate voltage pulse (MOS Controlled Thyristors, MCTs). The major focus of the present PhD thesis is limited to LTTs.

1.1 History of LTT development

Since the beginning of the thyristor era in HVDC in the 1960s a permanent improvement of the blocking and current conducting capability of these power semiconductors has taken place. While in the early years about 84.000 devices rated 1.5”/1.6kV would have been necessary to build a 3000MW system, today the same amount of power can be transmitted using only 3750 thyristors rated 5”/8kV. This remarkable reduction of the number of thyristors and their associated components led to a decrease of investment for a converter and to an increase of its reliability.

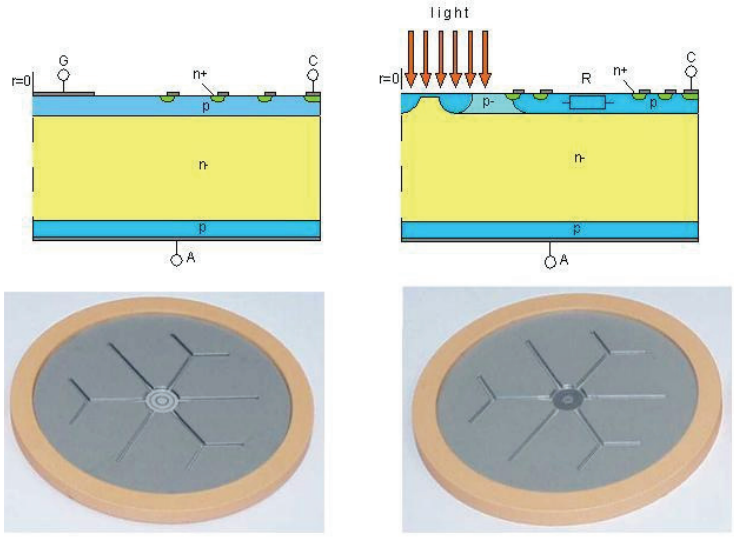
In parallel to this development there was a further step in innovation at the beginning of the 1980’s: the introduction of the direct-light-triggering of thyristors. It led to a significant reduction of the number of electronic parts necessary to trigger and to protect a thyristor and this caused a further increase of the converter’s reliability.

1.1.1 Principle of the direct-light-triggering

Because of the high voltage environment of thyristors in HVDC applications rated up to 500kV it is necessary to electrically separate the trigger unit at ground potential from the thyristor at high voltage potential. The trigger command for the thyristor is transmitted as a light pulse via a fiber optic cable even if ETTs are used. Therefore the possibility to directly trigger the thyristor with the help of a light pulse was early thought about. A conversion of the low power light pulse into a high power electrical gate pulse by a printed circuit board at thyristor potential, that is necessary when using an ETT, could then be avoided.

The amount of light needed to trigger a LTT is about 1000 times higher than the amount of light to transmit the trigger command to the printed circuit board associated to an ETT. Although the principle of triggering a thyristor directly by light has been known for more than 30 years, LTT application in HVDC was feasible only since sufficiently powerful and reliable light sources and optical components with low damping characteristics were commercially available. Note that the electrical power required to trigger an ETT is again about 1000 times higher than

what an LTT requires. Nevertheless, in early 1980s high power light sources became industrially available with the emergence of high power LASERs.



(a) (b)

Figure 1 Industrially available thyristor prototypes and their schematics

(a) ETT (b) LTT

1.2 Selection of optical parameters for optical trigger pulse

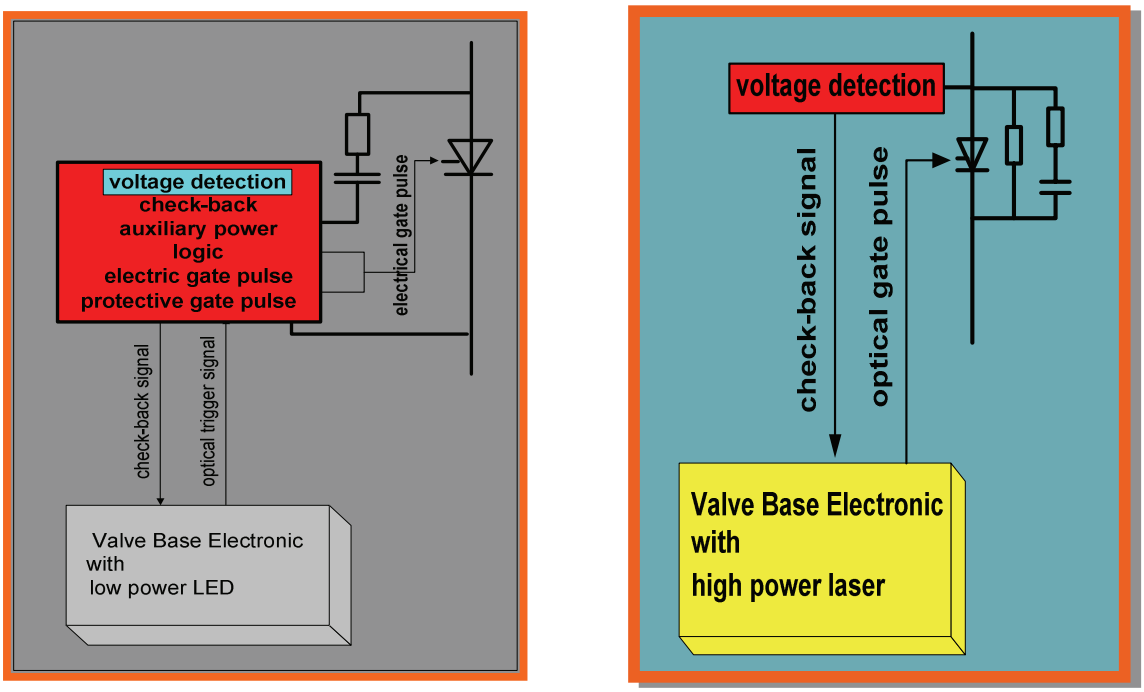
In the state-of-the-art LTTs, a high power light (in the order of tens of mWatt) is shined in the optical window by a LASER beam generator. 40mW is chosen to be the trigger pulse power since it is the optimum compromise between light-power (cost) and trigger sensitivity at typical industrial triggering voltages (Figure 3). The optimum light power for LTT triggering (the best compromise between light power and trigger delay) doesn't deviate significantly from 40mW for triggering voltages above 500V.

The wavelength of the shined light has to be less than or equal to 1040nm for the carriers to transit from Valence Band (VB) to Conduction Band (CB) of Silicon, i.e. to across the forbidden energy gap of Si (1.2eV). 970nm wave length of the light is chosen due to the highest relative optical absorption coefficient which in other words: an efficient use of light power to reduce the trigger delay of the thyristor (Figure 3).

1.3 Why LTTs over ETTs

Electrically Triggered Thyristors (ETTs) (Figure 1(a)) were the first thyristors ever to be developed. Basically they are equipped with an electrical gate circuit which sends electrical trigger pulses according to optical commands it receives from an intelligent (programmed) Valve Base Electronic (VBE) system. The electrical ground of the gate circuit and the electrical ground of the power circuit in which the load current flows have to be galvanically isolated to avoid undesired triggering pulses at thyristor level (Figure 2 (a)).

Light Triggered Thyristors (LTTs) (Figure 1(b)), ideally, provide a perfect isolation between the power and control circuits of a thyristor since the trigger pulses of LTTs are high power light pulses generated by LASERs and transmitted via optical fibers (Figure 2 (b)). This feature makes them very attractive in high and medium power applications especially from the application engineer's point of view. Typical application areas of LTTs are HVDC power transmission systems and electrical systems for improving the power factor in power distribution networks.



(a) (b)

Figure 2 Thyristor triggering and monitoring

(a) ETT approach (b) LTT approach

1.3.1 Advantages offered by LTTs over ETTs

- Number of electrical components in the valves reduces substantially, static failure rate is reduced, eliminates possibility of Electro-Magnetic Interference (EMI), providing inherently higher reliability.
- Firing pulses available independent of AC system voltage, no auxiliary energy required within the valve.
- Eliminates a potential source of Partial Discharge (PD), providing inherently longer life.

1.4 Major challenges in LTTs

To exploit the availability of optical trigger power, the developers of LTTs from the previous and the current decade focus on integrating safety measures against critical fault triggering scenarios in thyristors, viz. break over triggering, high di/dt triggering, fault dv/dt triggering, reapplied dv/dt triggering and thus reduce the control electronics necessary to protect the thyristor. The fault triggering scenarios in a thyristor operation are described in detail in section 1.5

The major focus of the present work is to integrate necessary and sufficient protection measures against all possible fault triggering mechanisms in LTTs and thus provide a dependable alternative to ETTs in industrial high power switching applications.

To start with, all the possible fault triggering scenarios in an LTT operation, which are mentioned above, are also present in an ETT operation. The disparity however is, in power systems equipped with ETTs, external intelligent control blocks are allowed which monitor the status of each ETT continuously and send a trigger pulse when the conditions for a fault triggering scenario are fulfilled, thereby protecting the thyristors and the power system from any possible damage. In case of LTTs, the boasted simplicity in regard to control circuitry doesn't allow a complex external intelligent control block. Hence, all the safety measures must be integrated physically within the thyristor.

A necessary condition to be fulfilled in LTTs to be protected against any fault triggering is that the AG1 of the thyristor is to be triggered first and thus the power load is distributed across all the AGs. Fulfillment of this condition avoids current filamentation and a possible thermal runaway.

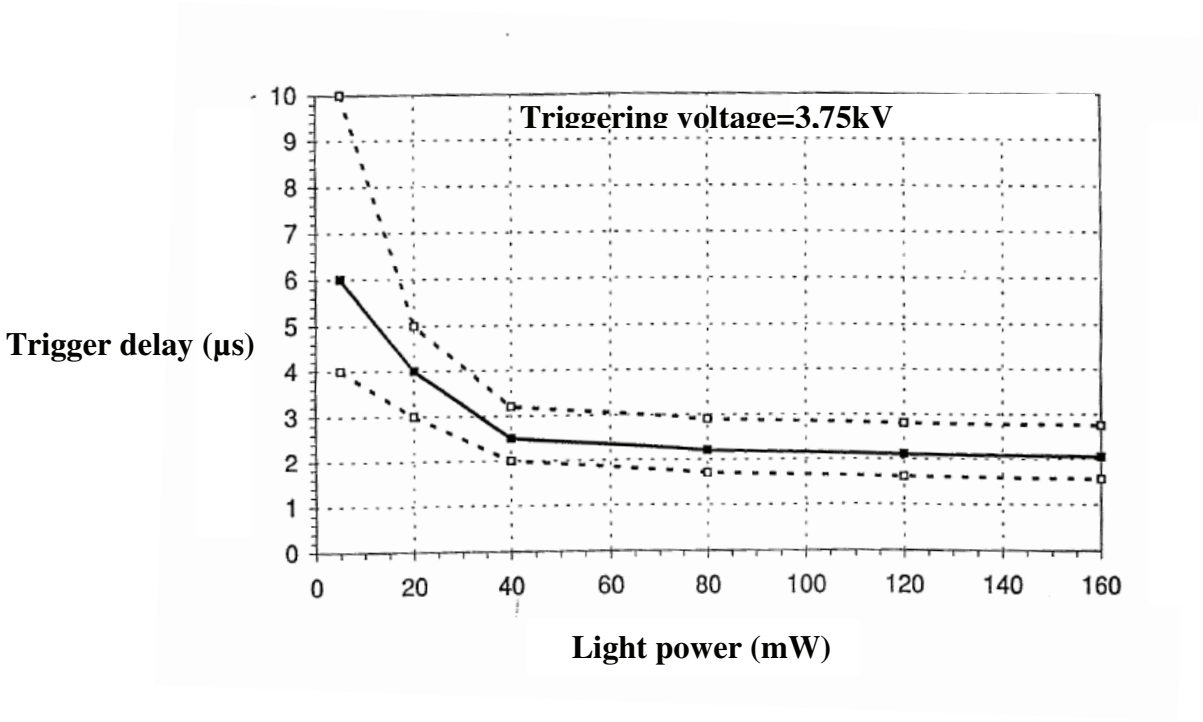


Figure 3 Trigger delay Trigger vs. light power at trigger voltage=3.75kV for 3 different thyristor samples

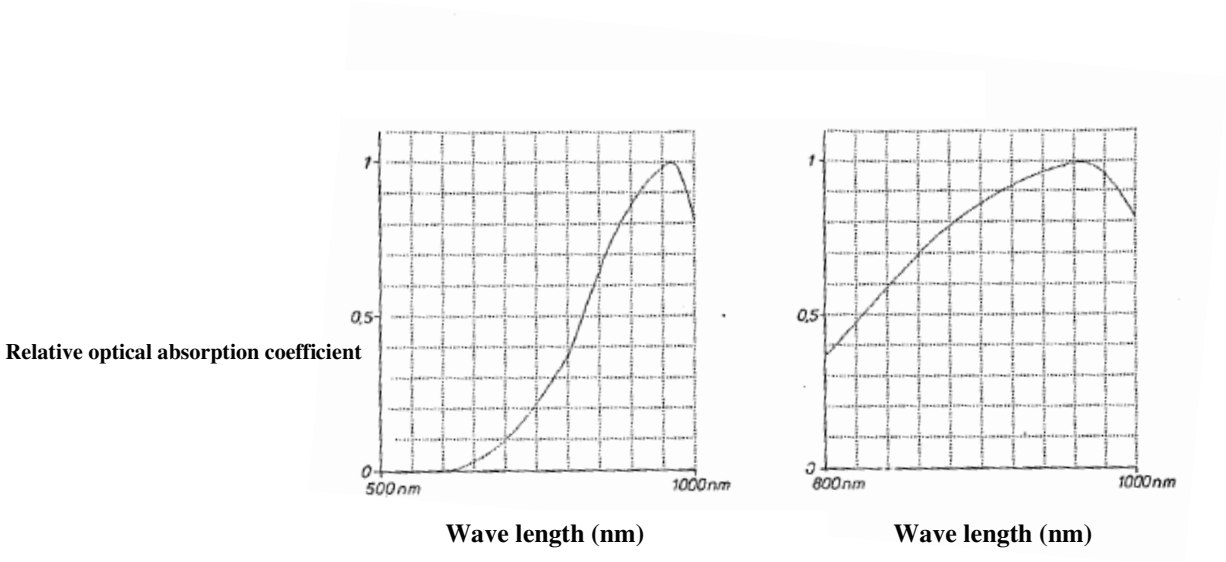


Figure 4 Relative optical absorption coefficient vs. Wave length

1.5 Description of the typical fault triggering scenarios in thyristors

1.5.1 Break-over triggering

When the forward voltage across the thyristor exceeds the forward break-over voltage of the thyristor, which is determined either by avalanche breakdown or punch through, thyristor goes into conduction at one or several different regions leading to a non-homogeneous current density distribution and consequently high temperature spots in the thyristor. Such an event is called Break-over triggering. Break-over triggering is the toughest fault triggering scenario for the thyristor due to maximum power dissipation in the thyristor.

The problem of break over triggering is already solved during the last decade with the introduction of a parallel avalanche diode or a Break Over Diode (BOD) to the thyristor. The breakdown voltage of the BOD is tailored lower than that of the forward breakdown voltage of the thyristor which means that the forward breakdown always occurs in the BOD. LTTs with integrated BODs are commercially available since last decade.

1.5.2 High di/dt triggering

In an LTT where the outer AGs are not fast enough in triggering and thus sharing the load, a local high current density may inflict the inner AGs region. Such a condition can lead to localized damage of the thyristor in the inner AG region. Therefore, much care has to be taken in selecting the maximum allowed di/dt in a thyristor, which is controlled mainly by the converter transformer's inductivity of a thyristor valve, not to overload the inner AG region.

Let us assume that in Figure 5, current is commutated from V1 to V3, and then di/dt in the loop marked with red in Figure 5 is

Equation 1.1
$$\frac{di}{dt} = \frac{V1 - V2}{L_{CT1} + L_{CT2} + L_{V1} + L_{V3}}$$

Where,

- L_{CT1}, L_{CT2} are inductive components of phase1 and 2 respectively of the current transformer.
- L_{V1}, L_{V3} are valve inductances of Valve1 and Valve 3 respectively to reduce the ripple factor.

As $L_{CT1}+ L_{CT2}$ is much higher in value compared to $L_{V1}+ L_{V3}$, Equation 1.1 can be reduced to,

Equation 1.2
$$\frac{di}{dt} = \frac{V1 - V2}{L_{CT1} + L_{CT2}}$$

LTTs from the Infineon Tech AG use the area of the integrated protection resistor to provide the inner AGs with a larger area and thereby withstand higher di/dts. This topic is discussed in detail in chapter 4.

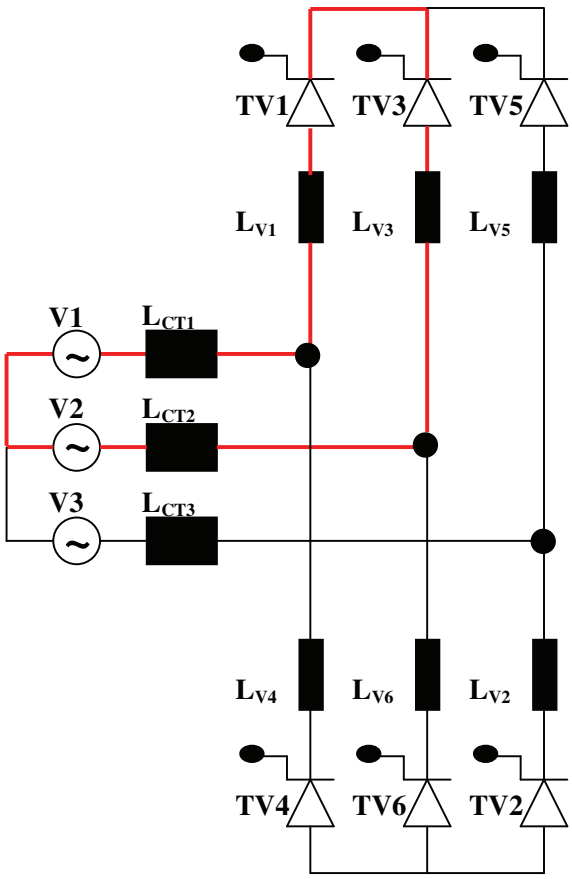


Figure 5 Equivalent circuit diagram of a 3-phase converter, current path during commutation between Thyristor Valves, TV1 and TV3

1.5.3 Fault dv/dt triggering

In a fault dv/dt triggering scenario, a forward dv/dt pulse appears across a thyristor in off-state (typically happens in AC converters) after plasma is either completely extracted or recombined in the thyristor (

Figure 6). This dv/dt pulse generates capacitive or, in other words, displacement current. In addition to this capacitive current, an amplified capacitive current by the PNP transistor in the thyristor also contributes to the total dv/dt current.

1.5.4 Fault reapplied dv/dt triggering

A fault re-applied dv/dt triggering scenario is basically just the same as a fault dv/dt triggering scenario except for the thyristor still contains rest plasma. That means, in

Figure 6, the recovery time $t_q<t_3$. If a dv/dt pulse appears across the thyristor before all the plasma from the thyristor is either extracted or recombined, then it is called a re-applied dv/dt pulse.

1.5.4.1 Present industrial method of overcoming fault reapplied dv/dt triggering

In the present commercially available LTT based power systems, each LTT is equipped with an electronic circuit board called Thyristor Voltage Monitor (TVM) built physically close to its respective LTT in the thyristor module (Figure 7 (b)) which monitors the voltage across its LTT continuously (Figure 7 (a)). When the LTT voltage, V_{AK} in

Figure 6 becomes zero, TVM sends a signal to Valve Base Electronic (VBE) which consequently sends a "Enable" signal to another electronic circuit board called Recovery Protection Unit (RPU) located in the thyristor module (Figure 7 (b)). The RPU is responsible for protecting the thyristor valve in case of a possible re-applied dv/dt scenario.

As it can be seen in Figure 7 (a), the RPU is connected in series to the grading capacitor, CG. The purpose of CG is three fold.

1. Avoiding voltage fluctuations across the thyristor valve
2. Power supply to the LASER diodes in the RPU
3. In case of a dangerously high positive dv/dt, CG produces current equal to CG*dv/dt which flows to and activates the RPU

The activated RPU sends an optical trigger pulse to Multimode Star Coupler (MSC) which distributes the trigger pulse from the RPU to all the LTTs in the thyristor valve and consequently trigger them and thus avoiding fault re-applied dv/dt triggering.

Integration of protection against fault reapplied dv/dt triggering and thereby avoiding the electronic circuit boards, TVM and RPU has been the most burning challenge for the LTT developers during the present decade. New concepts to integrate re-applied dv/dt triggering within the LTTs are discussed in Chapter 9

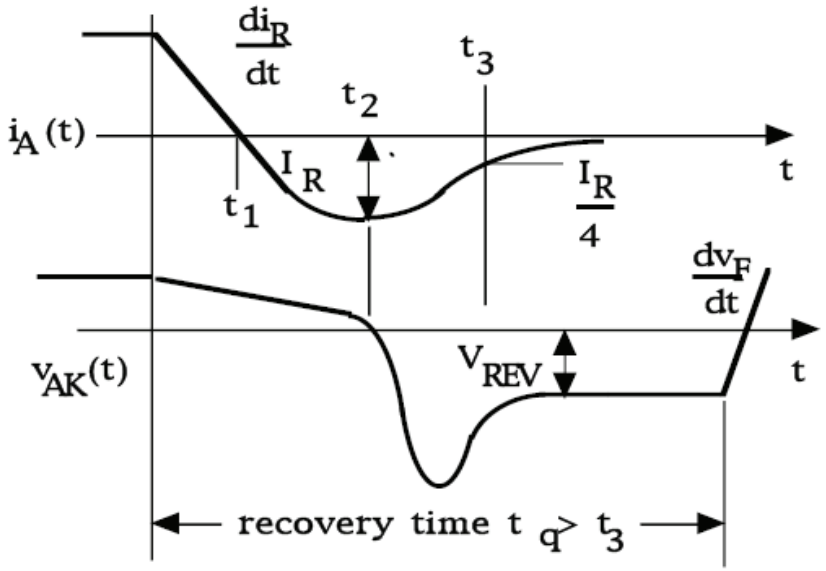
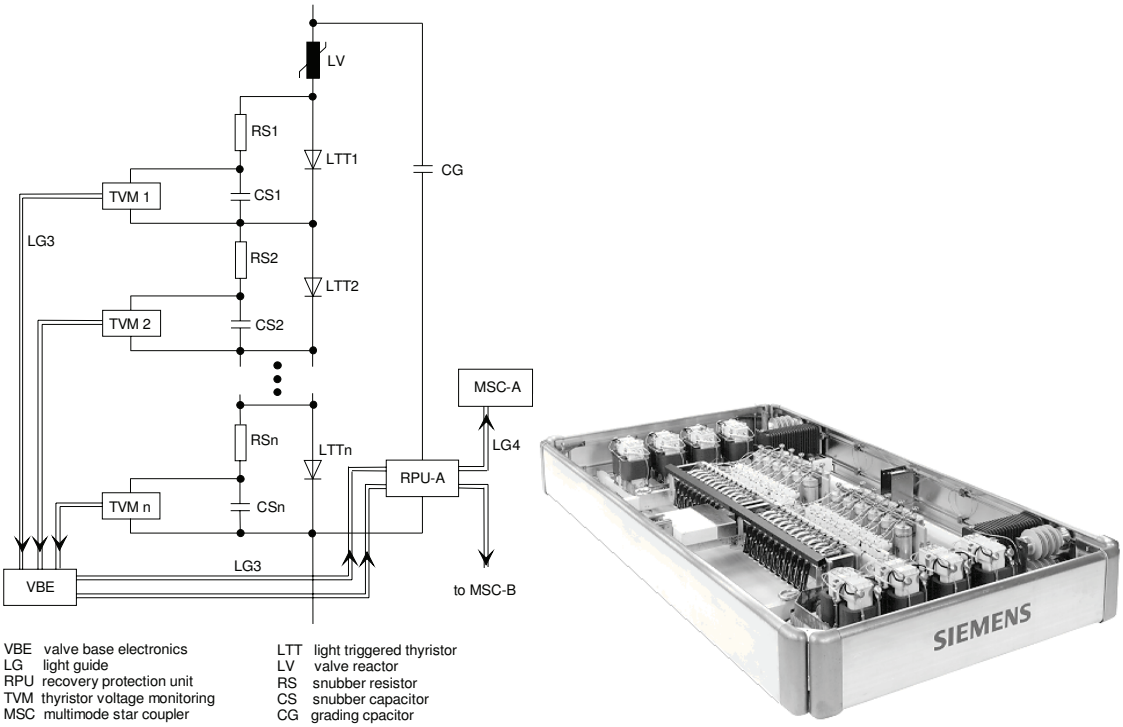


Figure 6 Thyristor turn-off process (Reference 16)



(a) **(b)**

Figure 7 (a) Principle circuit of a valve section (Reference 17)

(b) Thyristor module (Reference 17)

1.6 Tasks of the present PhD thesis:

1.6.1 Integrating safety measures in LTTs against fault triggering scenarios:

The contemporary developers of LTTs are working on integrating the safety measures against high di/dt triggering, fault dv/dt and re-applied dv/dt triggering.

In fault dv/dt triggering, a forward dv/dt pulse appears across a thyristor in off-state (typically happens in AC converters) and it is assumed that there is no rest plasma in the thyristor. This dv/dt pulse generates capacitive or displacement current. In addition to this capacitive current, an amplified capacitive current by the PNP transistor in the thyristor also contributes to the total dv/dt current. A fault re-applied dv/dt triggering scenario is basically just the same as fault dv/dt triggering scenario except for the thyristor still contains rest plasma. If a dv/dt pulse appears across the thyristor before all the plasma from the thyristor is either extracted or recombined, then it is called a re-applied dv/dt pulse.

Ensuring a safe re-applied dv/dt triggering is the most challenging task for the LTT-developers in the current decade.

1.6.2 Improving other LTT characteristics with the aim of reducing the cost for the customers

Increasing the blocking capability of a thyristor in forward and reverse blocking directions without considerably deteriorating its dynamic properties reduces the number of thyristors connected in series for a given power converter voltage rating. Less number of devices means reduction of size and most likely also cost for the customer.

My work at Institut für elektrische Antriebe, Leistungselektronik und Bauelemente, IALB, University of Bremen, Bremen is mainly focused on achieving the following objectives,

1. Investigating the behavior of LTTs for a better understanding of the operation. Especially the influence of mobile carriers on the dynamics of space charge region during triggering, amplification of currents by the PNP transistor action deserve a thorough investigation which has not yet been done.

2. Investigating the existing and new concepts to resolve the problems of integrating safety measures against high di/dt triggering, fault dv/dt and reapplied dv/dt triggering with the aid of simulations.

3. Investigating the concept of a Tandem device (asymmetrical thyristor in series with a diode) which can block symmetrically around 13kV with dynamic properties comparable to that of a symmetrical 8kV thyristor.

4. Furthermore, problems of simplifying the device structure which reduces the manufacturing price of the high voltage LTTs.

This work is supervised by Prof. Dieter Silber, IALB; University of Bremen who will also be my first supervisor in the examination for the title of a Ph.D.

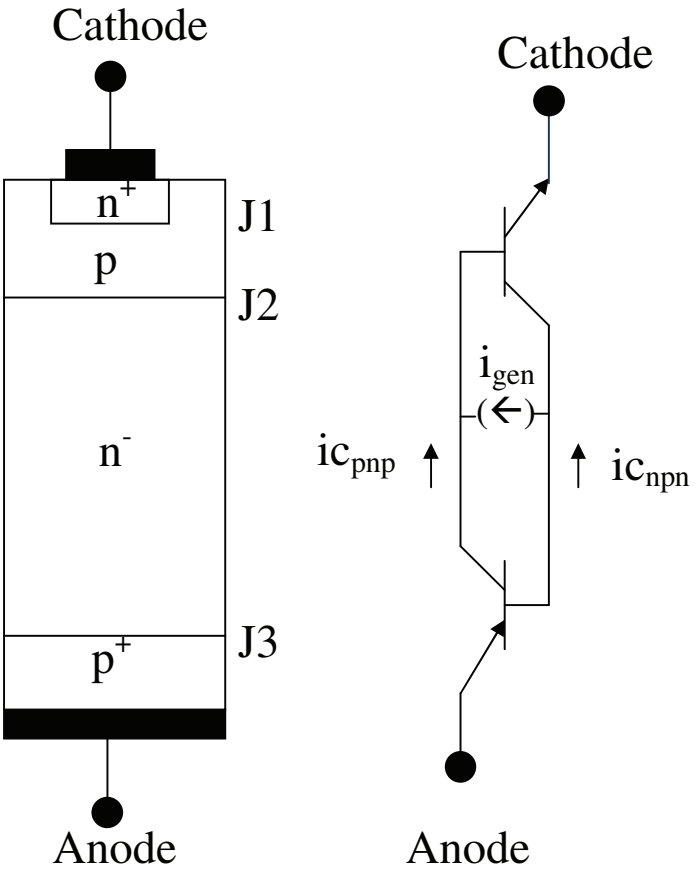
Infineon Tech. AG supported this project financially and also provided me with the necessary data and measurements for this project.

The topic of the work is chosen as “Turning-On behavior of high voltage optically and electrically triggered thyristors”.

2 Physics of thyristor operation

2.1 Thyristor 1D- model and the two-transistor equivalent circuit

In describing how the thyristor operates from a physical point of view, it is convenient to consider the device as an over simplified (without a cathode shunt) one-dimensional structure shown in Figure 8(a). An appropriate low-frequency equivalent circuit composed of a pnp and a npn transistor is shown in Figure 8(b), which is easily derived from the one-dimensional model.



(a) **(b)**

Figure 8 **(a) 1D thyristor model**

(b) Two-transistor equivalent circuit

2.2 Blocking states (forward and reverse)

To explain forward or reverse blocking, one shall consider a current generation source i_{gen} as shown in Figure 8(b).

Then,

Equation 2.1 $$ic_{npn} = (ic_{pnp} + i_{gen})\beta_{npn}$$

Equation 2.2 $$ic_{pnp} = (ic_{npn} + i_{gen})\beta_{pnp}$$

Equation 2.3 $$i_{cathode} = i_{anode} = ic_{npn} + ic_{pnp} + i_{gen}$$

Where,

ic – Collector current of the transistor

igen – Thermal generation current

β – Common emitter current gain of the transistor

Equation 2.4 $$\beta = \frac{\alpha}{1 - \alpha}$$

From 2.1 and 2.2,

Equation 2.5 $$ic_{npn} = \beta_{npn}((ic_{npn} + i_{gen})\beta_{pnp} + i_{gen})$$

Equation 2.6 $$ic_{npn}(1 - \beta_{npn}\beta_{pnp}) = \beta_{npn}(\beta_{pnp} + 1)i_{gen}$$

Equation 2.7 $$ic_{pnp}(1 - \beta_{npn}\beta_{pnp}) = \beta_{pnp}(\beta_{npn} + 1)i_{gen}$$

From 2.6 and 2.7,

Equation 2.8 $$ic_{npn} + ic_{pnp} = \frac{i_{gen}}{1 - \beta_{npn}\beta_{pnp}}(\beta_{npn}\beta_{pnp} + \beta_{npn} + \beta_{pnp})$$

Equation 2.9 $$i_{cathode} = i_{anode} = ic_{npn} + ic_{pnp} + i_{gen} = i_{gen}\left(\frac{1 + \beta_{npn} + \beta_{pnp}}{1 - \beta_{npn}\beta_{pnp}}\right) = i_{gen}\left(\frac{1 - \alpha_{npn}\alpha_{pnp}}{1 - \alpha_{npn} - \alpha_{pnp}}\right)$$

From 2.9, the condition for blocking is $\beta_{npn}\beta_{pnp} = \alpha_{npn} + \alpha_{pnp} < 1$. Therefore, the condition for blocking can be calculated using constant α and β if i_{gen} is included in the calculation of ic. If i_{gen} is not included in the calculation of ic, using constant α and β will result in an obvious current continuity equation.

2.3 Thyristor Turn-on process

2.3.1 Significance of differential common emitter current gain in considering thyristor turn-on process

Figure 9 shows a 1D model of thyristor (with a cathode shunt) during turn-on process.

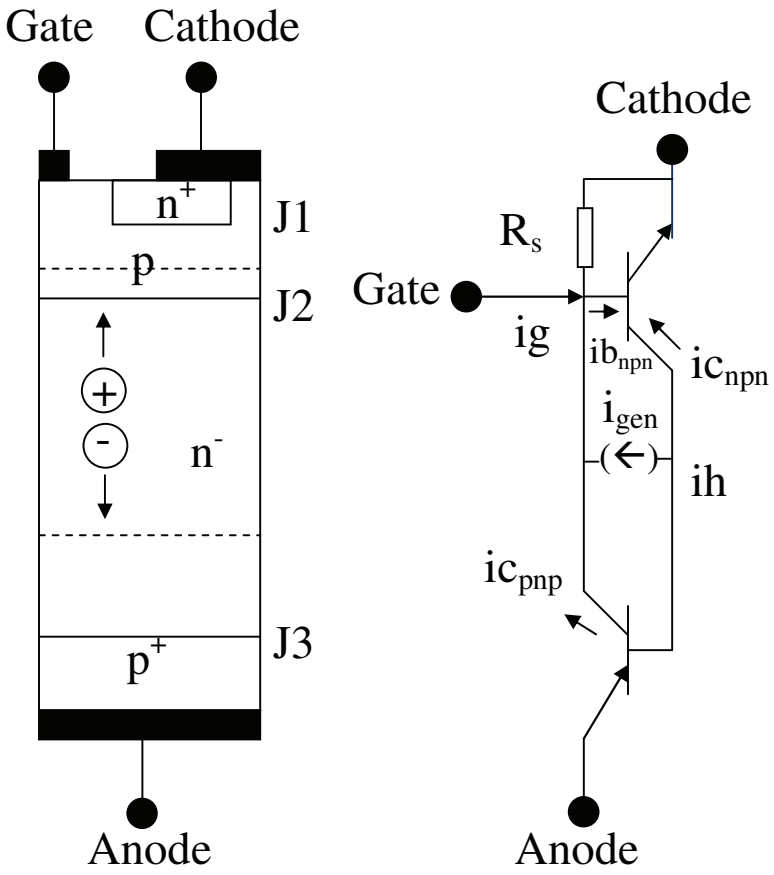


Figure 9 One dimensional turn-on process

(a) Schematic (b) Equivalent circuit

Hole current, ih= $i_{gen}+i_{opt}+i_{cap}$

i_{gen} - thermal generation current

i_{opt} - optical generation current

i_{cap} - capacitive current

Condition for “non-triggering”

$\beta_{npn}\beta_{pnp}<1$ or $\alpha_{npn}+\alpha_{pnp}<1$ where $\beta=\frac{ic}{ib},\alpha=\frac{ic}{ie}$

For the npn transistor, the shunt resistor is included as an inherent property. Therefore, the gate current is divided into two parts.

$ig = ib_{npn}+i_{Rs}$

On-state is obtained when the closed loop gain of the npn and pnp transistors, given by either $\beta_{npn}\beta_{pnp}$ or $\alpha_{npn}+\alpha_{pnp}$ approaches unity.

$\beta_{npn}\beta_{pnp}-1$

$\alpha_{npn}+\alpha_{pnp}-1$

This means that the parasitic currents or the gate current are negligible compared to $ic_{npn}+ic_{pnp}$.
Note: With ig = 0, $ic_{npn}+ic_{pnp}+ip=\alpha_{npn}ie_{npn}+\alpha_{pnp}ie_{pnp}+ip=ip+i_A(\alpha_{npn}+\alpha_{pnp})$

To determine the trigger level by parasitic or gate currents, it is inevitable to consider the strong dependence of β on base current. This is even the case if we want to determine the “temperature triggering”, because the increasing parasitic currents (blocking current) are more important than the temperature dependence of the β.

For βpnp, one may assume a relatively weak dependence on base current. This is not the case for βnpn.

Therefore,

Equation 2.10 $\beta_{pnp}\approx\tilde{\beta}_{pnp}=\frac{dic}{dib}$

Example to illustrate the significance of differentiation between constant and differential current gains during thyristor turn-on:

Assume an ideal npn transistor with internal current gain tending to infinity.

Then, because ig = i_{Rs},

Equation 2.11 $$ic = ic0 * e^{\frac{Rs*ig}{V_T}} \Rightarrow \frac{dic}{dig} = ic\frac{Rs}{V_T} = \tilde{\beta}_{npn}$$

Assume Rs= 20 Ω, at 300K

ic= 13mA for $\tilde{\beta} \to 10$

But $\frac{ic}{ib} \approx 0.4$

If we assume that $V_{BE} \approx 0.65V \Rightarrow \beta = 0.4, \tilde{\beta} = 10, \alpha = 0.3, \tilde{\alpha} = 0.9$

2.3.2 Condition for thyristor turn-on process

To calculate the condition for thyristor turn-on process, using βs instead of αs is the "natural" way to consider base current. Differential common emitter current gain $\tilde{\beta}$ is defined as,

Equation 2.12 $$\tilde{\beta} = \frac{dic}{dib} = \frac{\Delta ic}{\Delta ib}$$

A change (increase) in collector current of npn and pnp transistors,

Equation 2.13 $$\Delta ic_{npn} = \tilde{\beta}_{npn}\left(\Delta ig + \Delta ic_{pnp}\right)$$

Equation 2.14 $$\Delta ic_{pnp} = \tilde{\beta}_{pnp}\Delta ic_{npn}$$

Substituting 2.12 in 2.11,

Equation 2.15 $$\Delta ic_{npn} = \tilde{\beta}_{npn}\tilde{\beta}_{pnp}\Delta ic_{npn} + \tilde{\beta}_{npn}\Delta ig \Rightarrow \Delta ic_{npn} = \frac{\tilde{\beta}_{npn}\Delta ig}{1 - \tilde{\beta}_{npn}\tilde{\beta}_{pnp}}$$

This means that $\tilde{\beta}_{npn}\tilde{\beta}_{pnp} \to 1$ is sufficient for $\frac{\Delta ic_{npn}}{\Delta ig} \to \infty$

2.3.2.1 To calculate differential common emitter current gain $\tilde{\beta}$ of a shunted npn transistor

From Figure 9,

Equation 2.16 $ib = ig - i_{Rs}$

Assume, $ib = \frac{ic}{\beta i}$ where βi is constant common emitter current gain of the npn transistor.

Equation 2.17 $ic = ic0 * e^{\frac{Rs*i_{Rs}}{V_T}} = ic0 * e^{\frac{Rs\left(ig - \frac{ic}{\beta i}\right)}{V_T}}$

Equation 2.18

$$\frac{dic}{dig} = ic\frac{Rs}{V_T}\left(1 - \frac{1}{\beta i}\frac{dic}{dig}\right) \Rightarrow \frac{dic}{dig}\left(1 + ic\frac{Rs}{V_T \beta i}\right) = ic\frac{Rs}{V_T} \Rightarrow \frac{dic}{dig} = \frac{ic\frac{Rs}{V_T}}{\left(1 + ic\frac{Rs}{V_T \beta i}\right)} = \tilde{\beta}_{npn}(ic)$$

Where, $\tilde{\beta}_{npn}(ic)$ is the differential common emitter current gain of a shunted transistor as a function of ic.

If $\beta i \to \infty, \tilde{\beta}_{npn} = \frac{dic}{dig} = \frac{icRs}{V_T}$

For a reasonable $\tilde{\beta}_{npn} = \frac{dic}{dig} \approx 2 \to 4$ (from 2.15)

We have $icRs \approx 0.5V - 1V$. Therefore, at 300K, a voltage drop of 0.5V to 1V across the shunt resistance is required to turn-on and keep the on-state of a thyristor.

2.3.3 Pulse triggering of a shunted thyristor

A different analytical treatment than the classical charge control model found in thyristor literature is necessary for thyristor triggering by high current pulses (typical in high dv/dt triggering) in case of shunted thyristors.

Charge control model for un-shunted transistors:

Equation 2.19 $ic_{npn} = \frac{Q_{npn}}{tt_{npn}}$

Equation 2.20 $\frac{dQ_{npn}}{dt} = ib_{npn} + \frac{Q_{npn}}{\tau_{npn}}$

Equation 2.21 $$ic_{pnp} = \frac{Q_{pnp}}{tt_{pnp}}$$

Equation 2.22 $$\frac{dQ_{pnp}}{dt} = ib_{pnp} + \frac{Q_{pnp}}{\tau_{pnp}}$$

We can define,

Equation 2.23 $$\beta_{npn} = \frac{\tau_{npn}}{tt_{npn}}, \beta_{pnp} = \frac{\tau_{pnp}}{tt_{pnp}}$$

For a shunted thyristor:

$i_{Rs} \approx \frac{V_{BE}}{Rs}$ and V_{BE} = 0.6 to 0.7 V at 300K, 0.3 to 0.4 V at 400K

Therefore, we assume i_{Rs} is constant for a given temperature.

Equation 2.24 $$\frac{dQ_{npn}}{dt} = -\frac{Q_{npn}}{\tau_{npn}} + \frac{Q_{pnp}}{tt_{pnp}} - i_{Rs}$$

Equation 2.25 $$\frac{dQ_{pnp}}{dt} = -\frac{Q_{pnp}}{\tau_{pnp}} + \frac{Q_{npn}}{tt_{npn}}$$

Equation 2.26 $$\frac{d^2Q_{npn}}{dt^2} = -\frac{dQ_{npn}}{dt}\frac{1}{\tau_{npn}} + \frac{dQ_{pnp}}{dt}\frac{1}{tt_{pnp}} = -\frac{dQ_{npn}}{dt}\frac{1}{\tau_{npn}} + \frac{1}{tt_{pnp}}\left(\frac{Q_{npn}}{tt_{npn}} - \frac{Q_{pnp}}{\tau_{pnp}}\right)$$

Equation 2.27 $$Q_{pnp} = tt_{pnp}\left(\frac{dQ_{npn}}{dt} + \frac{Q_{npn}}{\tau_{npn}} + i_{Rs}\right)$$

Equation 2.28 $$\frac{d^2Q_{npn}}{dt^2} = -\frac{dQ_{npn}}{dt}\frac{1}{\tau_{npn}} + \frac{1}{tt_{pnp}}\left(\frac{Q_{npn}}{tt_{npn}} - \frac{tt_{pnp}}{\tau_{pnp}}\left(\frac{dQ_{npn}}{dt} + \frac{Q_{npn}}{\tau_{npn}} + i_{Rs}\right)\right)$$

From the above second order differential equation of Q_{npn}, a condition for constant Q_{npn} has to be derived above which we shall expect triggering and below which a decaying Q_{npn}.

Stationary case:

Equation 2.29 $$0 = 0 + \frac{1}{tt_{pnp}}\left(\frac{Q_{npn}}{tt_{npn}} - \frac{tt_{pnp}}{\tau_{pnp}}\left(0 + \frac{Q_{npn}}{\tau_{npn}} + i_{Rs}\right)\right)$$

Equation 2.30 $$\Rightarrow Q_{npn} = i_{Rs} \frac{tt_{npn} tt_{pnp} \tau_{npn}}{\tau_{npn}\tau_{pnp} - tt_{npn} tt_{pnp}}$$

$$\beta = \frac{\tau}{tt}$$

Equation 2.31 $$\Rightarrow Q_{npn} = i_{Rs} \frac{\tau_{npn}}{\beta_{npn}\beta_{pnp} - 1} = i_{Rs} \frac{\beta_{npn} tt_{npn}}{\beta_{npn}\beta_{pnp} - 1}$$

Note: τ_{npn}, τ_{pnp} are effective lifetimes containing emitter recombination. In case of infinite bulk lifetime, $\tau = \frac{W_B{}^2}{2D_h} \frac{\int n^+ dx}{\int N_A dx}$

Where,

$\int n^+ dx$ - Emitter Gummel number

$\int N_A dx$ - Base Gummel number

From Eq. 2.32, conditions for pulse triggering in case of a shunted thyristor is

$\beta_{npn}\beta_{pnp} > 1$ resulting in a positive Q_{npn}

The product $i_{Rs} * Rs \cong 0.6 \rightarrow 0.7$V at 300K and $0.3 \rightarrow 0.4$V at 400K

3 Schematics of an 8kV SCR and a 13kV tandem LTTs

In this chapter, the following topics are discussed:

- Schematics of an 8kV symmetrically blocking thyristor and a 13kV symmetrically blocking tandem LTTs
- Comparison of electric field profiles between an 8kV SCR and a 13kV ASCR

3.1 Schematic of an 8kV symmetrically blocking LTT

Figure 10 (a) shows the schematic of an 8kV symmetrically blocking LTT. An 8kV SCR is an n-p-n-p structure.

- n^+ emitters on the cathode side (shunted to the p-base)
- p-base
- n^- base
- p^+ emitter on the anode side

Doping profile of an 8kV SCR is shown in Figure 11.

3.2 Schematic of a 13kV symmetrically blocking tandem device

Figure 10 (b) shows the schematic of a 13kV symmetrically blocking tandem LTT. A 13kV tandem device is essentially, a series connection of a 13kV asymmetrically blocking thyristor and a 13kV diode. A 13kV ASCR is an n-p-n-n-p structure.

- n^+ emitters on the cathode side (shunted to the p-base)
- p-base
- n^- base
- n-buffer (Field stop layer)
- p^+ emitter on the anode side (shunted to the n-buffer)

Figure 12 shows the doping profile in a 13kV ASCR from a cut through p^+ emitter- n-buffer- n^- base- p-base-n^+ emitter. Figure 13 shows the doping profile in a 13kV ASCR from a cut through n-buffer- n^- base- p-base (i.e. cut through anode and cathode shunt)

A 13kV diode is an n-n-n-p structure

- n^+ emitters on the cathode side
- n-buffer
- n^- base
- p^+ emitter on the anode side

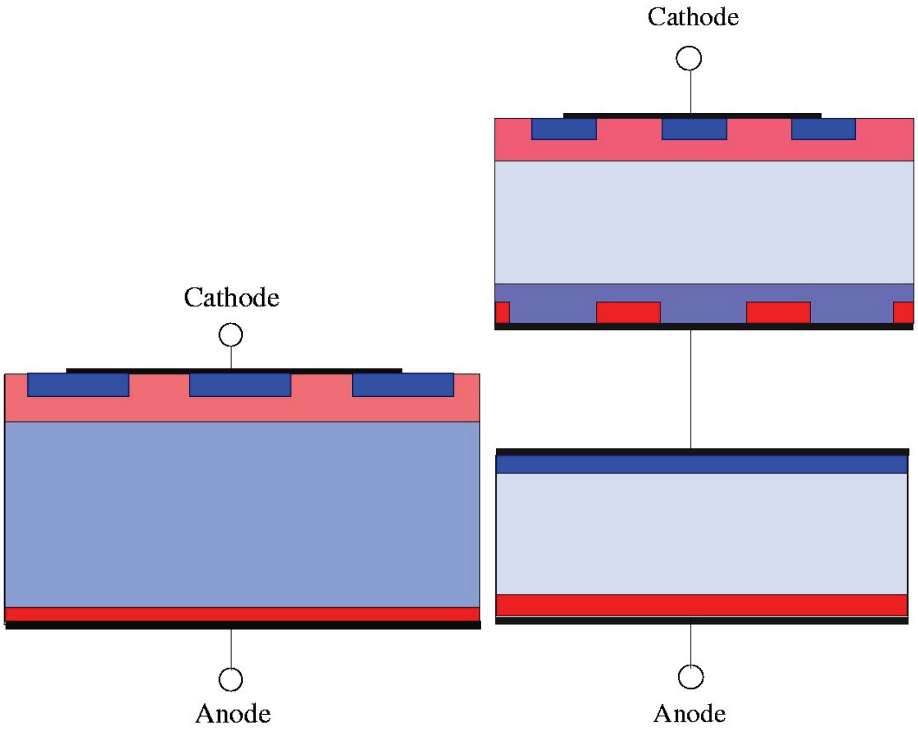
Figure 14 shows the doping profile of such a 13kV series diode.

The anode metal contact of the 13kV ASCR and the cathode metal contact of the 13kV diode are mechanically pressed together in the tandem device package to ensure a good electrical contact.

In this work, only the design of the 13kV asymmetrical SCR (ASCR) is investigated. Investigations on the design of the 13kV series diode are done by the high voltage diode development group in Infineon Technologies.

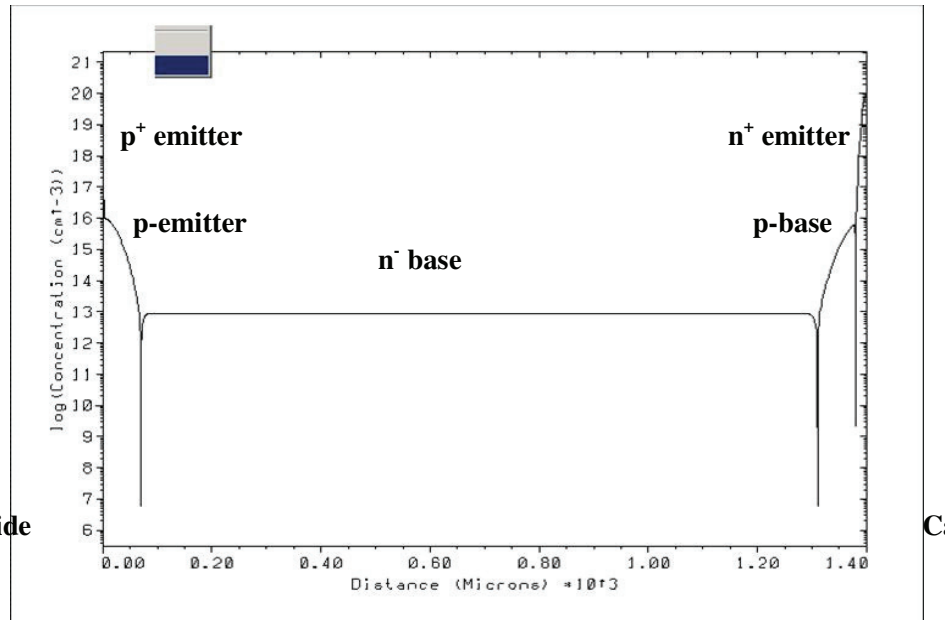
Primarily, the design of a 13kV ASCR is same as the 8kV symmetrical device on the cathode side. The n^- width of the 13kV ASCR is 1380µm where as the n^- width of the 8kV SCR is 1220µm .However, the anode side diffusion profiles and metallization are completely different to that of an 8kV device.

Essentially, a 13kV ASCR has an n-buffer on the anode side with a Gummel number higher than 2e12 cm^{-2}. The n-buffer layer stops the electric field from reaching the p^+ anode in forward blocking and limits the reverse blocking voltage to a few 10's of volts. The design aspects of the n-buffer and the anode p^+ emitter profiles are discussed in section 5.2 considering their influence on thyristor characteristics.



(a) 8kV symmetrically blocking SCR **(b) 13kV symmetrically blocking tandem device**

Figure 10 Basic schematic of an 8kV SCR and a 13kV tandem thyristor



Anode side **Cathode side**

Figure 11 Doping profile of an 8kV SCR

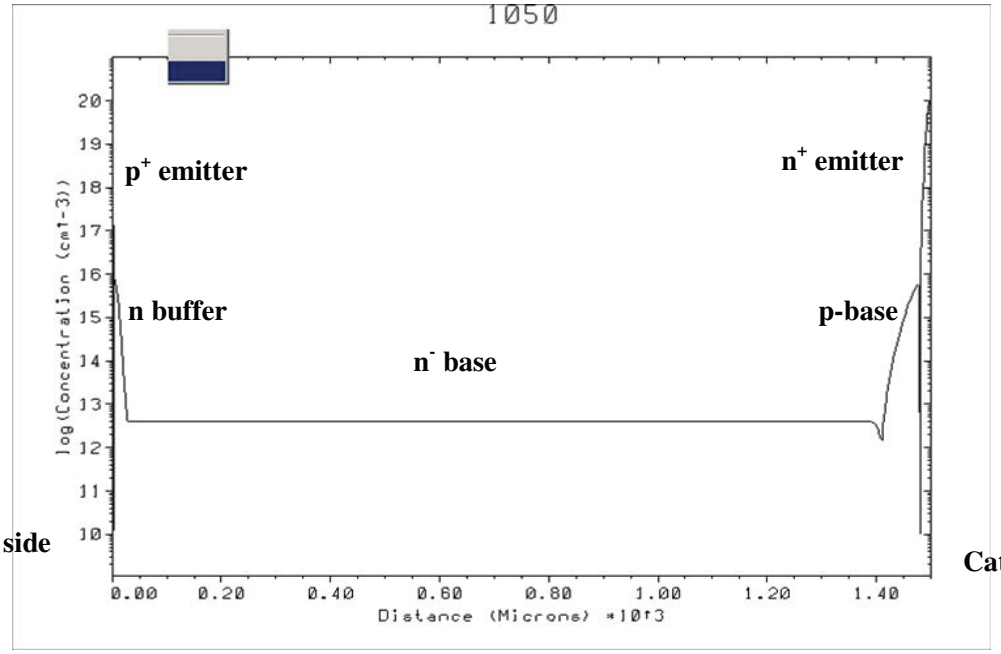


Figure 12 Doping profile of a 13kV ASCR

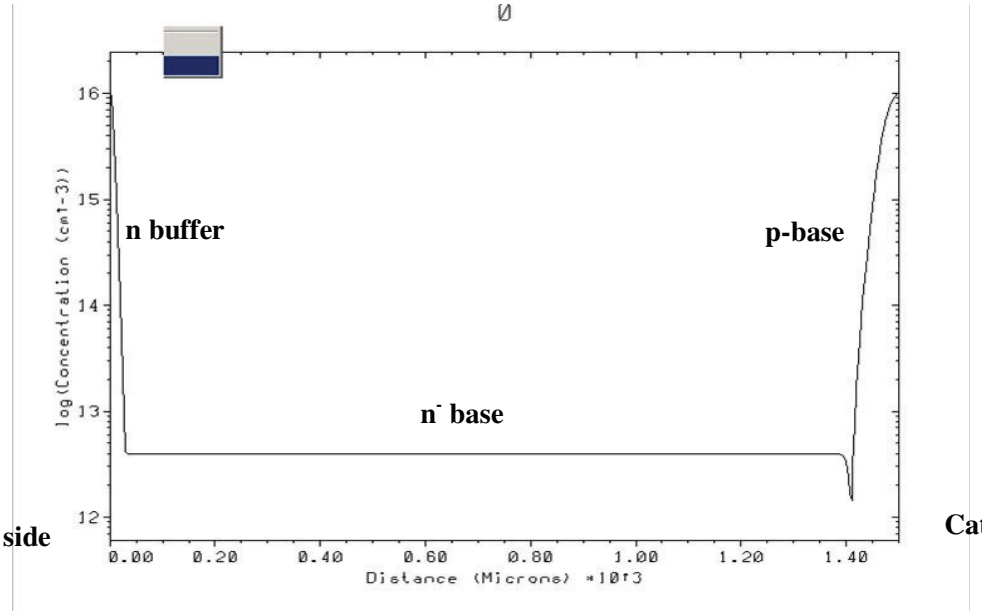


Figure 13 Doping profile of a 13kV ASCR (cut through an anode and a cathode shunting hole)

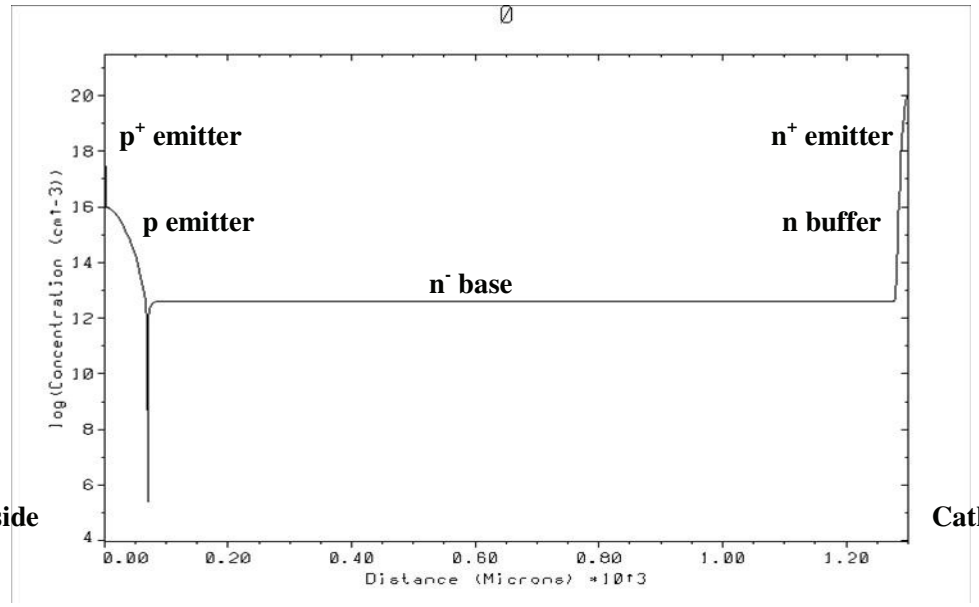


Figure 14 Doping profile of the series diode in a 13kV tandem device

3.3 Comparison of electric field profiles of an 8kV SCR and a 13kV ASCR in forward blocking state

3.3.1 8kV symmetrical thyristor

In a symmetrical thyristor, electric field profile is continually triangular with increasing voltage in both forward and reverse blocking conditions. In forward blocking state, the p-n junction formed at p-base-n^- -base is negatively biased. The space charge region spreads deeper into the n^- -base compared to p-base due to its lower doping concentration compared to the later as shown in Figure 15 (a). However, the edge of the electric field is not allowed to reach the p^+ emitter of anode in forward blocking conditions. Therefore, the Gummel number of the n^- -base has to be more than the critical Gummel number, 2.5e-12cm^{-2}. To make an efficient use of n^- width, the Gummel number of n^- -base is usually chosen very close to the critical Gummel number.

The forward break-over of thyristor is caused by either avalanche break-down or punch-through.

3. Schematics of an 8kV SCR and a 13kV tandem LTTs

3.3.1.1 Avalanche break-down

If the peak of the electric field at the p-base-n^- -base junction reaches the critical electric field, 1.8e5 - 2.6e5 $\frac{V}{cm}$ (for Si at 300K), an avalanche of carriers is generated which will lead to forward break-over. This phenomenon is called avalanche break-down.

3.3.1.2 Punch-through

During forward blocking, assume that the electric field is triangular in shape as shown in Figure 15(a) neglecting the penetration of SCR into the p-base region. The punch through voltage is given by,

Equation 32 $$V_{PT} = \frac{qN_D W_B^2}{2\varepsilon}$$

q- Unit charge

N_D- n^- doping concentration

W_B- width of the neutral n^- zone

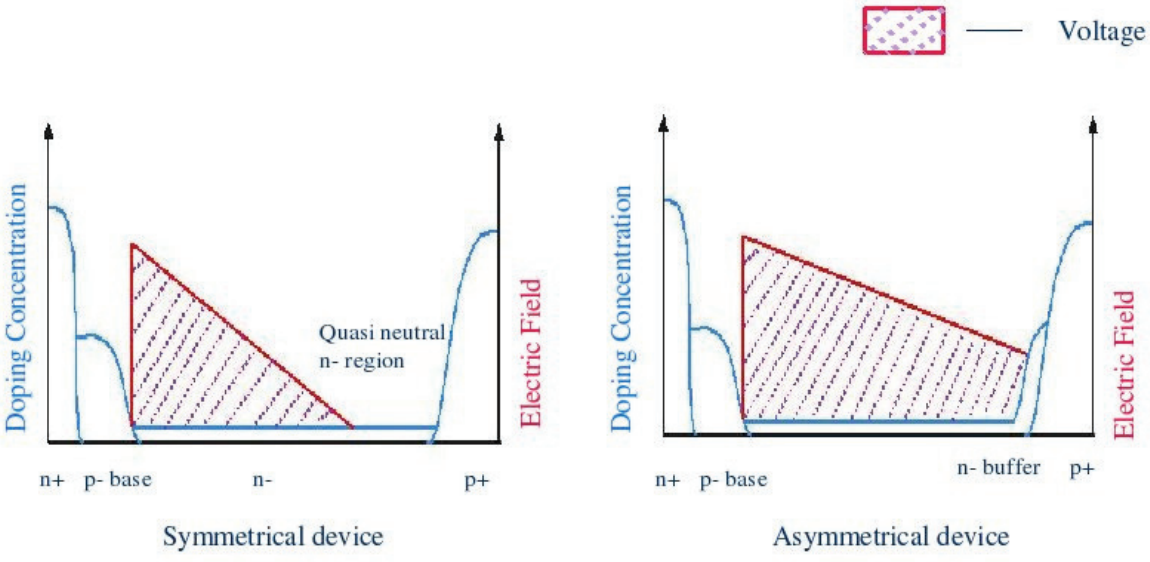
ε- Dielectric constant of Si

3.3.2 13kV asymmetrical thyristor

The electric field profile in an ASCR in forward blocking state is triangular until the edge of the electric field reaches the begin of n-buffer layer and since then converts into trapezoidal form as shown in Figure 15(b), where as in an SCR; the electric field profile is triangular continually. The trapezoidal electric field profile results in a higher blocking voltage in the same n^- width.

The Gummel number of the n^- base has to be less than the critical Gummel number so that the edge of the electric field can reach the n-buffer under sufficient voltage. The Gummel number of the n-buffer has to be marginally more than the critical Gummel number so that the edge of the electric field never reaches (punch-through) the p^+ emitter and still accommodate space charge and reduce the strength of electric field at the buffer.

3. Schematics of an 8kV SCR and a 13kV tandem LTTs



(a) **(b)**

Figure 15 Comparison of electric fields in an SCR and ASCR

4 Detailed gate structure of a LTT

The part of a thyristor which commutates the load current is referred to as “main thyristor”. The trigger sensitivity of a main thyristor is usually designed to such a value so that either specified fault voltage surges doesn’t produce enough capacitive (displacement) current to turn the thyristor ON. This means that the main thyristor must be designed in a way that it needs a reasonably high trigger current to be turned ON. Therefore, a series of pilot thyristors or Amplifying Gates (AGs) are necessary to amplify a safe trigger current pulse to a magnitude that is sufficient to trigger the main thyristor. The design parameters here include the magnitude of trigger pulse, di/dt, area of the AGs, speed of triggering, triggering voltage. The number of AGs is chosen from experimental data and experience in a way that the main thyristor trigger current is achieved from the trigger pulse of the AG1 without overloading (causing high temperatures locally) any AG.

“Unlike the state-of-the-art ETTs, the state-of-the-art LTTs require more pilot thyristors to be able to supply the trigger current for the main thyristor due to limited available optical power. The minimum number of AG stages necessary in a thyristor for a given nominal trigger current is determined by

In case of LTTs under investigation in the present work, four AGs are required to supply the trigger current for the main thyristor. The AG1 is designed to be the most sensitive among all four AGs by an increased sheet resistance of p-base underneath the n^+ emitter of the AG1. The triggering currents of other AGs are tailored by adjusting the physical dimensions of the n^+ emitters but the sheet resistance of the p-base is kept constant.

The width of the n^- region is selected to be 1415µm. The forward break-over voltage of a thyristor is normally determined by the 3D spatial integral of the electric field profile at avalanche breakdown of the p-base-n^- base junction. However, forward break over in the main thyristor can lead to inhomogeneous current distribution due to imperfections, for e.g. in doping profiles, leading to a possible current filamentation. To evade this problem, an avalanche diode, usually known as BOD (Break Over Diode) is integrated in the optical window region (Figure 17) of the thyristor which has a lower avalanche break-down voltage compared to the thyristor break down voltage. Therefore, the forward break down always occurs in BOD at the cost of a reduction of a few hundred Volts in the forward break over voltage specification.

As it can be seen in Figure 17, the curvature of the p- diffusion profile in the BOD which results in a cylindrical junction determines the avalanche break down voltage of BOD and therefore also of the thyristor. Hence, the curvature of the p-base profile in BOD has to be accurately reproducible in mass production to maintain the forward break over voltage. Appendix C describes the dependence of avalanche break down voltage of cylindrical and spherical junctions on the curvature of their junctions.

4. Detailed gate structure of a LTT

To protect thyristors in high di/dt triggering, a lateral resistor is introduced between 2nd and the 3rd amplifying gates (AGs). Such a lateral resistor (Figure 16) is required to protect the mechanically stressed and thus electro-mechanically sensitive inner AGs from high di/dt and BOD triggering or triggering from high voltages. The lateral resistor reduces the voltage in the inner AGs and thereby reduces the power drop which subsequently helps in keeping the temperatures low in inner AG region. The value of the resistor is selected as 100Ω from experimental data and experience.

AG1 and AG2 are designed in a way that for typical trigger pulses, AG2 triggers fast enough to share the load with AG1 and thereby avoid high temperatures in AG1 region. The same is valid for the design of AG3 and AG4.

The lateral protection resistor is realized by p-doping over a length of 2mm between AG2 and AG3. This extra area resulted by the integration of the lateral protection resistor helps the current to distribute over a larger area during turn-on and thereby improves the turn-on di/dt rating of the thyristor. During BOD and triggering from very high voltages, the lateral protection resistor dissipates a large amount of anode-cathode voltage and thus reduces the voltage and consequently temperatures in the inner AGs. This topic is discussed in detail in Chapter 6.

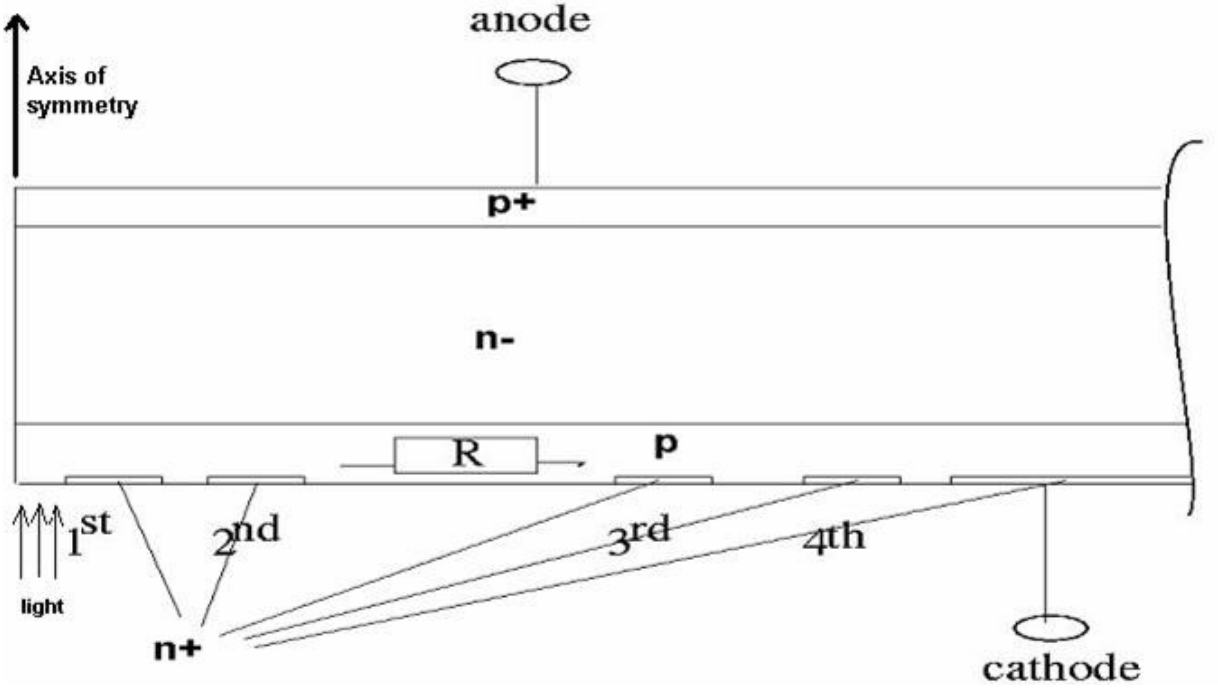


Figure 16 Basic schematic of an 8kV SCR

4. Detailed gate structure of a LTT

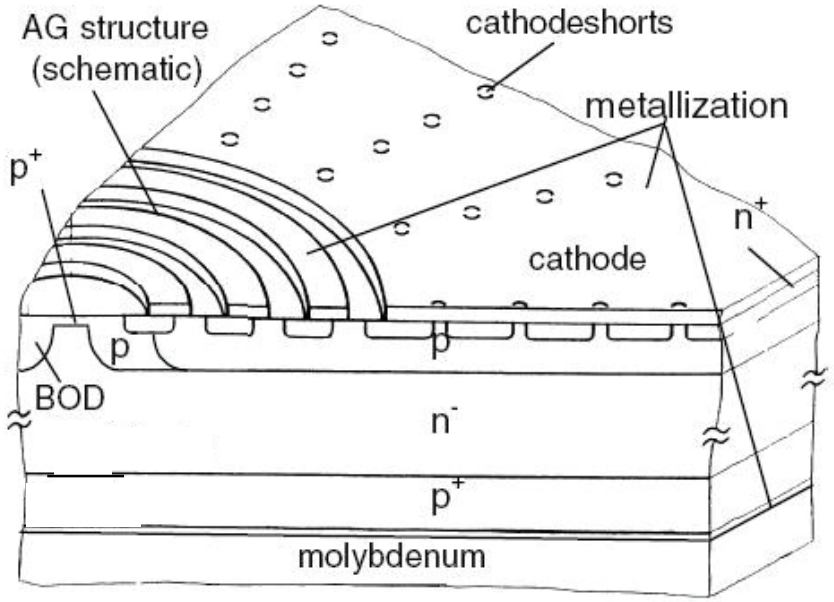


Figure 17 Detailed schematic of an 8kV SCR

5 Dynamics of Space Charge Region (SCR) in symmetrical and asymmetrical thyristors and its influence on the triggering speed and the temperature in the device

In this chapter, the influence of Space Charge Region (SCR) dynamics on the thyristor characteristics such as, temperature in the optical window, speed of triggering and electric field dynamics is studied.

If all the other influencing parameters are unaltered, the triggering speed of a symmetrical thyristor depends on the space charge dynamics. In asymmetrical thyristors, the triggering speed is mainly influenced by the PNP transistor current gain. In other words, by the anode emitter efficiency and the n-buffer Gummel number.

The temperature development with time in the inner AG regions is proportional to the integral of power dump over time in the inner AG regions. In other words, there are 3 degrees of freedom to reduce the temperature in the inner AGs, viz. voltage, current and time. Usually, reduction in one of these 3 parameters results in increase in either or both of the other 2 parameters.

However, a few tricks to solve this problem despite the interdependency are investigated in this work which will be discussed in detail in Chapter 8. A more important question that has to be answered is the confinement and location of the temperature which affects the robustness of the thyristor. The answer to this question directly depends on the dynamics of the space charge region in both symmetrical and asymmetrical thyristors. This dependency is discussed more clearly in the subsections 5.1.2, 5.2.2.

5.1 Symmetrical thyristors

5.1.1 Triggering speed

Triggering speed is an important factor in evaluating the robustness of a thyristor. Triggering speed is one of the parameters that influence the temperature growth in the inner AGs. Triggering of a thyristor involves two transit times, transit time of the holes and electrons to cross the n^- region and p base region respectively. Intuitively, triggering speed of a thyristor depends on the slower process of the thyristor triggering. In high voltage thyristors the transit

time of the holes to cross the larger n^- region is higher than that of electron's. In other words, the triggering speed directly depends on the delay caused by holes in the process of triggering.

If a thyristor is triggered from a high forward voltage so that most of the n^- region is loaded by space charge, reducing the effective width of the n^- region which the holes have to cross to reach the p-base (which acts like a collector to the pnp transistor), the triggering speed of the thyristor can be increased.

For a better understanding, assume that a thyristor is triggered from a high voltage. The SCR in the n^- region moves towards the p^+ anode resulting in a time dependent reduction of the transit time of the holes. When the SCR tend to touch the p^+ anode, the differential gain of the PNP transistor, $\tilde{\beta}_{PNP}$ tends to reach unity [Reference 1] which means that the number of electrons reaching the anode from the cathode side is equal to the number of holes emitted by the anode. The delay caused by transit time of electrons causes the SCR to move backwards for a short time. This phenomenon is called dynamic punch-through. Figure 18 depicts a simulation of dynamic punch-through

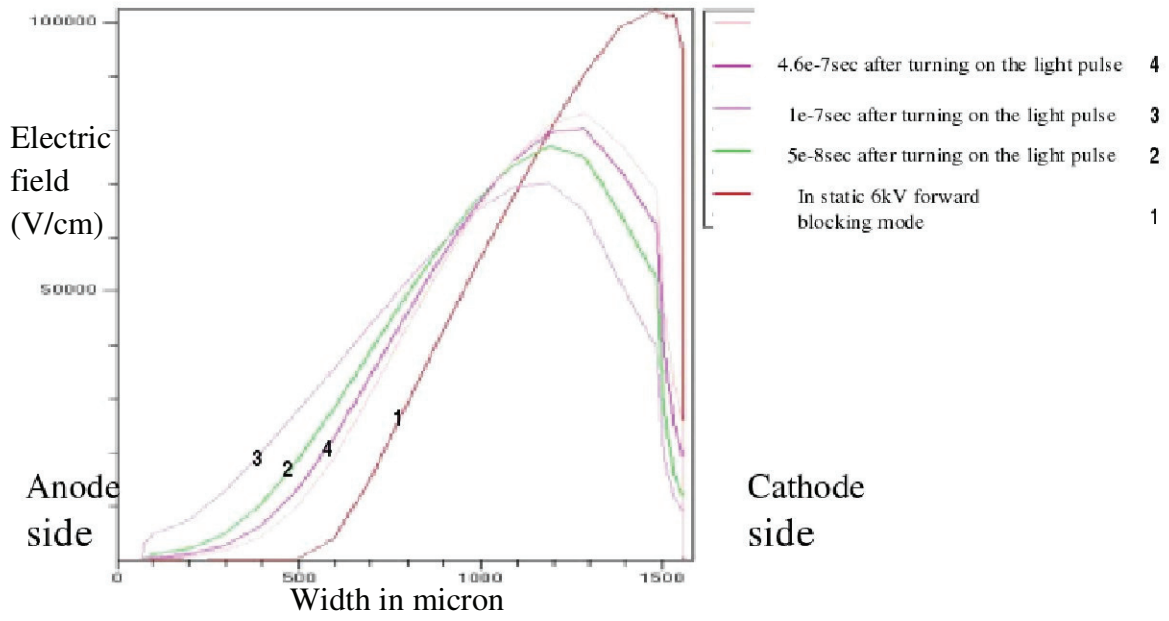


Figure 18 Phenomenon of dynamic punch-through

Dynamic punch-through has effect even if the thyristor is triggered from a low voltage, but does not result in a faster turn-on of the thyristor (Figure 19). Since, for thyristor triggering, the effective n^- region (W_{neff}= total width of n^- - width of SCR) has to be filled with plasma. The time required to fill this region with plasma is directly proportional to the square of the effective

width of the n^- region (W_{neff}^2). Since the W_{neff} is much larger in case of triggering from low voltages, the triggering speed is also much lower.

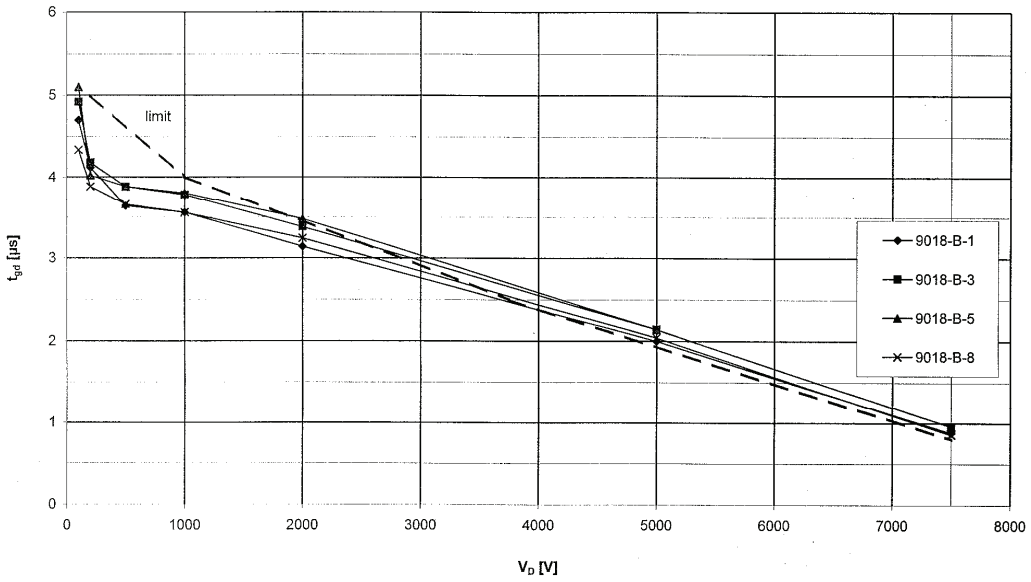


Figure 19 **Trigger delay Vs. Triggering voltage at junction temperature of a typical 8kV LTT, T_{vj}=25°C, trigger power= 40mW**

5.1.2 Temperature development

During triggering, the electric field peak shifts from cathode towards anode side in symmetrical thyristors due to emission of electrons from n^+ emitters. With the electric field peak, the hot spot also moves to the anode side. If the thyristor is cooled both from anode and cathode sides (typical in HVDC applications), this phenomenon shall not influence the effective cooling of the thyristor significantly. Nonetheless, if only one sided cooling is allowed, cooling on the anode side is recommended. In this case, the faster the hot spot moves to the anode side, the better is the effective cooling.

When a thyristor is triggered from high voltage, the magnitude of the temperature can be high at the hot spot until the voltage breaks down to a lower value. Dynamic punch-through consequences in a faster turn-on of the AG1, thus in a faster break down of the voltage which results in a relatively lower temperature at the hot spot.

A lateral resistor is introduced between the inner and outer AGs to reduce the voltage in the inner AGs during triggering. This resistor slumps approximately 30% of the anode-cathode voltage during triggering from very high voltages (in the order of 6kV to 7kV) and thereby

protects the inner AGs. The lateral resistor is designed in such a way that a homogeneous current density is achieved radially.

5.2 Asymmetrical thyristors (ASCRs)

5.2.1 Triggering speed

The triggering speed of an ASCR is directly related to $\tilde{\beta}_{PNP}$ which is mainly influenced by the n-buffer Gummel number and the p+ emitter efficiency.

In this work, 1-D simulations are done on two extreme cases.

- case1- High p+ emitter efficiency and low n- buffer Gummel number($\tilde{\beta}_{PNP}$ is high)
- case2- Low p+ emitter efficiency and high n- buffer Gummel number($\tilde{\beta}_{PNP}$ is low)

Clearly, the device with case1 anode side profile has a higher triggering speed than that of case2 due to higher $\tilde{\beta}_{PNP}$.

5.2.2 Temperature development

Dynamics of SCR play an important role in temperature growth in ASCRs. In asymmetrical thyristors with lower $\tilde{\beta}_{PNP}$, e.g. case2 in Figure 20, a stronger shift in electric field peak from cathode to anode side is observed as shown in Figure 21 (a). In case of thyristors with higher $\tilde{\beta}_{PNP}$, e.g. case1 in Figure 20, the higher electric field on the anode side is reduced by a faster and stronger emission of holes from the anode as shown in Figure 21 (b). Consequently, it is clear that a thyristor with higher $\tilde{\beta}_{PNP}$ will have a lower temperature at the hot spot (Figure 22). In both cases (as these are two extreme cases), the hot spot will always be on the extreme anode side. Therefore, anode side cooling in asymmetrical thyristors has a better cooling effect.

However, in a Tandem device (Figure 10(b)), the thyristor package includes an ASCR connected in series with a diode. During triggering, the hot region in the ASCR is on the anode side (middle of the tandem device) and in the diode on the cathode side (middle of the tandem device). This means that the hot region in a Tandem device is not close to any of the heat sinks even in double sided cooling which leads to higher power losses.

A comparison study has been performed where the total losses in a thyristor valve with 8kV SCRs are compared to a thyristor valve with 13kV tandem devices from HVDC applications point of view. Although the number of tandem devices required to attain the same valve-voltage rating is 40-50% lower compared to the number of 8kV SCRs, the total

valve-losses are 20-30% higher in case of valves with tandem devices compared to valves with 8kV SCRs.

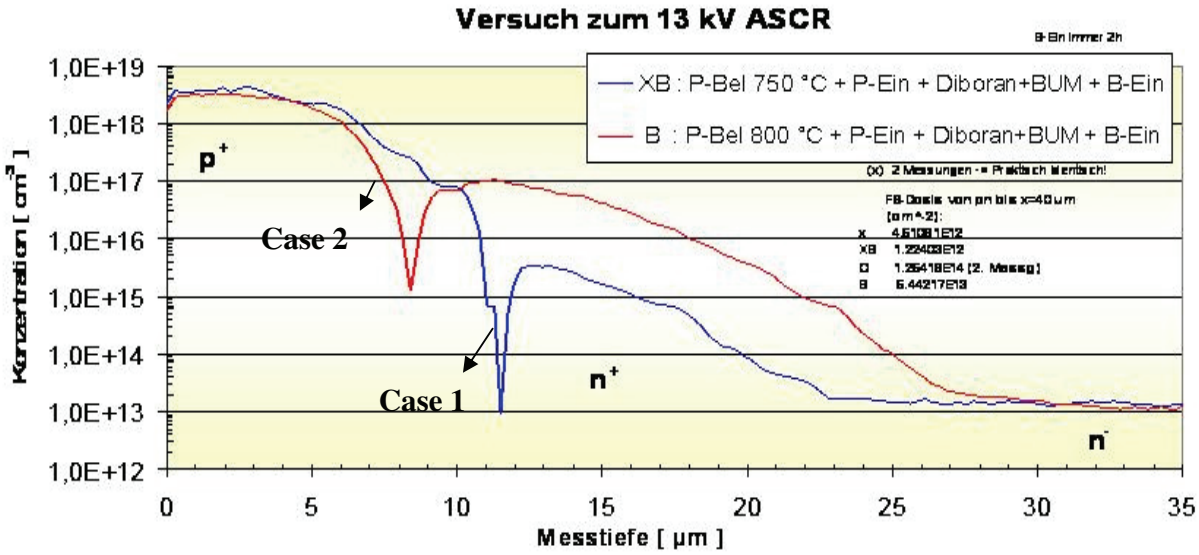
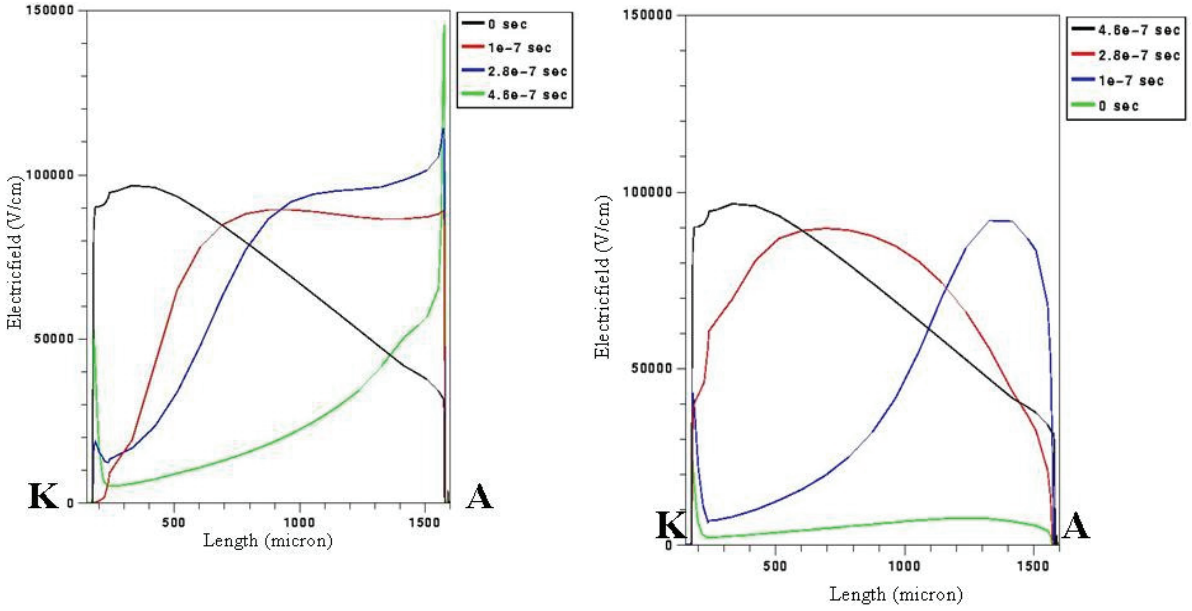


Figure 20 Two different types of investigated anode-side profiles



(a) **(b)**

Figure 21 Comparison of dynamics of electric fields in 13kV ASCR with anode side profiles shown in Figure 20

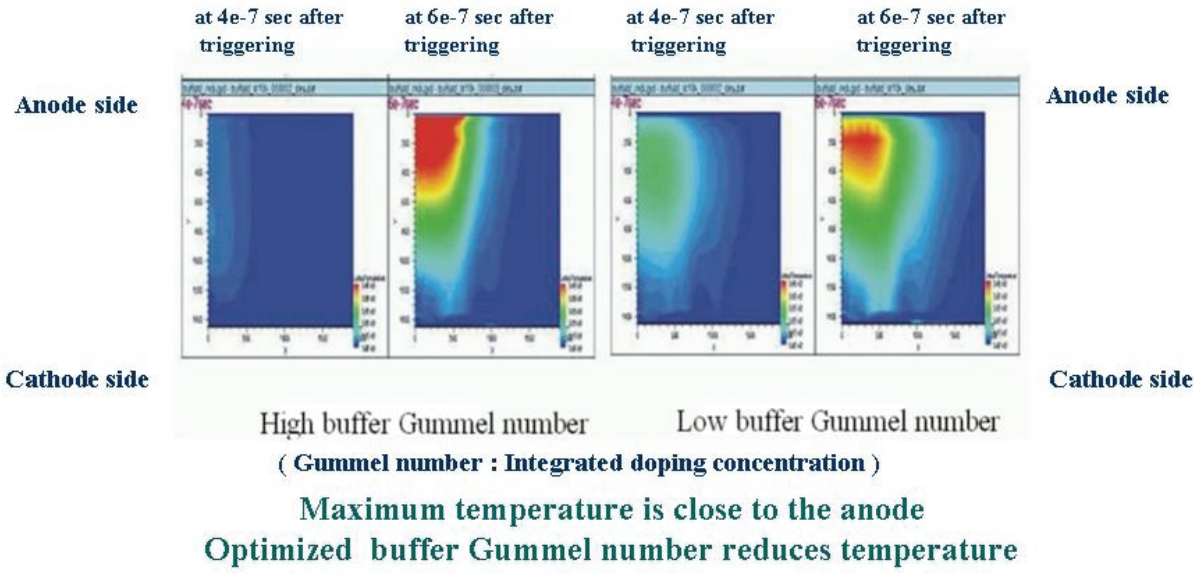


Figure 22 Development of temperature in 13kV ASCRs with two different anode-side profiles shown in Figure 20

5.2.3 Anode shunting in 13kV ASCR

5.2.3.1 Necessity of anode shunting

Differential current gain of the PNP transistor, $\tilde{\beta}_{PNP}$ in 13kV ASCR (even with case2 anode side profile in Figure 20) is so high at temperatures over 400K that the forward blocking voltage of a tandem device is drastically reduced as shown in Figure 23. To achieve full blocking capability, $\tilde{\beta}_{PNP}$ has to be drastically reduced. Reducing the p^+ emitter efficiency or increasing n-buffer Gummel number in the allowed limits doesn't reduce the PNP transistor gain $\tilde{\beta}_{PNP}$ enough to attain a full forward blocking capability.

The following ways to reduce $\tilde{\beta}_{PNP}$ are investigated [Reference 9]:

1. To lower the lifetime in the n- buffer or in the junction of p^+ emitter and n-buffer.
2. To introduce anode shunting

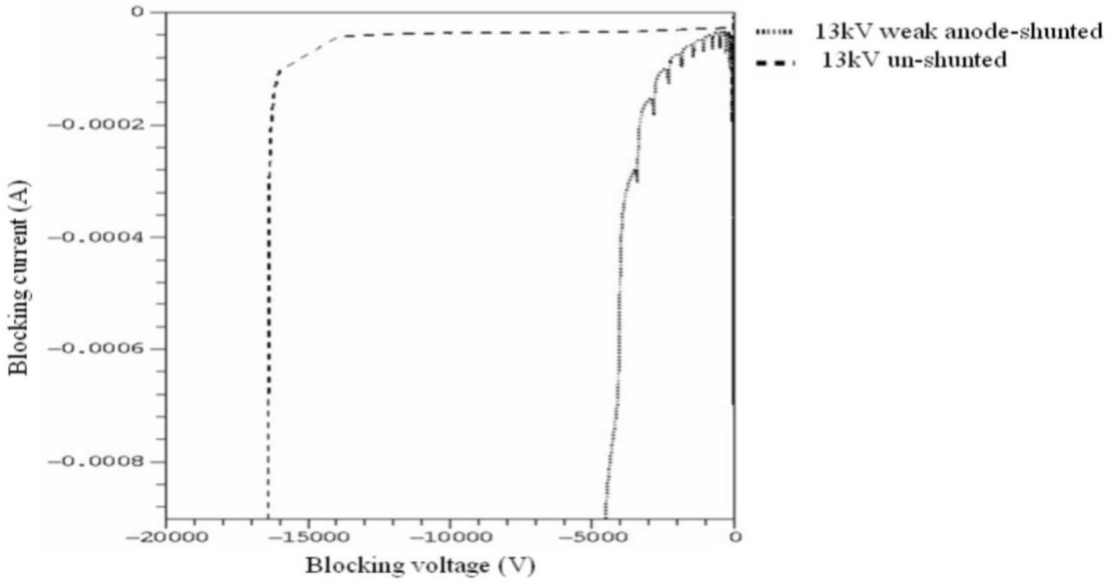


Figure 23 Comparison of forward blocking capability of a 13kV ASCR with and without anode shunting at 400K operating temperature

Although these two ways reduce $\tilde{\beta}_{PNP}$, their effects on other thyristor characteristics are diverse.

In case of lifetime reduction, at high current densities, current is calculated according to the high level lifetime and at low current densities, current is calculated according to the low level lifetime (which is typically three times lower than the high level lifetime for both electrons and holes).

In the anode shunted region, at low current densities, $\tilde{\beta}_{PNP}$ is nearly zero and at medium and high current densities, plasma concentration is lower than at the un-shunted region due to reduction of resistivity by plasma at shunted regions.

Simulation studies [Reference 6] demonstrated that the anode shunting has a better performance compared to local lifetime reduction taking on-state voltage drop and forward blocking characteristics (blocking voltage vs. blocking current) into account. Figure 23 shows that even a weak (less dense) anode shunting is enough to attain full forward blocking voltage at high operating temperatures around 400K.

5.2.3.2 Improving the characteristics of an ASCR using anode shunting.

As anode shunting provides an additional degree of freedom in design of asymmetrical devices, it can be exploited to improve other features of an ASCR.

In this work, different anode shunting profiles are investigated to improve dv/dt rating of a 13kV ASCR. A stronger anode response to dv/dt pulses could result in a fault dv/dt triggering.

As shown in Figure 24, a 13kV ASCR without any anode shunting has a strong anode response to a dv/dt pulse of 8kV/1µsec. With a strong (denser) anode shunting, the anode response to a dv/dt pulse can be reduced drastically as shown in Figure 24. The anode response of an 8kV symmetrically blocking thyristor is also shown for an equivalent dv/dt pulse of 5kV/1µsec. It can be established that the anode response is very weak in an 8kV symmetrical device.

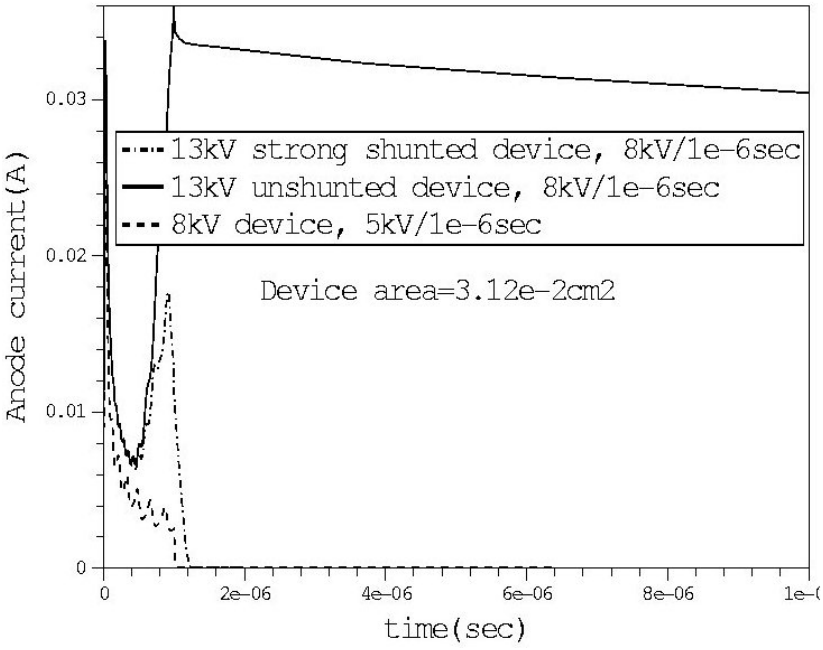


Figure 24 Comparison of anode responses of a 13kV densely shunted, un-shunted ASCRs and 8kV symmetrical thyristors to an equivalent dv/dt pulse (For 13kV ASCR, 8kV/1µsec is equivalent of 5kV/1µsec for an 8kV SCR)

Note:

Traditionally, the strength of anode shunting is calculated as the ratio of total area of shunting holes (number of shunting holes x area of a shunting hole) to the area of the anode metal contact. Such a definition is not complete as it doesn't give any information about the profile of shunting holes. It is important to include the parameter "distance between the centers of shunting holes" when specifying a shunting profile. A denser shunting means that additional shunting holes are introduced between the existing shunting holes and thereby effectively reducing the distance between the centers of neighboring shunting holes.

5.2.3.3 Influence of anode shunting on on-state voltage drop of the device

Evidently, an increase in on-state voltage drop shall be predicted owing to anode shunting because of reduction in the effective anode emitter efficiency. An increase in on-state voltage drop means an increase in the on-state power losses. If the increase in on-state voltage drop is not within the allowed limits, then anode shunting shall not be accepted.

Simulation results of plasma profiles of an un-shunted 13kV ASCR and a densely shunted 13kV ASCR are compared (Figure 25). It can be seen that the plasma concentration at the anode shunted regions is only slightly lower compared to that of the un-shunted regions. The resulting increase in on-state voltage drop at the lowest typical current density (30 A/cm^2), where the difference in the on-state voltage drops shall be high, is only 0.2V compared to that of the un-shunted device. This result hints that a weak anode shunting affects only a minor increase in the on-state voltage drop of an ASCR.

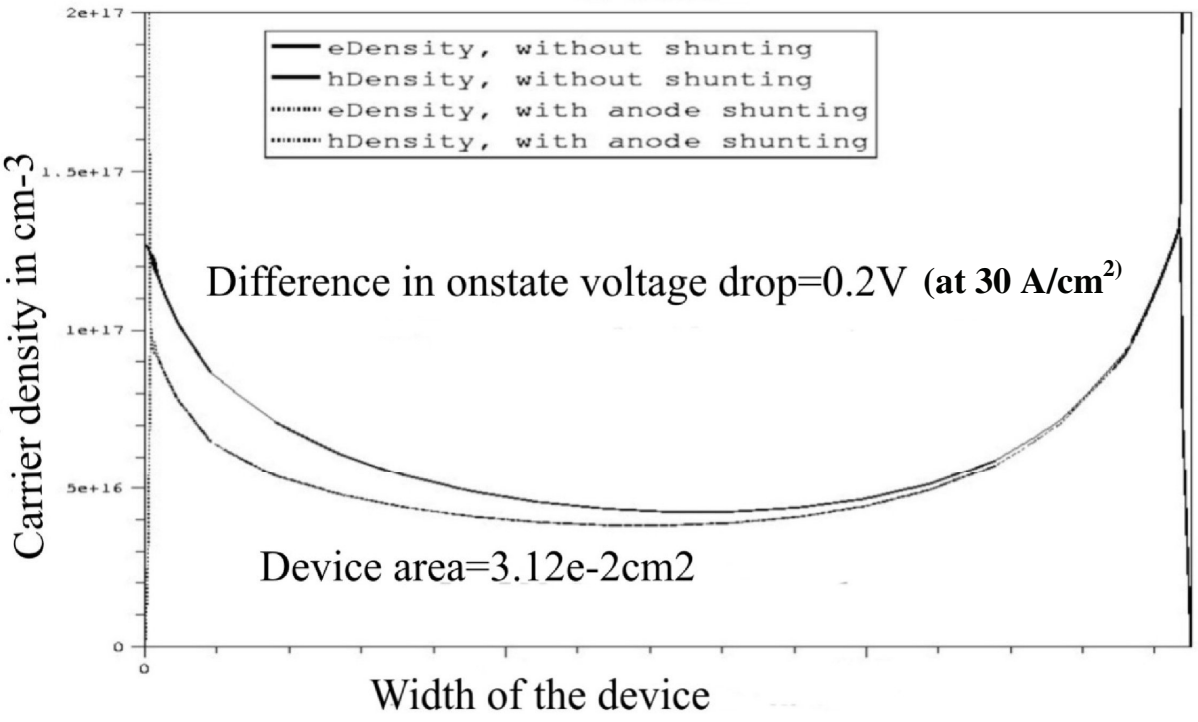


Figure 25 Comparison of plasma concentration between a weakly anode-shunted thyristor and an un-shunted thyristor

6 Lateral resistance between inner and outer AGs, advantages and disadvantages

A protection resistor between AG2 and AG3 is a means to reduce the high temperatures that generate in the optical window and in the inner AG regions during triggering from very high voltages and BOD triggering.

To reduce the temperatures in the thermo-mechanically sensitive regions of a thyristor, one or more of the factors contributing to the volumetric power density, viz. voltage, current, time (trigger delay) have to be reduced. A lateral resistance between AG2 and AG3 reduces the voltage in the thermo-mechanically sensitive optical window and inner AG regions.

A lateral resistance between the inner and outer AGs, shown in Figure 28, (the inner circle comprises the inner AG rings, exterior to the outer circle are the outer AGs and the region in red shows the lateral resistor) is integrated to protect the inner AGs during critical triggering scenarios.

This lateral resistor is conceived by a homogeneous p-type doping. At higher electric fields (above $20\frac{kV}{cm}$), due to velocity saturation of holes, such a resistor exhibits non-linearity which is otherwise purely ohmic (Figure 28).

This temperature dependent, ohmic, lateral resistance is chosen to be 100Ω at 300K and varies with temperature according to the temperature dependence of mobility of holes. The lateral resistance protects the inner AGs by reducing the voltage in the inner AG region but only at the cost of increasing the minimum triggering voltage for the thyristor.

In the device under investigation, AG3 is designed to trigger at 1A. This entails that the minimum trigger voltage of the thyristor is 100V if the protection resistance is 100Ω. Triggering from high voltages may result in highly inhomogeneous temperature distribution across the lateral resistor which create hot spots in the inner radius of the protection resistor. This topic is treated in detail in section 6.1.

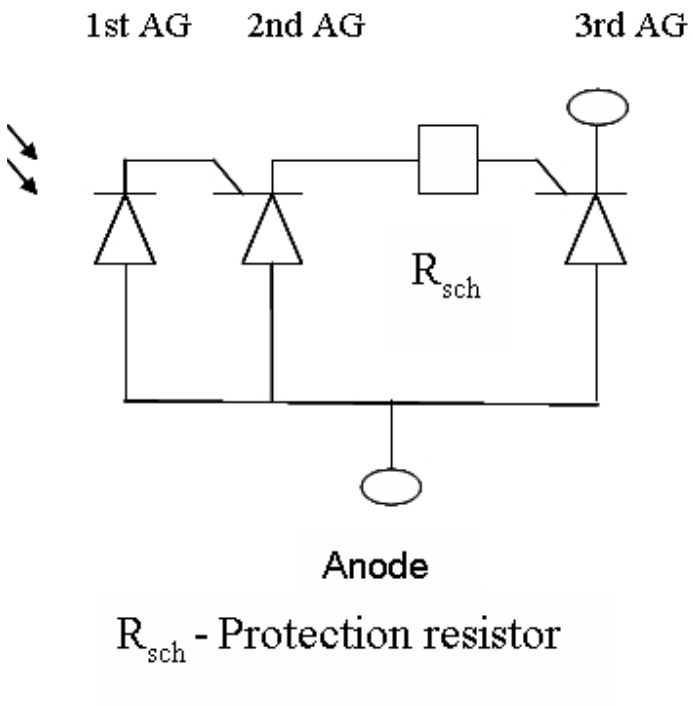


Figure 26 Protection resistor between 2nd and 3rd AGs

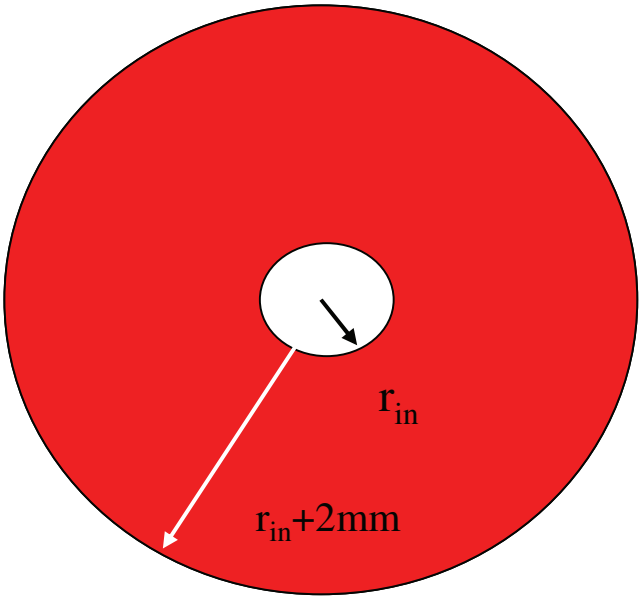


Figure 27 Basic schematic of the radial ohmic resistor

6. Lateral resistance amid inner and outer AGs, advantages and disadvantages

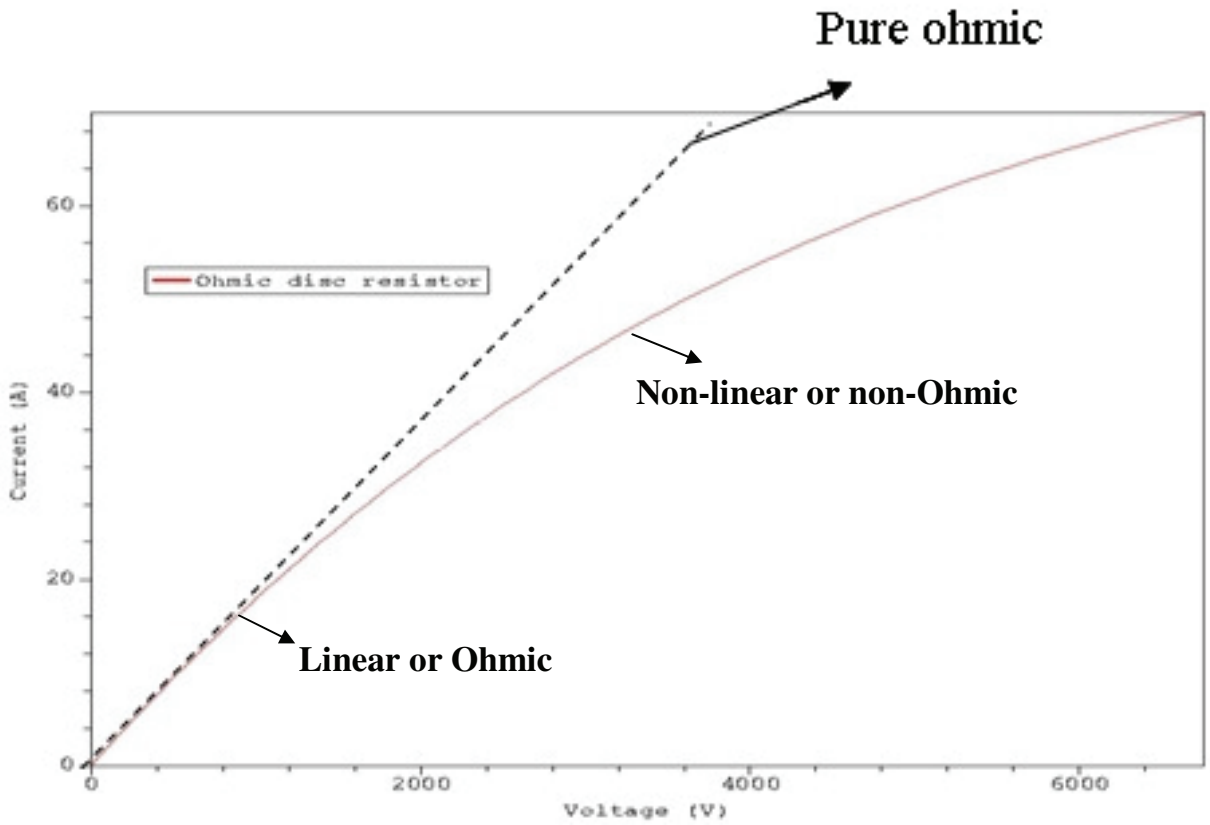


Figure 28 Characteristics of the radial ohmic resistor

6.1 Temperature distribution across the lateral resistance during triggering

Voltage drop across the lateral resistor during triggering results in a lateral electric field. The lateral electric field together with lateral hole current to the outer AGs from inner AGs affect a significant energy drop across the lateral resistance.

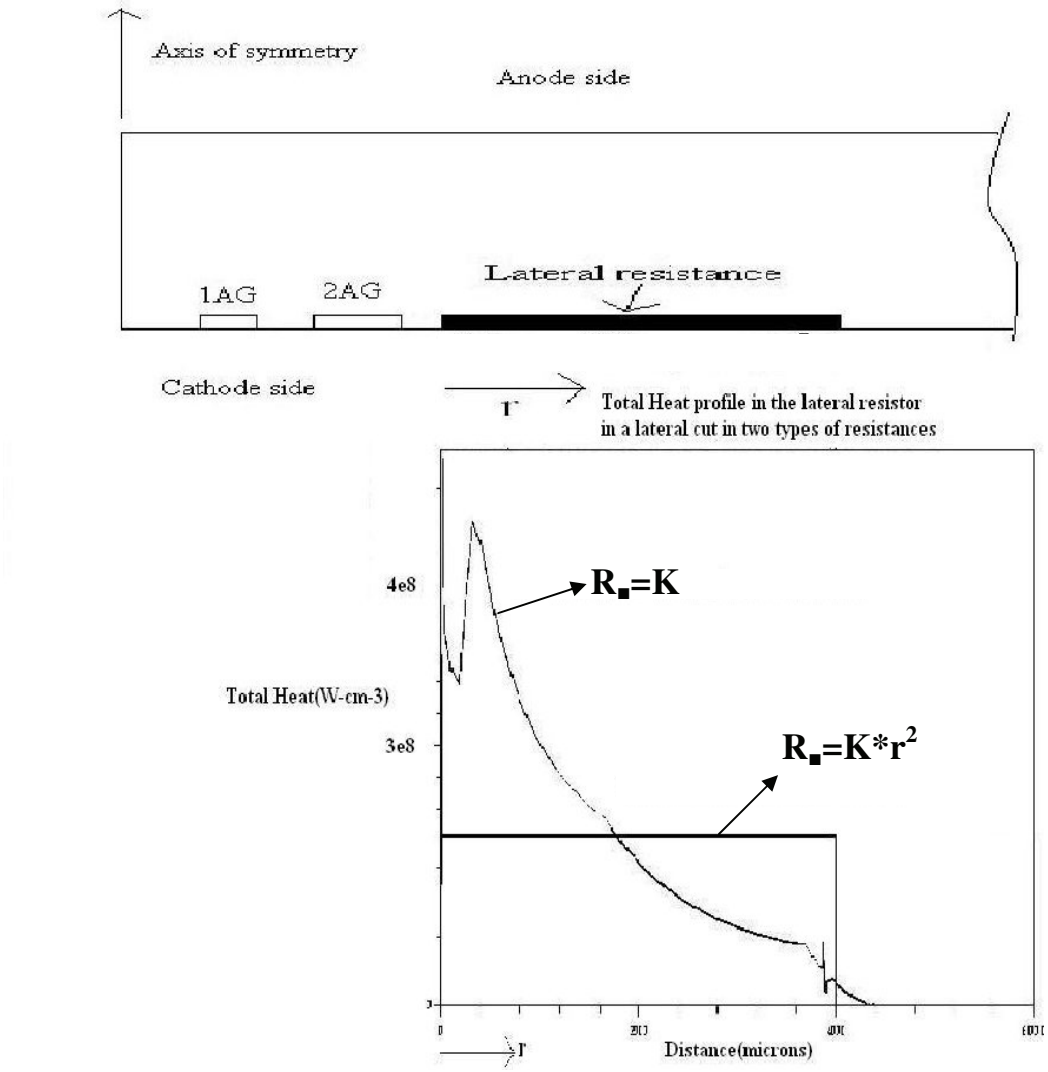


Figure 29 Purpose of the lateral resistor, distribution of heat energy across two different types of lateral resistors,

1. Sheet resistance of the resistance is constant with radius, $R_{\blacksquare}=K$

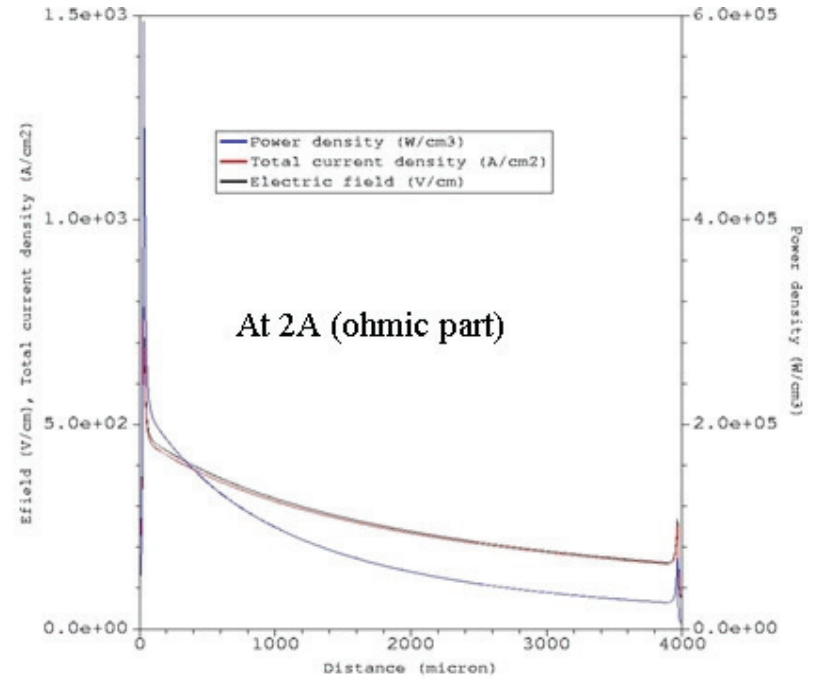
2. Sheet resistance of the resistance is proportional to the radius $R_{\blacksquare}=K*r^2$

It can be seen in Figure 29 that the heat energy is very high in the inner radius of the lateral resistor and decreases with radius if the sheet resistance of the protection resistor is constant with radius ($R_{\blacksquare}=K$). A protection resistor whose sheet resistance is proportional to the square of the radius ($R_{\blacksquare}=K*r^2$) results in a homogeneous heat profile. This suggestion is discussed in detail in chapter 7.

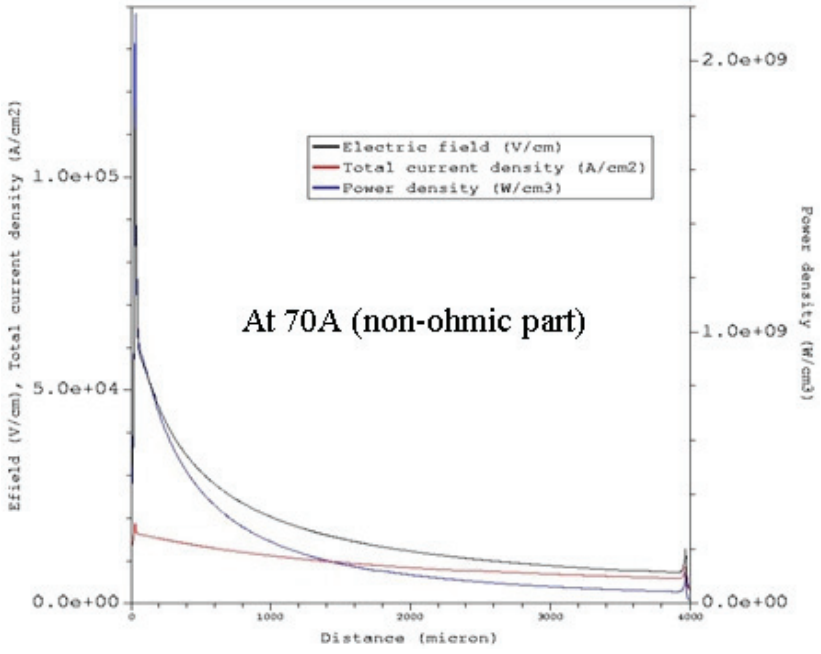
Development of power density with increasing current is investigated for the case of ohmic resistor ($R_{\blacksquare}$=K). Figure 30(a); (b) correspond to the ohmic and non-ohmic regions in Figure 28 of the resistor respectively.

In case of 2A (Ohmic part), electric field and power density are nearly linear across the lateral protection resistor (Figure 30 (a)). In case of 70A (non-Ohmic part), electric field and power density become parabolic (Figure 30 (b)) resulting in a much steeper power density profile in the inner radius of the lateral protection resistor.

From the above simulation results, it is apparent that the electric field and power density increase very steeply in the inner radius of the lateral resistor during its non-ohmic behavior. Such a local high lateral electric field across the lateral resistance may cause hot spots.



(a)



(b)

Figure 30 Electric fields, total current densities and power densities across the radial ohmic resistor when the resistor is acting ohmic and non-ohmic

6.2 Temperature diffused to the inner AGs from the lateral resistance region

The temperature across the lateral resistance diffuses to the inner AGs and consequently increases the net temperature in the inner AGs. For that reason, it is important to inspect how high the diffused temperature from the lateral resistance to the inner AGs is.

The maximum temperature point in the lateral resistance is located in the inner radius region of the lateral resistance purely due to higher electrical and thermal resistance of the inner radius region as shown in Figure 31. The temperature profile across the lateral resistance after one pulse of forward break over voltage is shown in Figure 32(a).

The profile of the temperature that diffused from the lateral resistance to the inner AGs is shown in Figure 32(b). The supplementary temperature diffused to the center of the device due to the temperature distribution in the lateral resistance is tolerable for one pulse of over-voltage or BOD triggering. In case of multiple over voltage or BOD triggering events which can take place in AC converter operation, the supplementary temperature diffused to the inner AGs from the hot-spot of the lateral resistor can be convoluted and may result in critically high temperatures over time.

The temperature diffused to the inner AGs as a result of a 50Hz over-voltage pulse in 3sec, which in other words 150 over-voltage triggering pulses with a 20msec time difference is calculated. Since simulation of a high voltage device for 3sec ca is lengthy, this calculation had to be done analytically (problem of convolution).

Convolution of temperature in the inner AG regions for 150 over-voltage pulses with a 20msec time difference results in a 20K increase in temperature in the center of the device, which is within the tolerable limits. Hence, it can be said that hot-spot in the lateral resistance does not increase the temperature in inner AGs critically.

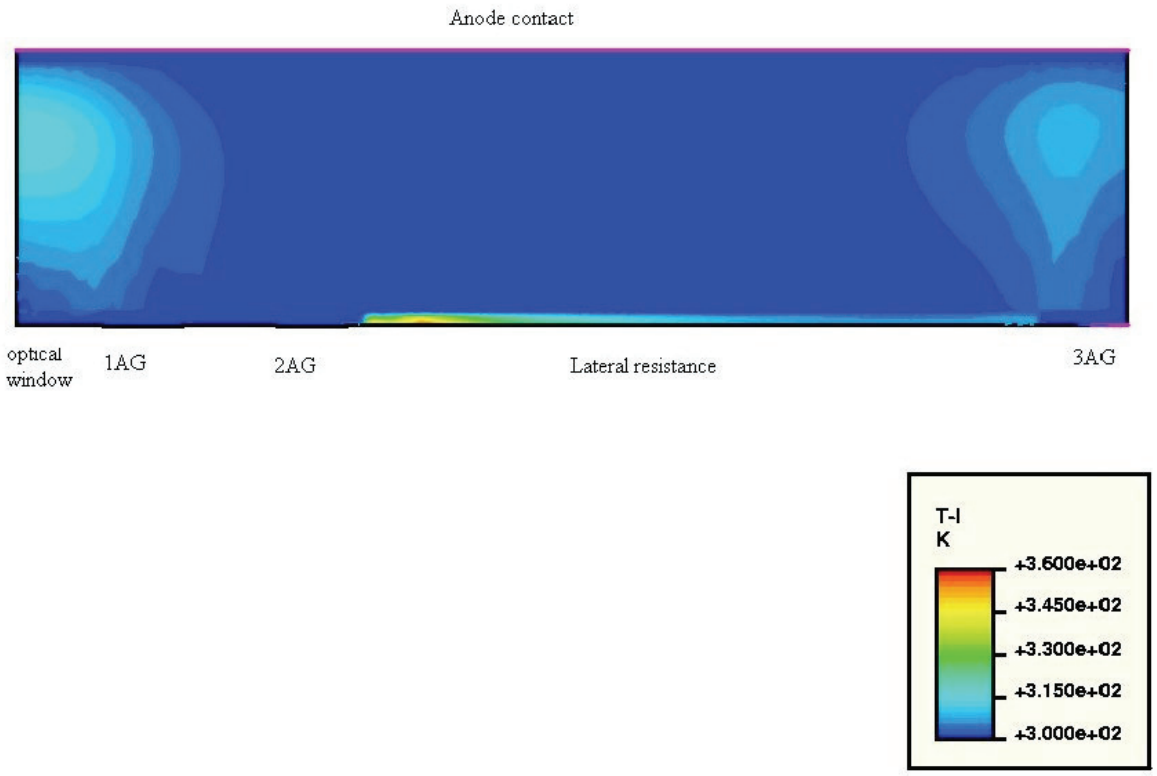
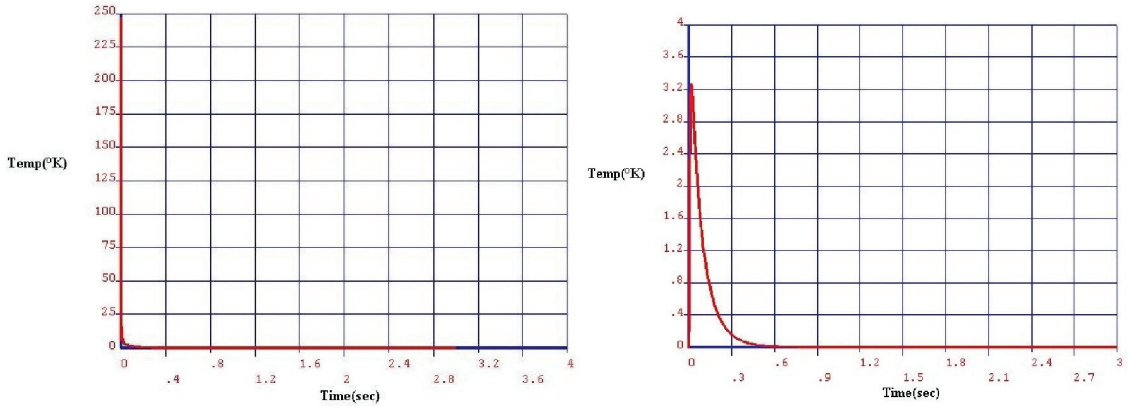


Figure 31 Distribution of temperature across the lateral resistor with emphasis on the maximum temperature point



(a) **(b)**

Figure 32 (a) Temperature at the hottest spot (inner radius) in the lateral resistor after one BOD pulse

(b) Temperature profile of the diffused temperature to the inner AGs after one BOD pulse

7 Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs

(" $R_{\blacksquare}$ "- sheet resistance of the p-base and "r" - radius from the center of the device, "K" - proportionality constant)

Although a lateral ohmic protection resistor protects the inner AGs from high temperatures by reducing the voltage in the inner AGs, it inflicts the following consequences.

1. High minimum trigger voltage of the thyristor
2. Inhomogeneous distribution of heat across the lateral resistor

If the application demands a lower minimum trigger voltage and if the inhomogeneous heat distribution across the lateral resistor is unacceptable (for e.g. due to hot spots), a complementary design of the lateral resistor is proposed with the following aims.

- Protection of the inner AGs in over-load conditions (high di/dt triggering, BOD or triggering from very high voltages)
- Low thyristor triggering voltage (around 100V)
- Homogeneous heat distribution across the lateral protection resistor
- Avoid any negative resistance behavior (snap-back in I-V characteristics) in the working region of the protection resistor

Ideal I-V characteristic of such a resistor is shown in Figure 33.

1. Low resistance at low voltages and high resistance at high voltages (necessary to reduce the temperature development in the inner AG region and at the same time allow the thyristor triggering from a low voltage.)
2. No snap-back after the voltage break down (necessary to protect the lateral resistance from current localization which may cause high temperature spots)

The basic design of the new resistor is shown in Figure 34. The inner white circle comprises the optical window, AG1, AG2 and outside of the red disc comprises AG3, AG4 and the main cathode area. The etching design of the p^+-p^--p^+ ring is shown in Figure 35 and the diffusion and implantation profiles are shown in Figure 36. The functionality of such a structure is studied in detail in section 7.1.

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs

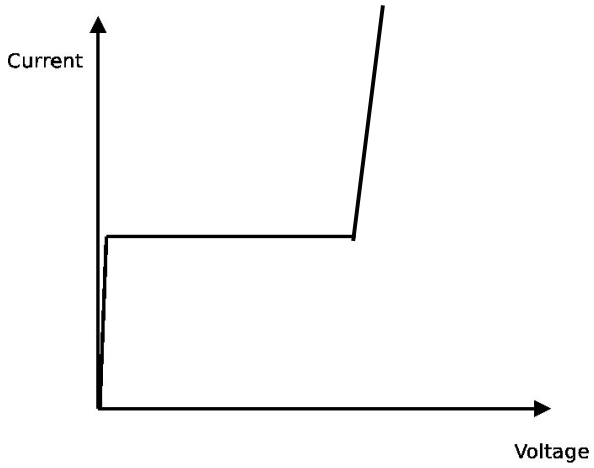


Figure 33 Ideal I-V characteristics of the non-linear resistor

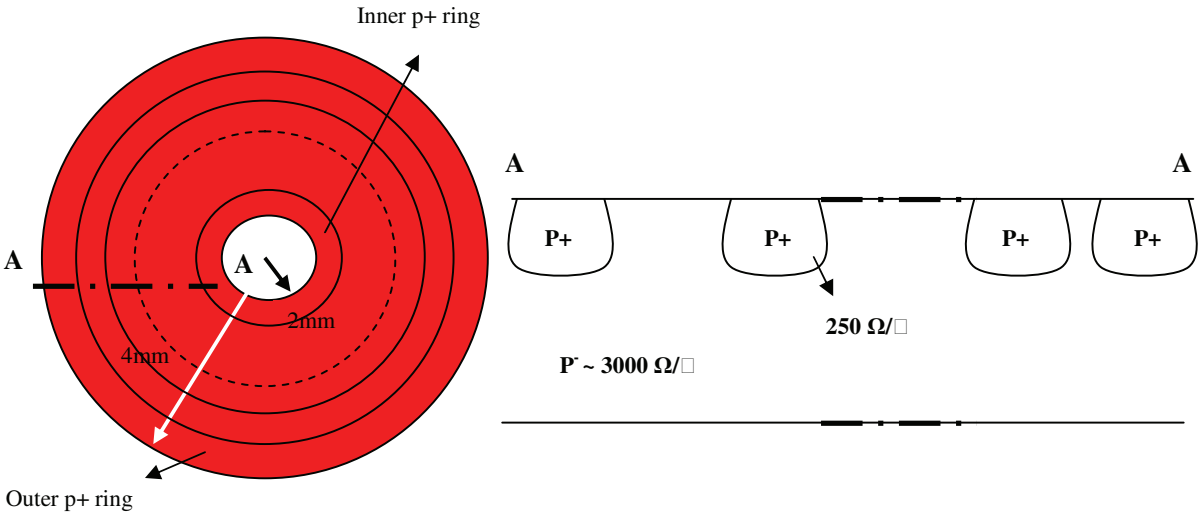
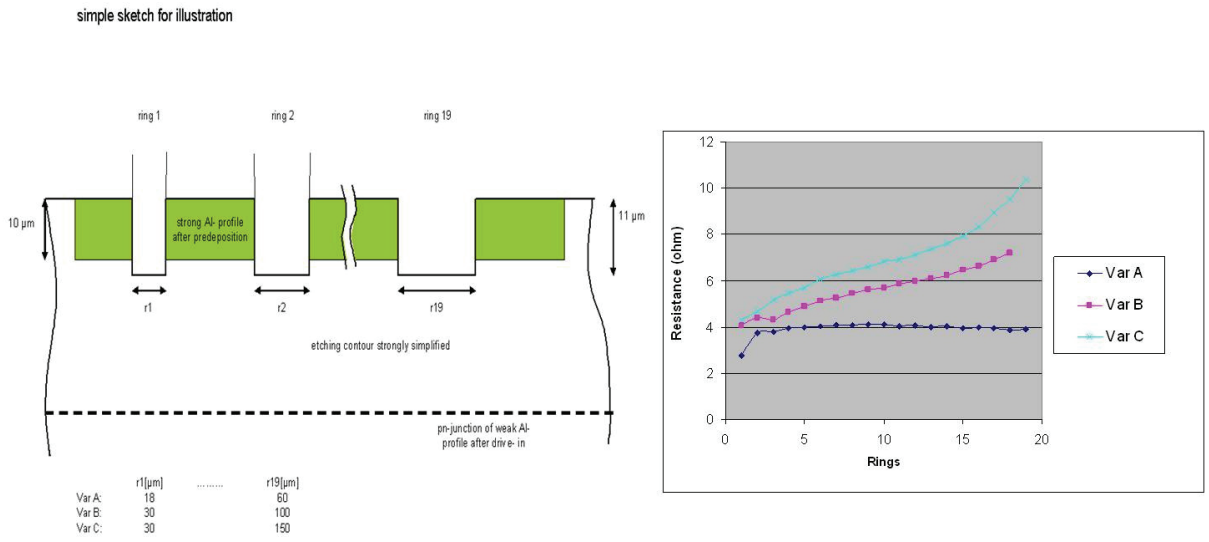


Figure 34 Schematic of the new resistor design

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs



(a) **(b)**

Figure 35 **(a) Etching design of the new resistor**

(b) Resistances of each p^- region in 3 different etching profiles

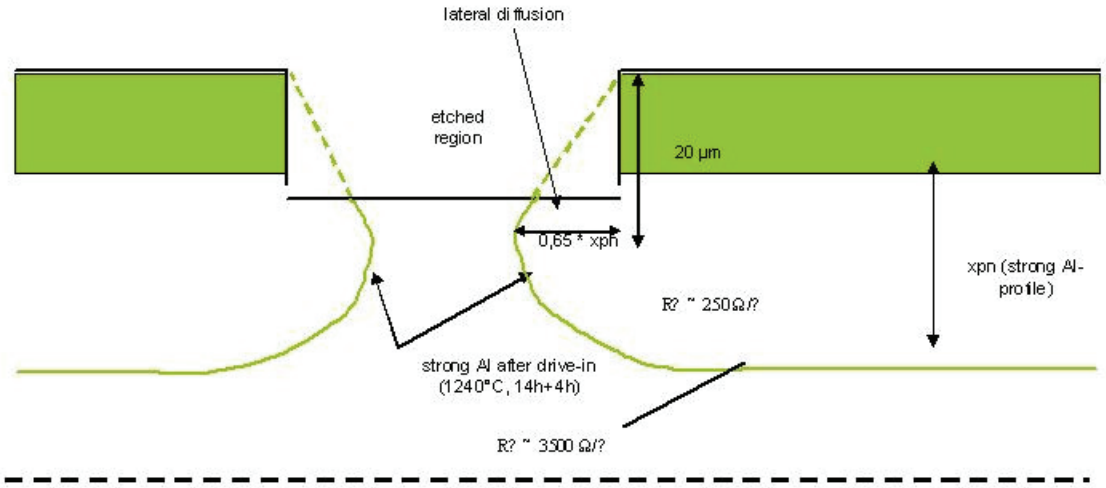


Figure 36 **Structure of a p^+-p^- -p^+ after Al implantation (p^-) and Boron diffusion (p^+)**

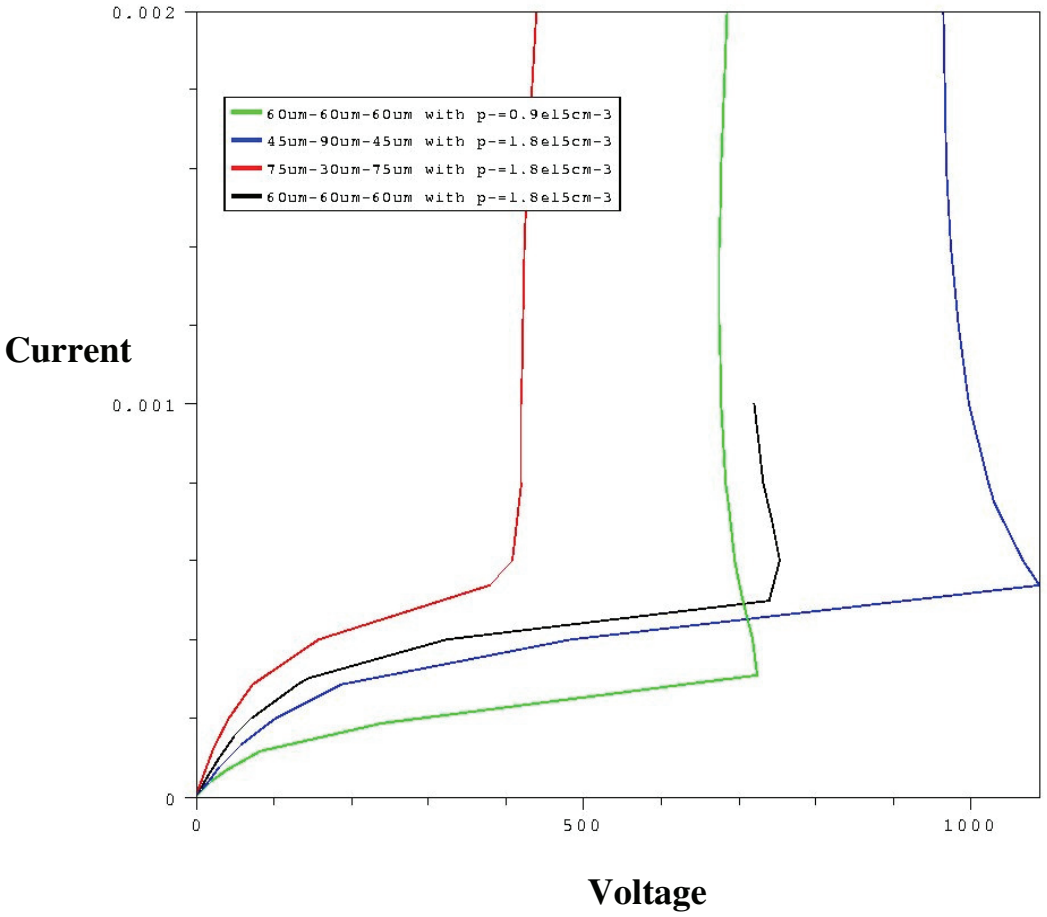
7.1 Functionality of a p^+-p^- -p^+ structure

Simulations are done to analyze the I-V characteristics of a p^+-p^- -p^+ structure. Figure 37 (a) shows the simulated I-V characteristics of a p^+-p^- -p^+ structure for different dimensions and p^- doping concentrations. Figure 37 (b) shows the characteristic segments in a typical I-V characteristic of a p^+-p^- -p^+ structure.

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs

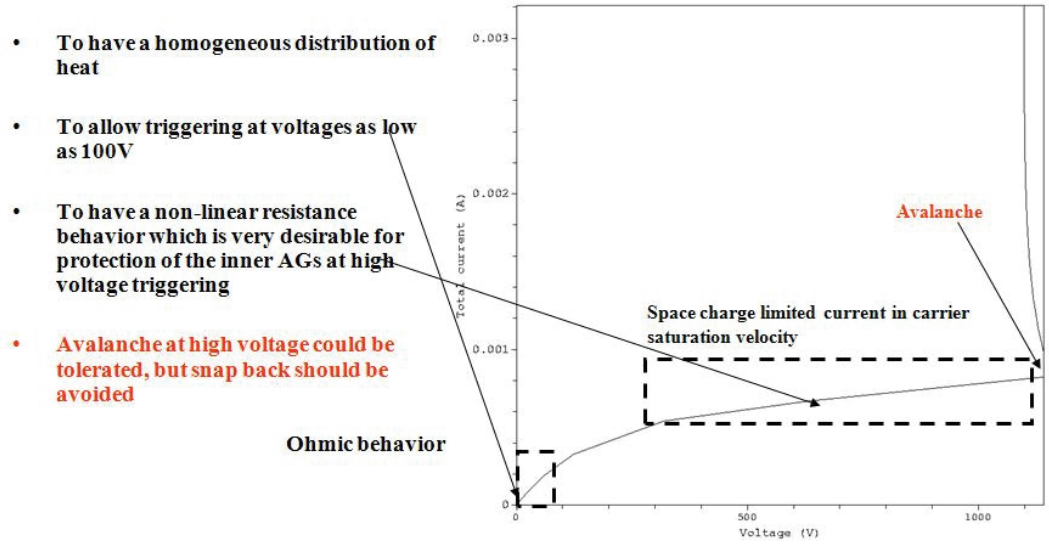
I-V characteristics of a p^+-p^- -p^+ structure can be segmented into 3 parts.

1. Linear part which is due to the ohmic behavior of the p^- region
2. Current saturated region which can be explained as a combination of space charge limited current and velocity saturation of holes.
3. Avalanche breakdown part when the ionization integral reaches unity and the current increases steeply for a small change in voltage.



(a)

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs



(b)

Figure 37 (a) Simulated I-V characteristics of a p^+-p^--p^+ structure

(b) Description of 3 regions in the I-V characteristics of a p^+-p^--p^+ structure

7.2 Achieving non-linear resistance

The first aim of the new design of the lateral resistance is to achieve a non-linear resistance (very low resistance at low voltages and high resistance at high voltages). The purpose of such resistance is to protect the inner AGs from high temperatures and still be able to trigger the device from low voltages. The ideal I-V characteristics expected from such a non-linear resistor is shown in Figure 33.

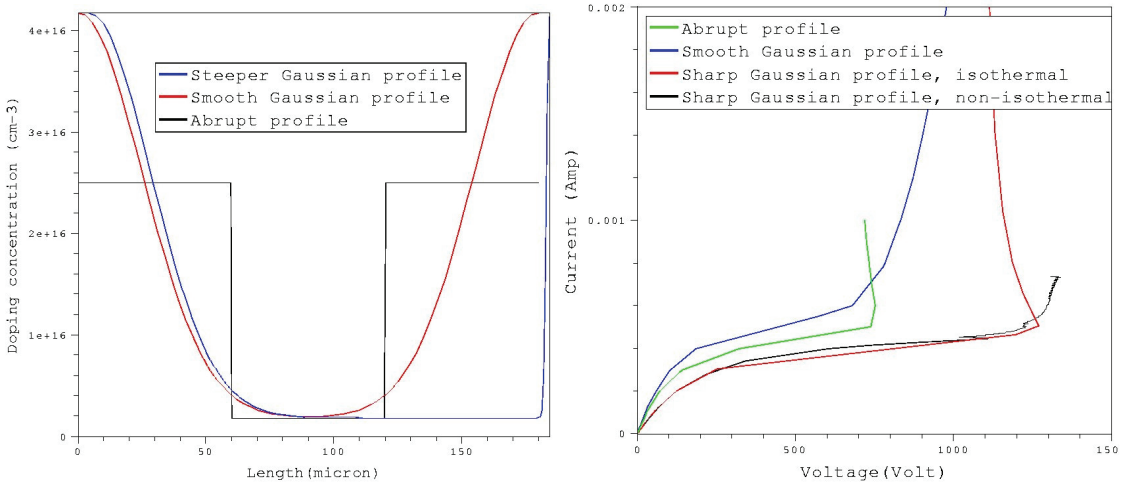
Such a non-linear resistor provides low minimum trigger voltage due to its low resistance at low voltages and currents and at the same time provides safety to the optical window and the inner AG regions at high voltages due to its high resistance at higher voltages and currents.

Although the new design of the lateral resistance offers the characteristics that are demanded and can also be easily integrated in the LTT with the current state-of-the-art processing technology due to the simplicity of the design, it poses new problems when the device operates at high current densities.

Simulations are done on a simple p^+-p^--p^+ structure to investigate the current-voltage behavior of such a structure at high current densities.

Different p^+-p^--p^+ structures are investigated to understand the influence of different parameters of p^+-p^--p^+ structures on their I-V characteristics. Three basic prototypes of these profiles are shown in Figure 38 (a). I-V characteristics of these structures are shown in Figure 38 (b).

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs



(a) **(b)**

Figure 38 (a) Investigated p^+-p^- -p^+ structures (b) I-V characteristics of the investigated p^+-p^- -p^+ structures

The most important observation to be made is the difference between the I-V characteristics when the profiles vary with respect to the type of the junction. It can be clearly seen that the abrupt profile and the sharp Gaussian profile have shown a snap-back behavior (negative resistance) in I-V characteristics at high current densities where as the smooth Gaussian profile doesn't.

Such a snap-back shall be avoided since it can inflict current filamentation in the device and possibly consequent device destruction when the device is operating at high current densities. Different p^- widths and p- doping concentrations are simulated varying the type of the junction.

I-V characteristics of all abrupt and sharp Gaussian profiles have a similar shape. But in the case of smooth Gaussian profiles, no snap-back after the avalanche break down is observed. To understand this important and interesting difference in I-V characteristics when the pp^- junction becomes sharper, one should have a look at the electric field profile development with voltage for a smooth Gaussian and abrupt profiles (Figure 39).

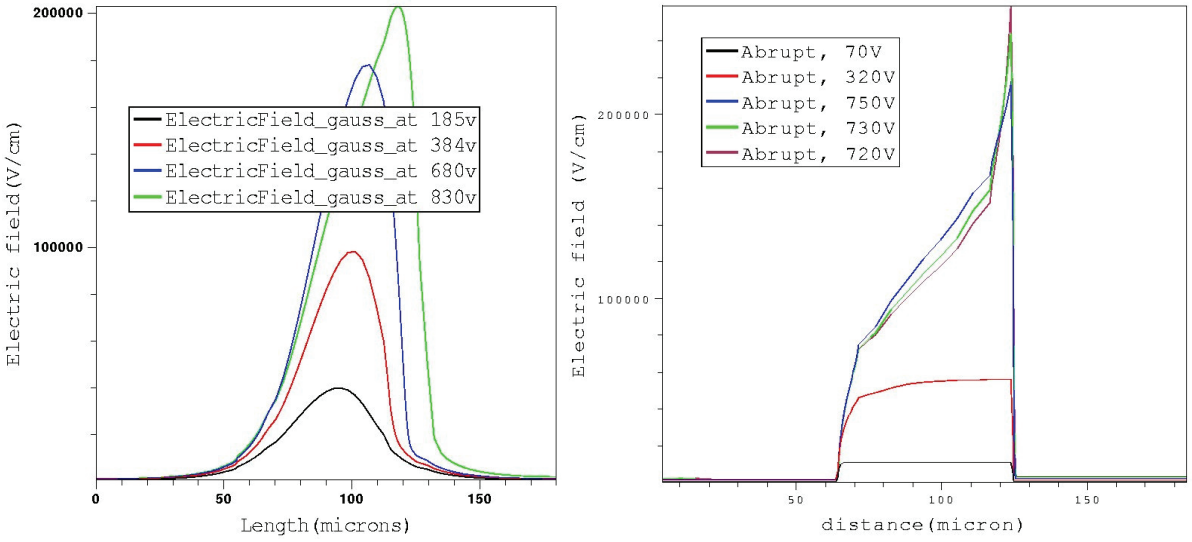
In case of an abrupt profile, the electric field peak is narrower and mainly limited very close to the junction unlike smooth Gaussian profile. When the impact-ionization integral is very close to unity, electrons generated due to impact ionization flow towards left side (to the reader), i.e. towards positive polarity, resulting in a higher electron concentration on the left side of the junction than on the right side. This electron concentration compensates the ionized acceptor concentration in the space charge region reducing the height of the electric field in the p^- region.

If the reduction of height of the electric field in the p^- region results in a reduction in spatial integral of the electric field and thereby a lower voltage across the device, a snap-back in the I-V

characteristics shall be observed. If the reduction in the height of the electric field is too low to result in a lower voltage, a snap back shall not be observed.

In the simulated structure, the drop in the height of the electric field results in a reduction in the total voltage across the device which is reflected in the observed snap back. This phenomenon can be named as "half-Egawa" (Description of this effect is given in Appendix B). In case of a smooth Gaussian profile, electric field is distributed over a larger volume unlike in case of an abrupt profile. Although an avalanche breakdown occurs at high current densities also in this case, a "half-Egawa" phenomenon doesn't take place in this case and thus no snap-back is observed. Hence, a smooth Gaussian profile is a superior solution for the design of the new lateral resistance.

However it is interesting to find out the influence of temperature on the snap-back particularly for the case when thyristors with the new resistor design are connected in parallel to each other. Results of this course of investigation are presented in section 7.5.



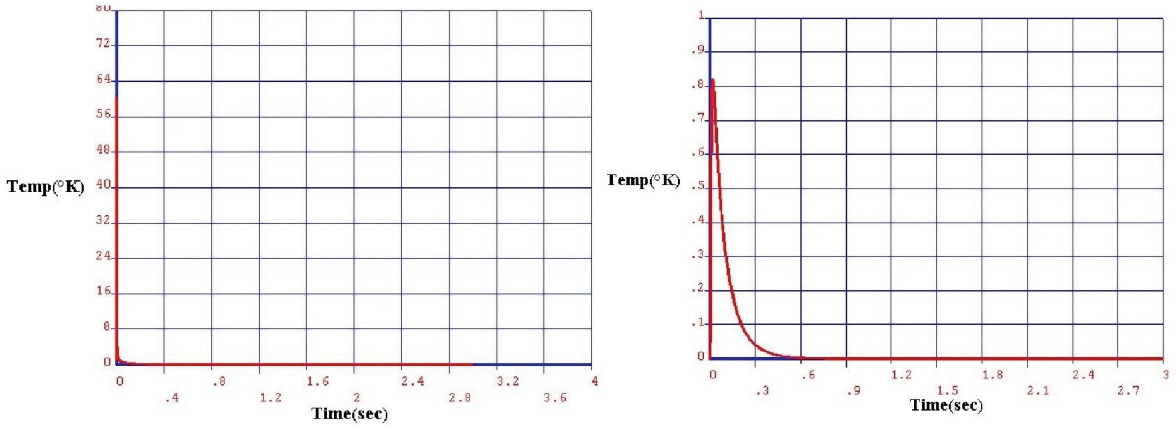
(a) Gaussian junction **(b) Abrupt junction**

Figure 39 Comparison of development of electric field with current in Gaussian and abrupt p^+-p^--p^+ structures

7.3 Achieving homogeneous temperature distribution across the lateral resistance.

It is shown in section 6.1 that in the case of homogeneously doped ($R_{\blacksquare}=K*r$) lateral resistance, temperature distribution is inhomogeneous which caused in a high temperature spot in the inner radius of the lateral resistance.

The new design of the lateral resistance prevents high temperature spots in the lateral resistance. By designing the lateral resistance according to the rule $R_{\blacksquare}=K*r^2$, heat energy is distributed homogeneously across the lateral resistance and it results in 4 times lower temperature peak than the homogeneously doped lateral resistor (Figure 29). The proof is given in APPENDIX A.



(a) **(b)**

Figure 40 Illustration of diffused temperature to the inner AGs from the lateral resistor with the new design

The result is a better protection to both the lateral resistance region and the inner AGs region. As shown in Figure 40(a) (compare to the maximum temperature in Figure 32 (a)), the maximum temperature which is homogeneously distributed across the lateral resistance is 4 folds lower than that of the previous design ($R_{\blacksquare}=K*r$) of the lateral resistance. In Figure 40 (b), one can see that the diffused temperature to the inner AGs from the new design of the lateral resistance after 150 BOD pulses with 50Hz frequency is negligible.

7.4 Functionality of the total radial resistor including a series of p^+-p^- -p^+ rings

The total radial protection resistor between AG2 and AG3 includes a series of p^+-p^- -p^+ rings with increasing p^- widths with increasing radius to realize a resistor whose sheet resistance increases according to $R_{\blacksquare}=K*r^2$.

The radius of the total resistor disc is approximately 4mm divided into approximately 20 p^+-p^- -p^+ rings with increasing p^- width with radius. The voltage blocked by a p^+-p^- -p^+ ring increases with the increase of the p^- ring width. For the sake of analysis, 3 variations with different realistic p^- widths (Wp^-) with a p^- doping concentration of $1e15cm^{-3}$(equivalent to 14 $\frac{\Omega}{cm}$ are simulated (Figure 41).

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs

A quasi-stationary simulation for a given current is performed and the current - voltage behavior is observed. Figure 42 shows the $\frac{current}{length}$ Vs. Voltage of these 3 variations.

Rings with 60µm, 100µm, 150µm p^- widths represents rings belonging to the inner, middle and outer radius of the resistor disc respectively.

As it can be seen in Figure 42, the rings with p^- widths of 60µm, 100µm, 150µm block 300V, 700V, 1100V respectively before reaching avalanche breakdown. The y-axis here represents $\frac{current}{length}$. To calculate the approximate total current, the $\frac{current}{length}$ value shall be multiplied with the intermediate length of the ring. These multiplication factors are noted in the Figure 42 for each ring.

One should bear in mind that at a given current, each of these rings will be at different $\frac{current}{length}$ values according to the ratio of their ring circumferences (Figure 43).

Following deductions can be made from Figure 43:

- At low current densities (all the rings operating in their ohmic region indicated by the blue dots), power density is homogeneously distributed over all the rings.

- At medium level current densities (some or all of the rings operating in the current saturated part indicated by green dots), power density is in-homogeneously distributed over the rings. Inner rings reach avalanche breakdown prior to outer rings at a given current value. Thereby, inner rings tend to be hotter than outer rings at a given current.

- At high current densities (indicated by red dots), all the rings operate in the avalanche breakdown region. After avalanche breakdown, outer rings tend to have a snap-back in their I-V characteristics. Thereby, current localization is possible in the outer rings.

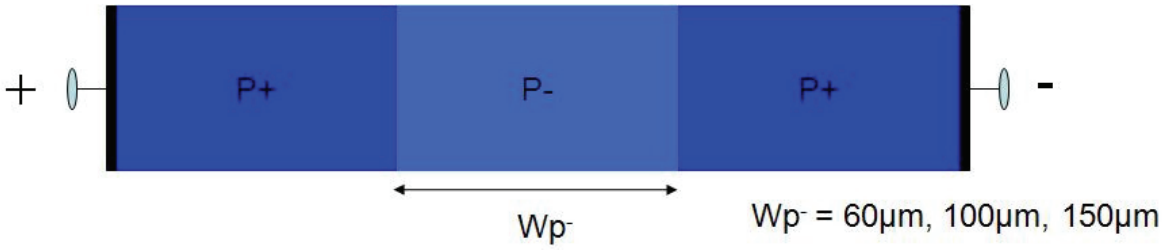


Figure 41 Simulated p^+-p^--p^+ structures

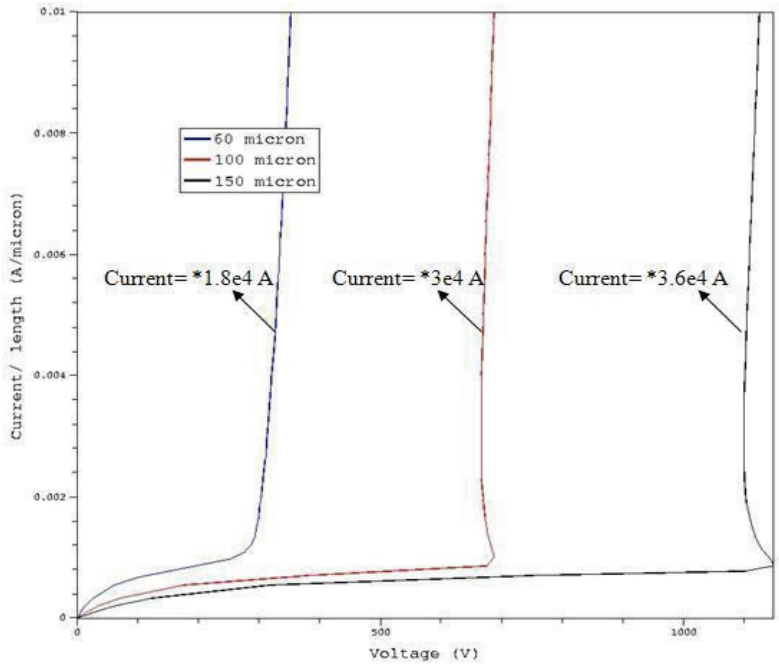


Figure 42 $\frac{current}{length}$ **vs. voltage characteristics of 3 p^+-p^--p^+ structures with different p^- widths, current=** $\frac{current}{length} * p^- width$

- **9A total current. Ohmic region (constant power density in all rings)**
- **18A total current, saturated carrier velocity, space charge limited current**
- **36A, Avalanche situation**

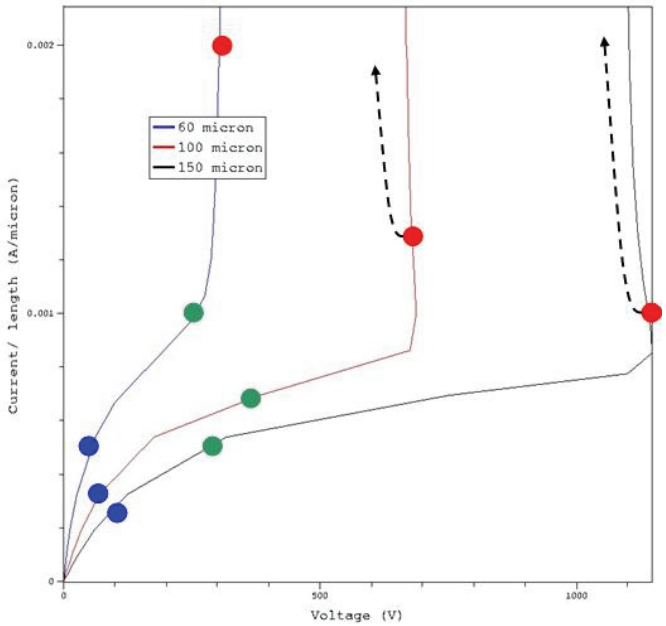


Figure 43 $\frac{current}{length}$ **in each ring at a given current**

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs

To understand the importance of avoiding snap-back in outer rings, simulations are done to depict the increase of power density in the outer ring compared to the inner ring as $\frac{current}{length}$ increases.

In Figure 44, it can be seen that the peak power density at a given $\frac{current}{length}$ is nearly the same in 60 µm and 150 µm cases. Figure 45 shows the comparison of power densities at a given current in 60 µm and 150 µm cases. Green dots represent current before avalanche breakdown where as red dots represent current after avalanche breakdown.

Following deductions can be made from Figure 45:

- Peak power density is higher in 60µm ring (representing inner rings) compared to 150µm ring (representing outer rings) at a given current.
- After snap-back in the outer ring, the power density increases very rapidly to a very high value in the outer ring.
- The region of power density peak becomes narrower after snap-back indicating a hot spot as a result of half-Egawa effect (refer to Appendix B).

Figure 46 shows the distribution of temperature in the outer ring of the resistor disc with increasing current. When the outer ring is in the Ohmic region, heat is distributed homogeneously through out the ring. In the non-Ohmic region, electric field increases steeply with radius resulting in an increasing temperature profile with radius. At avalanche break down, a “half-Egawa” effect is observed and results in high temperatures in the outer most part of the ring (represented by “before snap-back” in Figure 45). After snap-back, due to negative resistance characteristic, heat is crowded to a weak point (in case of a p^+-p^--p^+ structure, a slightly higher p^- doping concentration at a point in the ring can be a weak point) in the outer-most part of the ring resulting in a hot-spot.

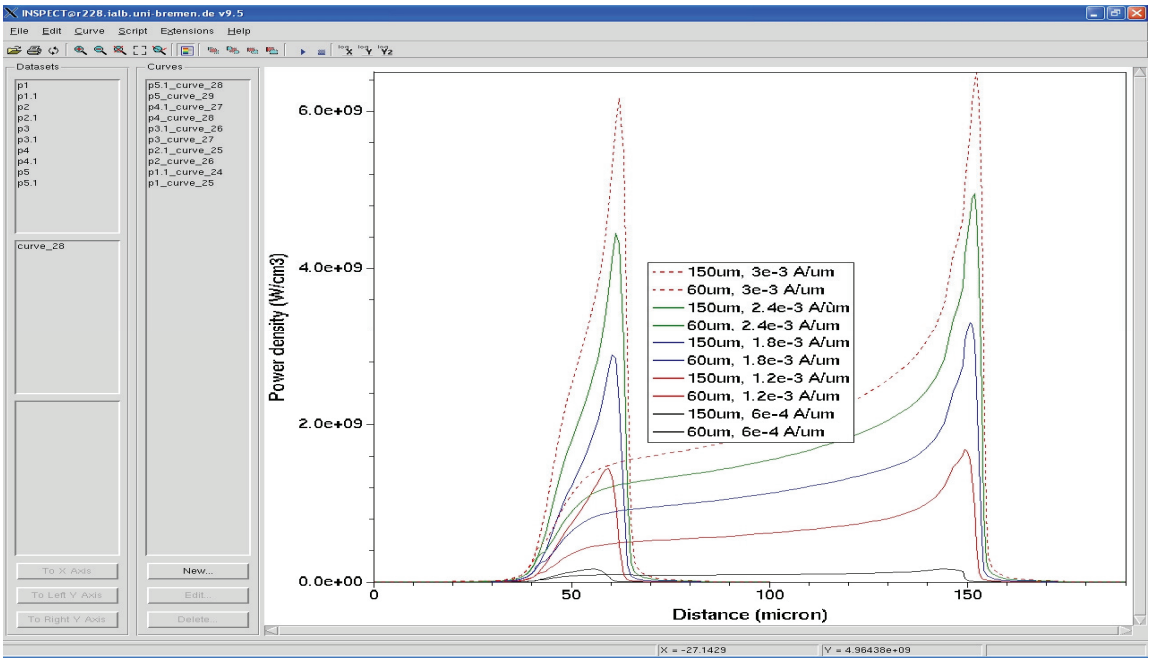


Figure 44 Comparison of development of power densities in 60µm, 150µm rings with increasing $\frac{current}{length}$

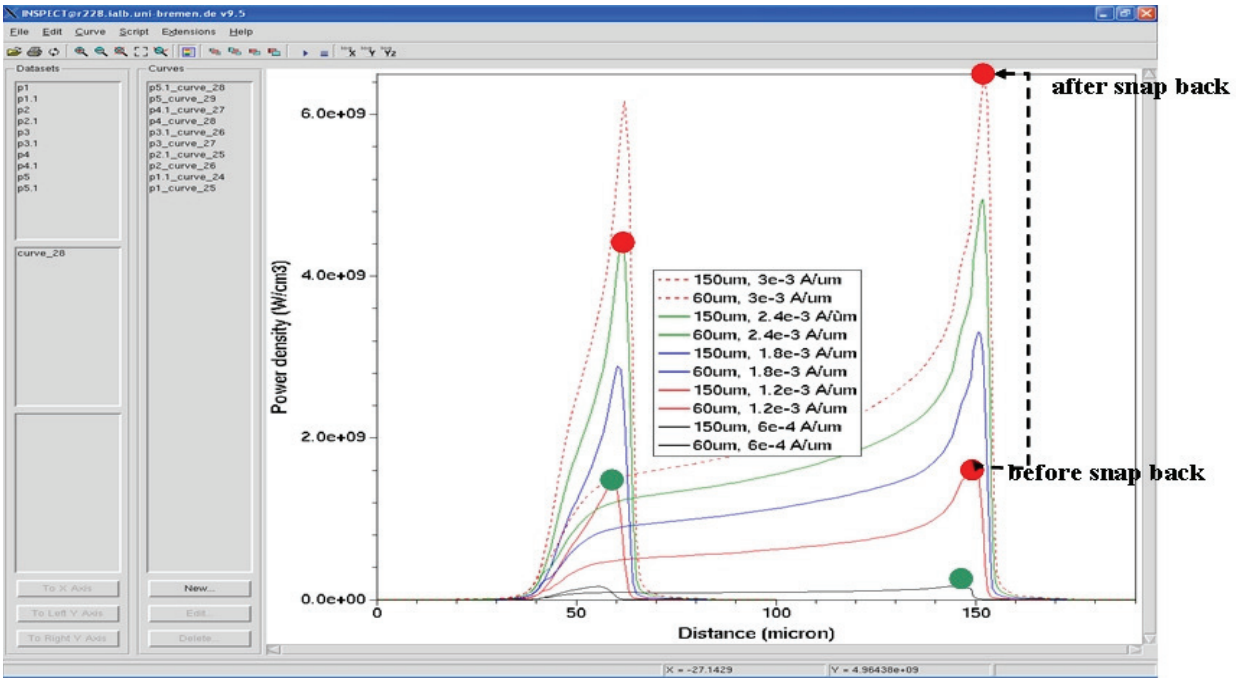


Figure 45 Comparison of power densities in 60µm and 150µm rings at a given current

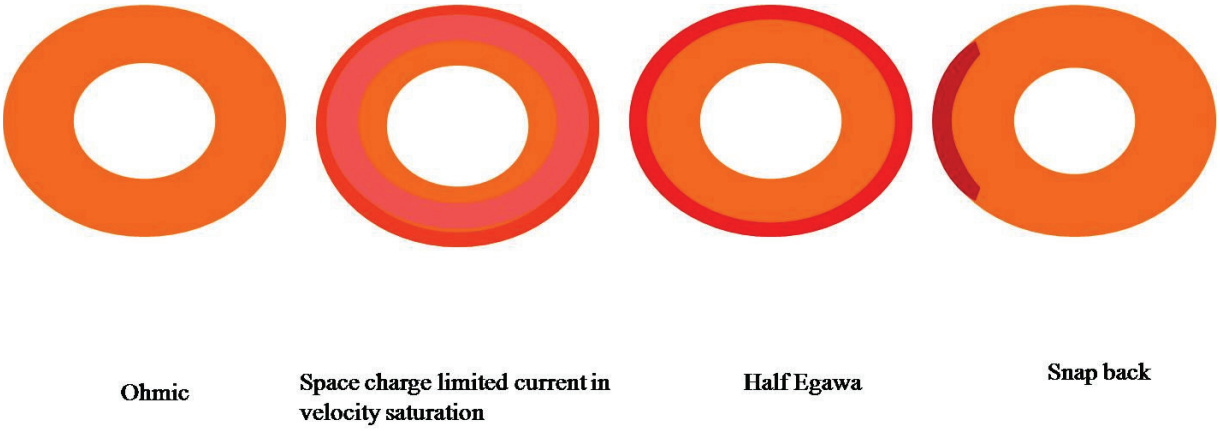


Figure 46 Pictorial representation of the temperature distribution in the outer ring at different points in the I-V characteristics

7.5 Critical issues in the ring-sequence protection resistor

- From non-Ohmic region in the I-V characteristics, heat is mainly concentrated in the outer radius of each ring leading to a non-homogeneous heat distribution within each ring which means that there exists a sequence of hot-spots in the ring-sequence protection resistor disc.
- The outer rings exhibit a half-Egawa behavior leading to a negative resistance behavior.

7.6 Consequences of a snap-back

- In general any negative resistance behavior (seen as a snap-back in I-V characteristic) can lead to current localization or in other words current crowding. In this particular case of p^+-p^--p^+ ring sequence resistor, a snap-back (which can lead to thermal run-away) is possible in the outer most p^+-p^--p^+ ring at high current densities where an avalanche break down occurs.
- Current can re-distribute itself across the ring homogeneously after reaching the positive slope (positive differential resistance) after snap-back in the I-V characteristics. This means, how strong the snap-back is can also play a role on the temperature development due to snap-back.

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs

7.7 Avoiding snap-back in a p^+-p^- -p^+ structure

The electric field peak (where the impact ionization is the strongest) in a p^+-p^- -p^+ structure is at the outer p^- -p^+ junction where p^+ is positively biased compared to p^-. Smoothening (reducing 3D curvature) of the electric field profile in its peak region reduces impact ionization and delays avalanche break down. Even after the avalanche break down, the number of carriers generated due to impact ionization is lower due to less denser electric field vectors (**APPENDIX C**). This means, the number of electrons generated due to impact ionization which reduce the height of electric field in the p^- region are lower.

Therefore with increasing current, the area of electric field in p^- region may slightly reduce but the electric field in p region (Figure 47 (a)) will increase in area. If the net area of the electric field reduces with current, a snap back is observed and vice versa. Hence, the tendency towards a snap-back can be reduced by introducing a p-buffer region to smoothen the electric field peak at the p^- -p^+ junction as shown in Figure 47.

A p^+-p^- -p^+ structure with a p-buffer before the outer p^+ is simulated with the aim of avoiding snap-back in case of voltage breakdown. Variation of Lateral Doping (VLD) of Stengl and Gösele (Reference 15) can be employed to create an increasing effective p-doping concentration (Figure 47). With this technique, using the same p-diffusion and by shortening the distances between the p-diffusion masking holes, a smoothly increasing effective p-doping concentration can be achieved.

Simulation of such a p^+-p^- -p^+ structure (Figure 48) doesn't show a snap-back in case of voltage break-down.

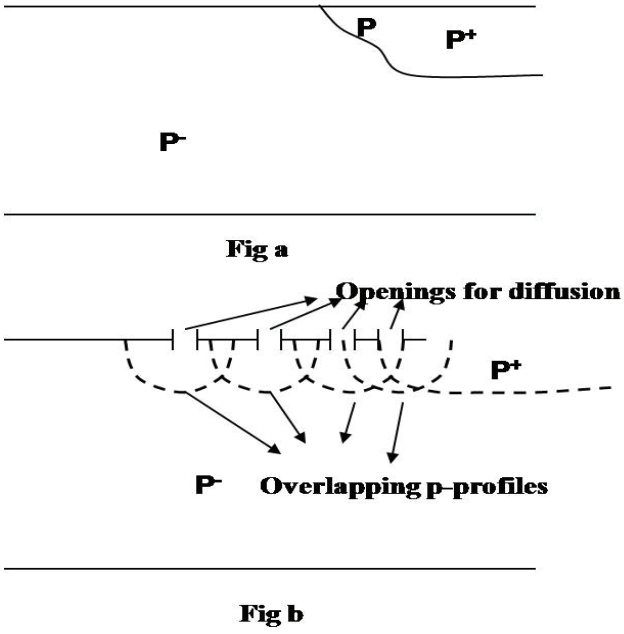
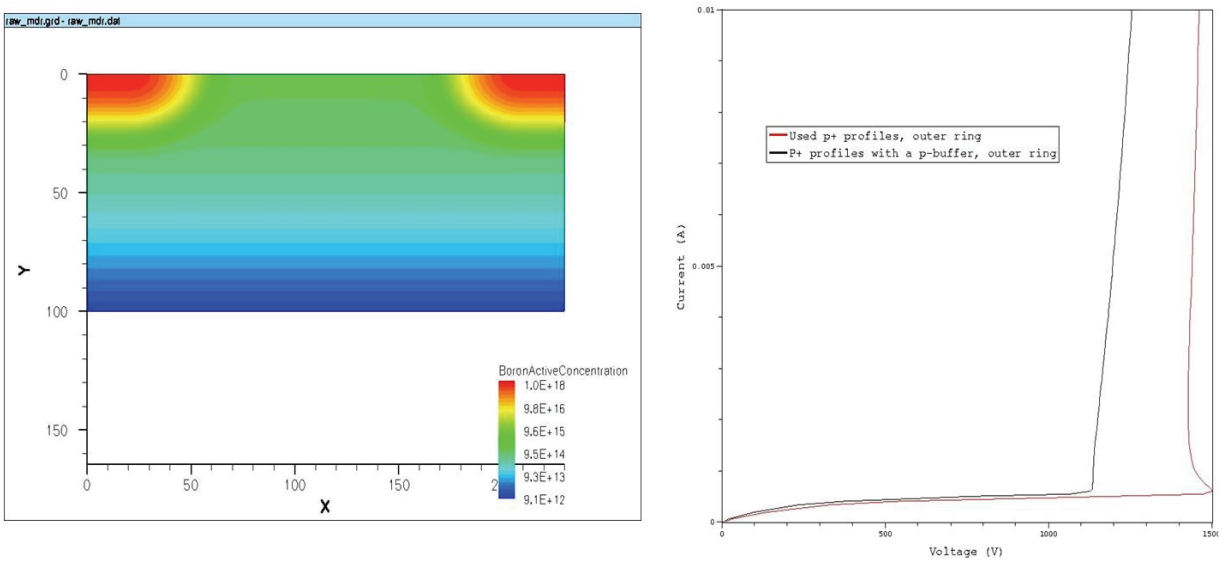


Figure 47 Schematic of a p^+-p^- -p^+ structure with p-buffered p^+ regions

7. Complementary design of the lateral resistance ($R_{\blacksquare}=K*r^2$) between the inner and outer AGs



(a) **(b)**

Figure 48 **(a) simulated p^+-p^- -p^+ structure with p-buffered p^+ regions**

(b) I-V characteristics of p^+-p^- -p^+ structures with and without p-buffered p^+ regions

8 Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

The new design of the lateral resistance ($R_{\blacksquare}=K*r^2$) is not good enough to reduce the minimum thyristor triggering voltage to the order of typical on-state voltage of a thyristor. Although the new lateral resistance exhibits non-linear behavior, the resistance of the low voltage region is still Ohmic. This means that the new lateral resistance serves well in providing a higher resistance at the high voltages, thereby protecting the inner AGs better. But it is not any better in reducing the minimum triggering voltage of the thyristor compared to a purely Ohmic resistor. The ideal non-linear resistance is supposed to exhibit a much lower resistance. A few different approaches in solving this problem are modeled and investigated.

All these ideas try to achieve a single objective, i.e. to reduce the temperature in the inner AG region by reducing the current in the inner AGs with out a lateral resistance. Once this objective is achieved, there is no need for the lateral resistance anymore which in other words means that the minimum triggering voltage for the device can be so low that the on-state voltage drop of a parallel thyristor will be enough to re-trigger the off- thyristor.

8.1 Reducing the p^+ emitter efficiency or completely eliminating the p^+ emitter in the region of the AG1

The idea is to reduce the PNP transistor gain in the AG1 and thereby reduce the total current in this region. The schematic of such structure is shown in the Figure 49. Reduced p^+ emitter efficiency and even removing the p^+ emitter completely are investigated.

- Case1- p^+ emitter in the complete device
- Case2- Reducing the p^+ emitter efficiency in the AG1 region
- Case3- Removing the p^+ emitter completely in the AG1 region

Since the inner AGs are more susceptible to destruction during triggering from very high voltages, case 1, 2, 3 thyristors are investigated for temperature development in the inner AGs when triggered from 7kV.

Figure 50 shows the development of current over time for case 1, 2, 3 thyristors when triggered from 7kV using the same trigger pulse. It can be seen that case 1 thyristor is faster than case 2 and case 2 thyristor is faster than case 3 which can be directly explained from the PNP transistor current gain in the AG1 region.

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

The maximum device temperatures for case 1, 2, 3 thyristors are plotted in Figure 51. It can be seen that the reduction of anode emitter efficiency in AG1 region reduces the maximum device temperature thereby improving the di/dt capability of the thyristor.

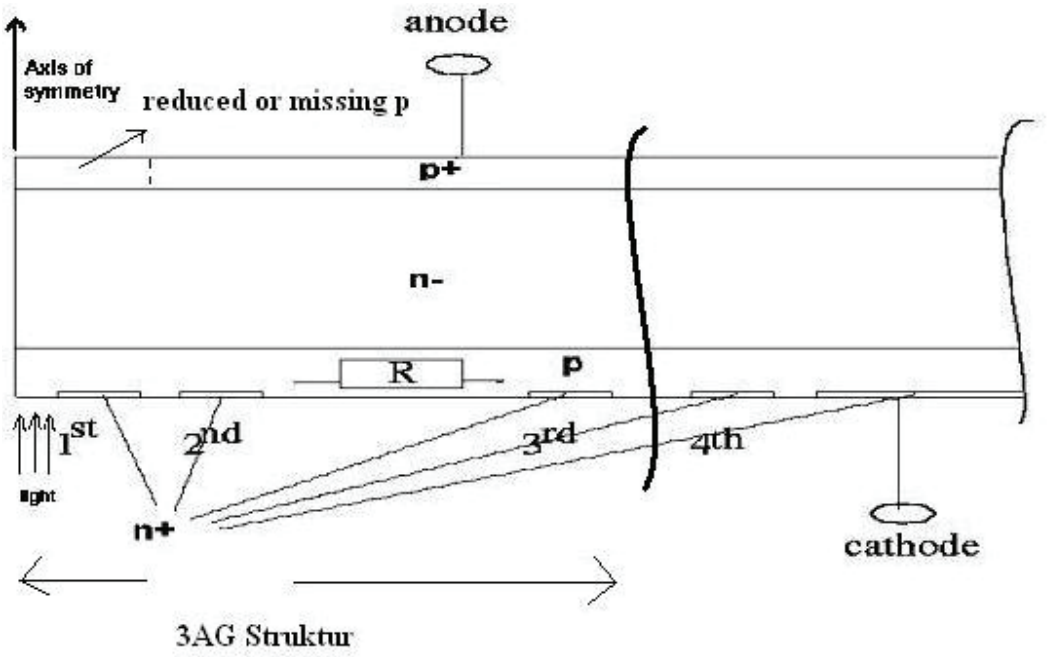


Figure 49 Schematic of the structure with reduced or completely deleted p^+ emitter in the AG1

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

- 73 -

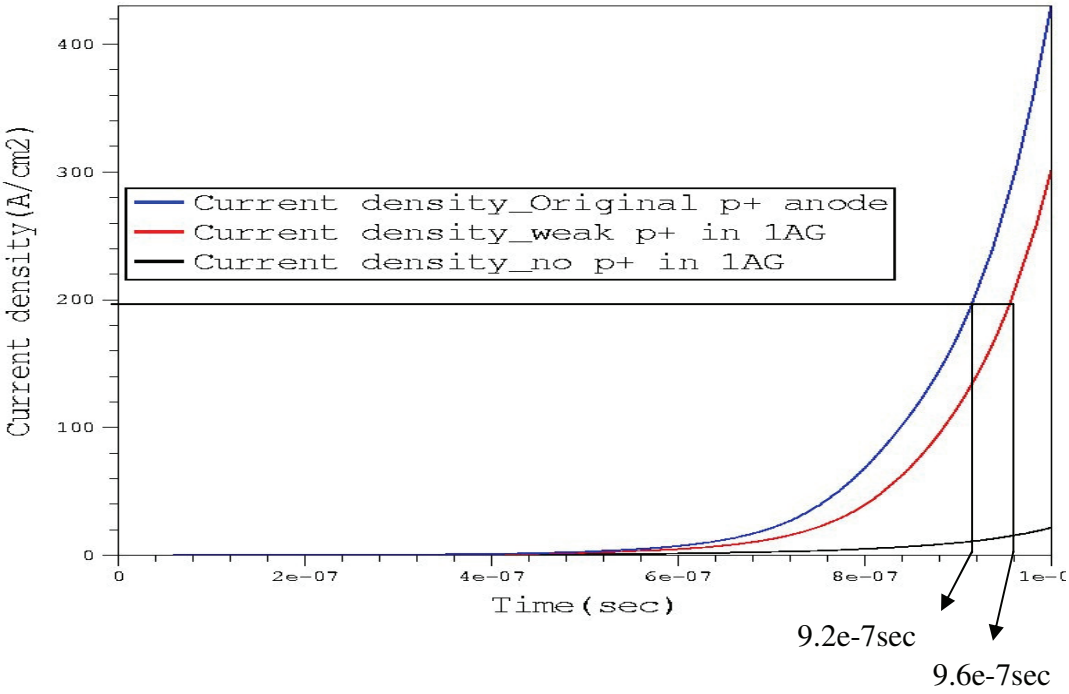


Figure 50 Development of current over time for three different anode-types when triggered from 7kV

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

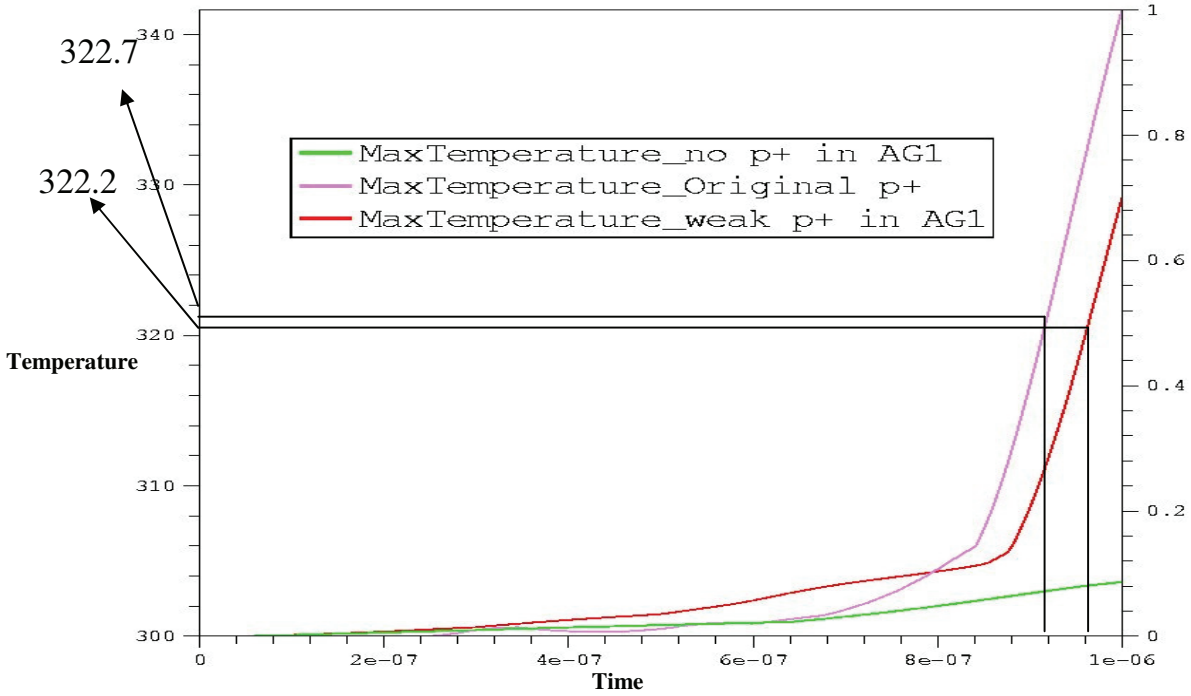


Figure 51 Development of temperature over time for three different anode-types when triggered from 7kV

A comparison of the electron and hole current densities at a given time after triggering for case1, 3 (extreme cases) is shown in Figure 52. As expected, the electron and hole current densities in the case3 thyristor are significantly lower in the AG1 region compared to the case 1 thyristor thereby protecting the inner AGs and improving the di/dt capability of the thyristor.

It can also be seen in Figure 52 that reducing the p^+ emitter efficiency or removing the p^+ emitter completely also has a favorable side-effect, viz. at a given time after triggering, the AG3 is conducting a higher current in case3 thyristor compared to the case1 thyristor, despite a lower total current in case3 thyristor compared to the case 1 thyristor. This means, the AG3 overtakes the load from AG1, 2 faster and thereby reducing the temperature in inner AGs in a case3 type thyristor compared to a case1 type thyristor.

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

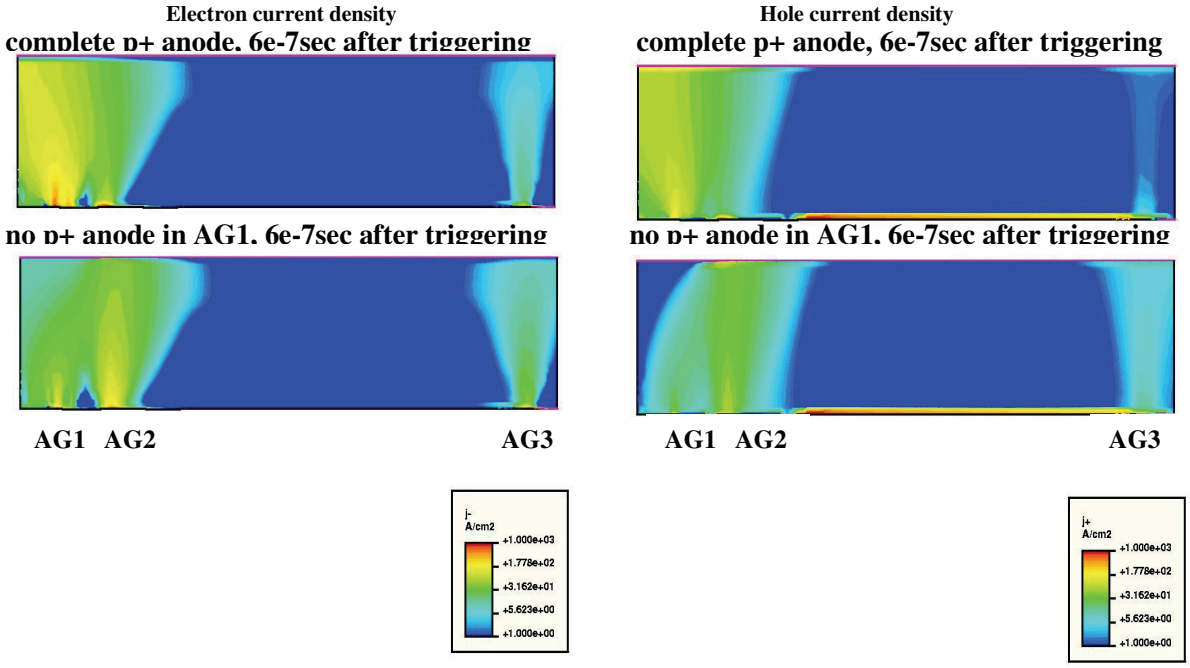


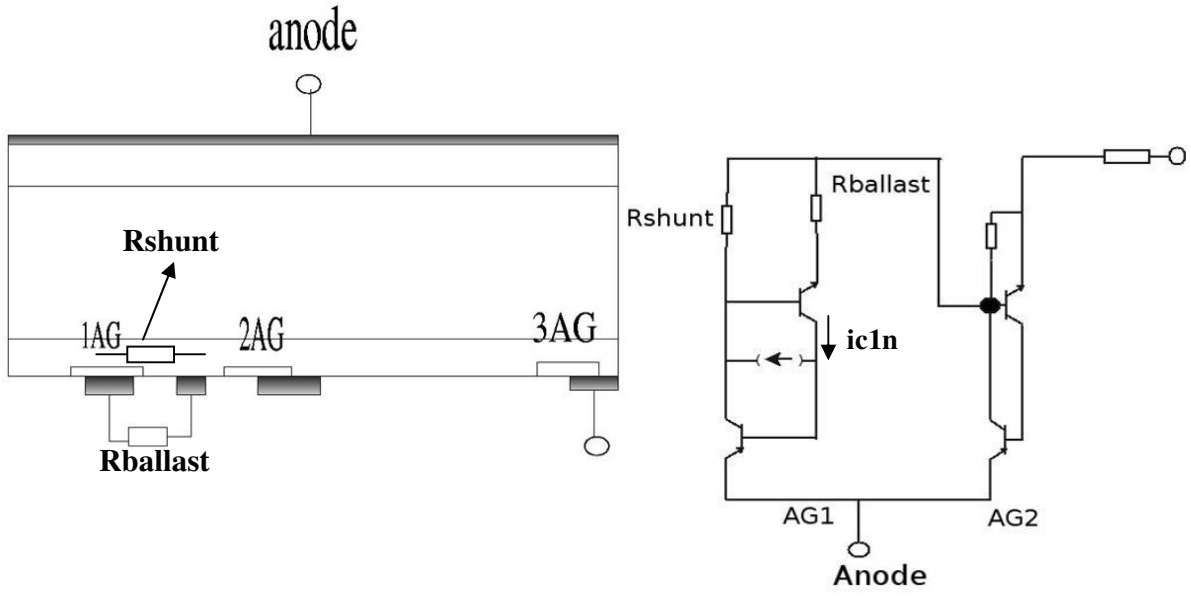
Figure 52 **Electron and hole current density distributions in the thyristor with complete p^+ emitter vs. thyristor with no p+ emitter at a given total current density**

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

8.2 Structure of the Restricted Current Gain (RCG) amplifying gate

In this structure, current in the AG1 is limited to a certain value by an external ballast resistor at the AG1. The schematic structure of a RCG is shown in Figure 53(a). The ballast resistor is called Rballast. The equivalent circuit diagram of the RCG is shown in the Figure 53(b).

The first two transistor model represents the AG1 and the second two transistor model represents AG2 and so on. The emitter ballast resistor is represented by "Rballast" and the shunt resistance for the AG1 is represented by "Rshunt". "ic1n" is the collector current of the NPN transistor in AG1. The operation principle is explained below.



(a) (b)

Figure 53 Structure and equivalent circuit diagram of the Restricted Current Gain (RCG) amplifying gate

The common emitter current gain of the NPN transistor of the AG1 is given by,

Equation 8.1 $$\beta_{NPN} = \frac{Rshunt}{Rballast} = \frac{100\Omega}{20\Omega} = 5$$

The value of β_{NPN} depends only on the values of "Rshunt" and "Rballast". While "Rballast" is a constant external resistor, "Rshunt" is the shunt resistance of the first n^+ emitter

and is modulated (reduced) when the p-base region is flooded with plasma (voltage breakdown situation) resulting in a reduction in β_{NPN} which in other words means reduction in the AG1 current.

Until the voltage breaks down, the current in the AG1 is limited by the external ballast resistor, Rballast. By varying this parameter, the current in the AG1 can also be controlled as needed.

Figure 54 shows the comparison of electron and hole current density profiles between a normal 8kV SCR and a RCG at a given time after triggering. It can be seen in Figure 54 that in RCG, the AG1 is unloaded from current density compared to normal 8kV SCR and thereby hints a lower temperature during triggering.

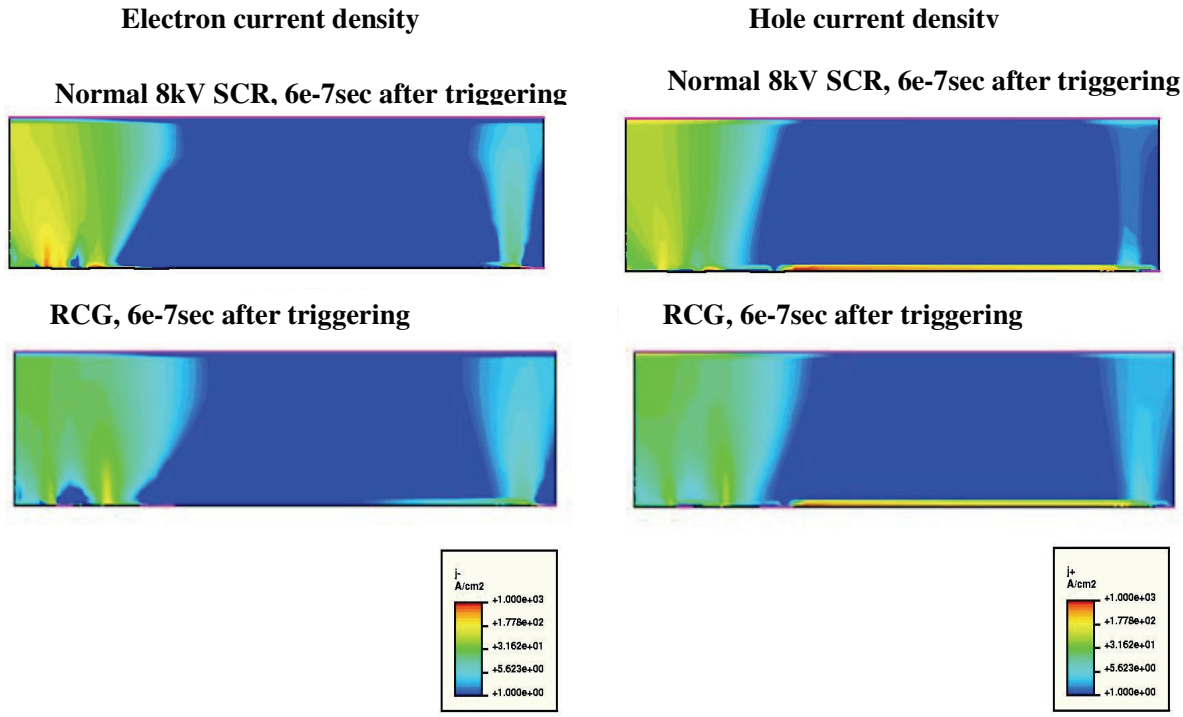


Figure 54 Comparison of electron and hole current densities profiles in the normal 8kV SCR to a RCG structure at a given time after triggering

8.2.1 Using a non-linear ballast resistor

A non-linear ballast resistor limits the AG1 current stronger compared to a linear ballast resistor and thereby improving the turn-on di/dt capability of the thyristor.

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

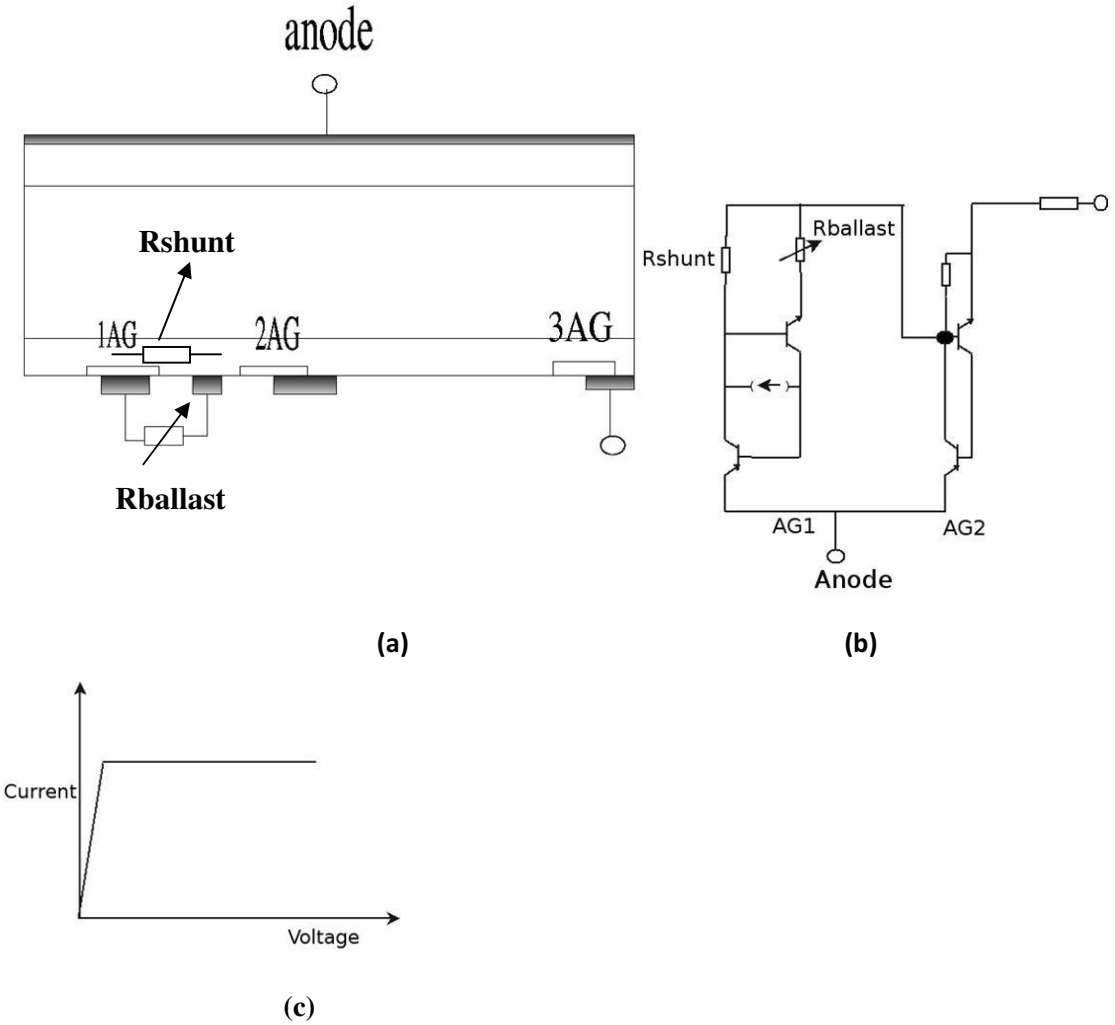


Figure 55 RCG with a non-linear ballast resistor

(a) Schematic of the structure

(b) Equivalent circuit diagram

(c) Ideal I-V characteristics of the non-linear resistor

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

8.3 Structure of the Self Turn off (STO) amplifying gate

A much better protection of the AG1 can be achieved if the current in the AG1 is completely turned off after it has triggered the AG2. This functionality can be achieved by several structures. One such structure is shown in the Figure 56(a).

In this figure, “m2” and “m3” act as shunts for the AG1 and AG2 respectively. “m1” brings the hole current of the AG3 through “m4” which flows in the opposite direction of the trigger current of the AG1 thereby creating a negative feed back to the AG1. This means, as soon as some positive hole current reaches the contact “m4”, a negative feed back is created for the AG1. Clearly a positive hole current reaches “m4” only after the AG2 is triggered completely. Hence this structure serves the purpose of turning off the AG1 after the AG2 is turned on.

It can be seen in the Figure 57 that the current in the AG1 starts to reduce where as the currents in the AG2 and AG3 are still increasing. It can also be seen in Figure 57 on the right Y-axis that the anode voltage is still very high (approx. 6500V while the device is turned on from 7kV). A simple mathematical explanation to the operation of this device is presented here.

Equation 8.2 **The base current of the AG1, iB1=** $\frac{(\mathrm{RE2}+\mathrm{REG})(\mathrm{ic1}+\mathrm{ic2})}{\mathrm{RB1}}$

The common-emitter current gain of the AG1,

Equation 8.3 $\frac{\mathrm{ic1}}{\mathrm{iB1}} = \frac{\{\mathrm{ic1}\}}{\{\mathrm{ic1}+\mathrm{ic2}\}} * \frac{RB1}{REG+RE2}$

Equation 8.4 **For, ic2=0,** $\frac{ic1}{iB1} = \frac{RE1}{REG+RE2} = \frac{100}{14} = 7$

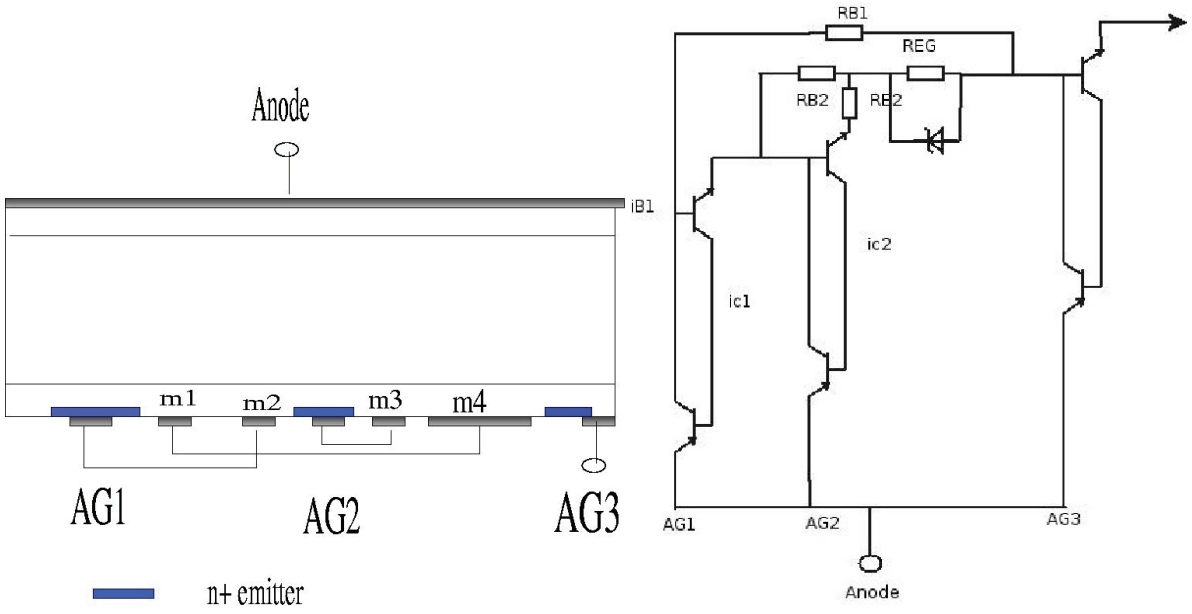
Equation 8.5 **ic2=ic1,** $\frac{ic1}{iB1} = 3.5$

Equation 8.6 **ic2=10*ic1,** $\frac{ic1}{iB1} = 0.64$

Equation 8.7 **ic2=20*ic1,** $\frac{ic1}{iB1} = 0.33$

This means that as the collector current of the AG2 increases, the common emitter current gain of the NPN transistor reduces and results in a complete turn off of the AG1 and hence AG1 is very well protected.

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor



(a) **(b)**

Figure 56 Structure and equivalent circuit of the Self Turn Off (STO) amplifying gate

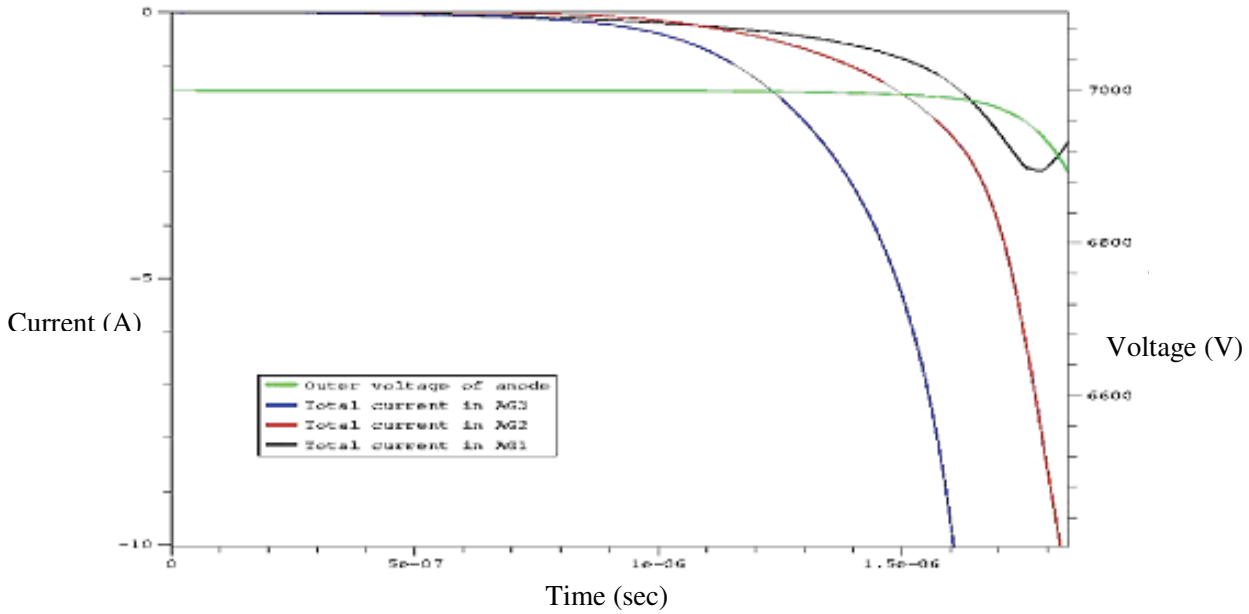


Figure 57 Development of total current in AG1, AG2, AG3 and the anode voltage breakdown over time

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

8.4 Capacitive ballasting

The di/dt capability of a LTT can be improved also by ballasting AG1 with impedance (a network of capacitors, inductors, resistors). In the current work, a parallel network of a capacitor and a resistor as ballast impedance is investigated.

The schematic and equivalent circuit of the investigated structure is shown in Figure 58 (a), (b). The AG1 current charges the ballast capacitor C_{integr} and the ballast resistor $R_{ballast}$, discharges the ballast capacitor with a time constant given by $R_{ballast} * C_{integr}$ until the voltage across C_{integr} reaches a constant magnitude. When the voltage across C_{integr} reaches a constant magnitude, the current through AG1 is limited by $R_{ballast.}$ By choosing the values of $R_{ballast}$ and C_{integr} appropriately, the AG1 current can be limited to a lower value thereby increasing the di/dt capability of the thyristor.

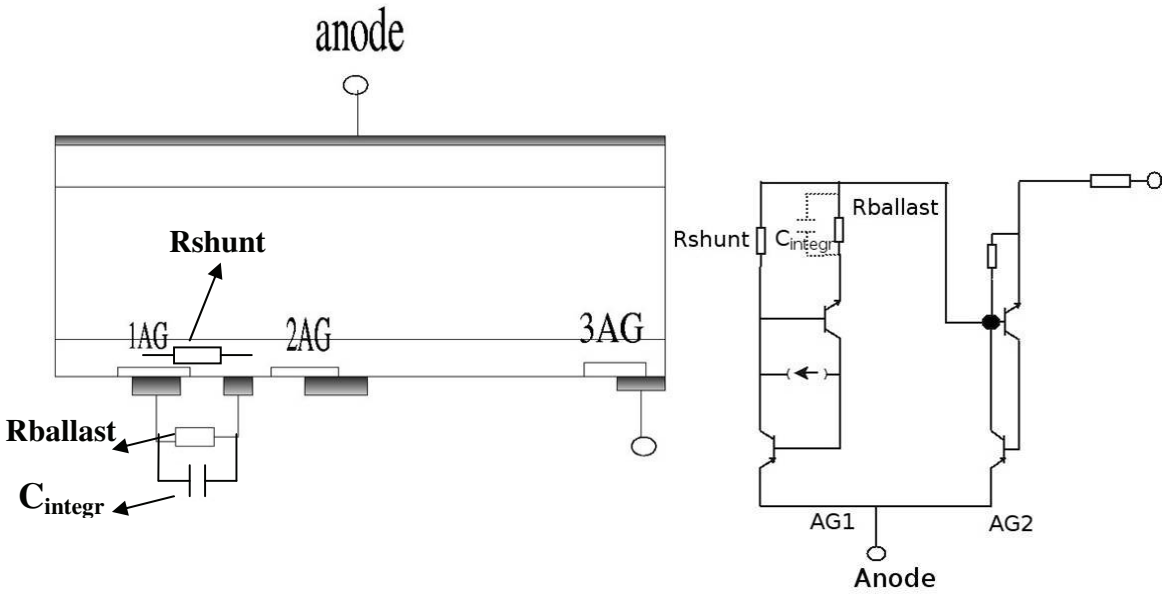


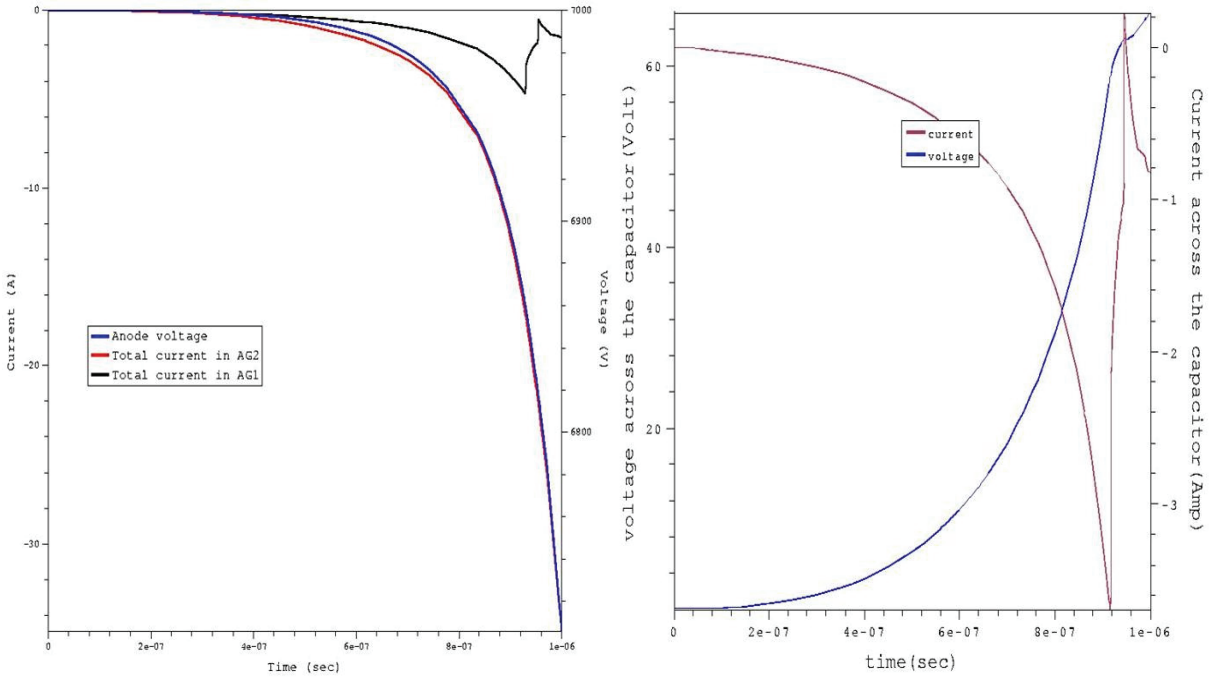
Figure 58 Concept of capacitive ballasting (a) Schematic of an LTT with capacitive ballasting for the AG1 (b) Equivalent circuit diagram

8.4.1 I-V characteristics

Simulations are done to observe the current development in AG1, AG2 and the anode voltage over time. $C_{integr} = 10nF$, $R_{ballast} = 50\Omega$ is chosen resulting in a 0.5µsec time constant. Figure 59 (a) shows the current development in AG1, AG2 and the anode voltage over time. It can be seen that the current in the AG1 is limited. For a better analysis, the voltage across the capacitor nodes and current through the capacitor are plotted in Figure 59 (b).

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

The current through the AG1 charges C_{integr} increasing the voltage across the capacitor nodes. When the capacitor is fully charged, the voltage across the capacitor becomes constant and the current through the capacitor becomes zero. Before the voltage across the capacitor reaches a constant value, oscillations in the AG1 current can be observed (Figure 60) due to charging and discharging of C_{integr} by $R_{ballast}$. A zoomed version of the oscillations with detailed analysis can also be seen in Figure 60.

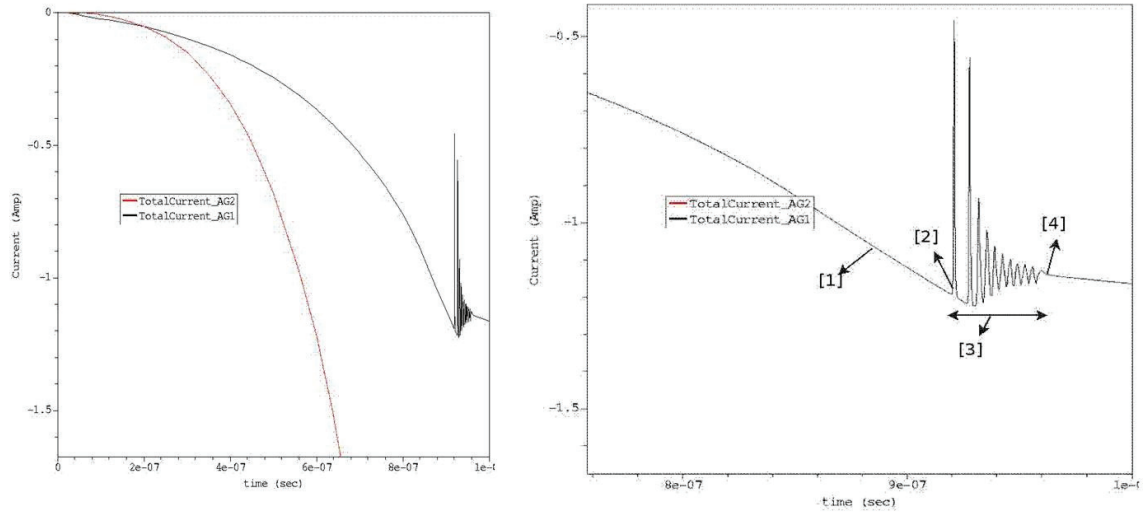


(a) **(b)**

Figure 59 **(a) Development of total current in the inner AGs and the anode voltage over time**

(b) I, V vs. time across the capacitor nodes with C=10nF, R=50 ohm

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor



[1]- The capacitor C is being charged
[2]- The capacitor C starts to discharge
[3]- The capacitor C charges and discharges with a time constant $\tau = R_{ballast}C$
[4]- The voltage across the capacitor becomes constant (indicating the conductivity modulation in the p-base) and the 1st AG current reaches a constant value limited by the $R_{ballast}$ value

Figure 60 Zoomed version of the current development in the inner AGs over time

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

8.4.2 Integration of capacitive ballasting

Several possibilities of integration of a RC network are investigated in the following sections.

8.4.2.1 Method 1:

This is a simple method of integration of a RC network in the AG1 region. An insulating material (for e.g. SiO_2) is sandwiched between the AG1 metal contact and the shunt-contact as shown in Figure 61. This capacitance can be calculated as,

$$C_{\text{int}egr} = \frac{\varepsilon A}{d} \qquad \textbf{Equation 8.8}$$

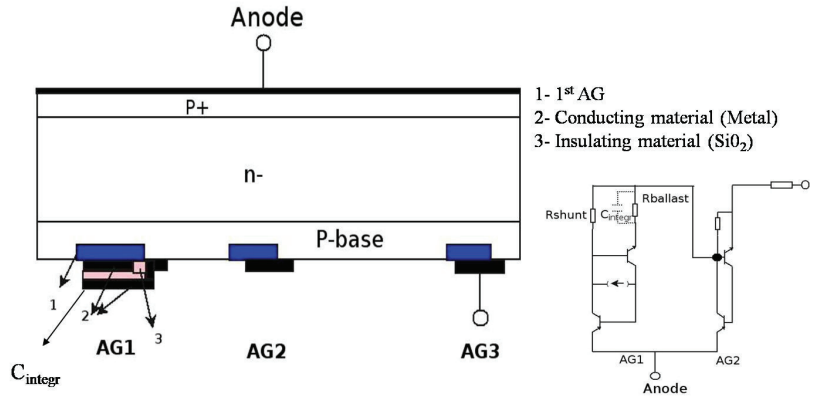
Where, ε= Permittivity of the insulating material

A= approximately the area of the overlapping between the AG1 metal contact and the shunt-contact

d= thickness of the insulating material

To integrate a 10nF capacitance in the available AG1 area in the present structure and using SiO_2 as insulation material, the required thickness of the SiO_2 layer is not in the acceptable tolerance level. Therefore, either an insulating material with a much higher permittivity or a much higher AG1 area is required to integrate a capacitance in the order of Nanofarad.

Increasing the AG1 area will tend to reduce the dv/dt capability of the thyristor.



Note: If the demanded capacitor value is high, integration of the capacitor in this method requires either
(a) an insulating material with a high relative permittivity (or)
(b) a large ring area in the 1st AG region which can lead to a fault dv/dt triggering

Figure 61 Integration method-1 of the capacitor in the AG1 area

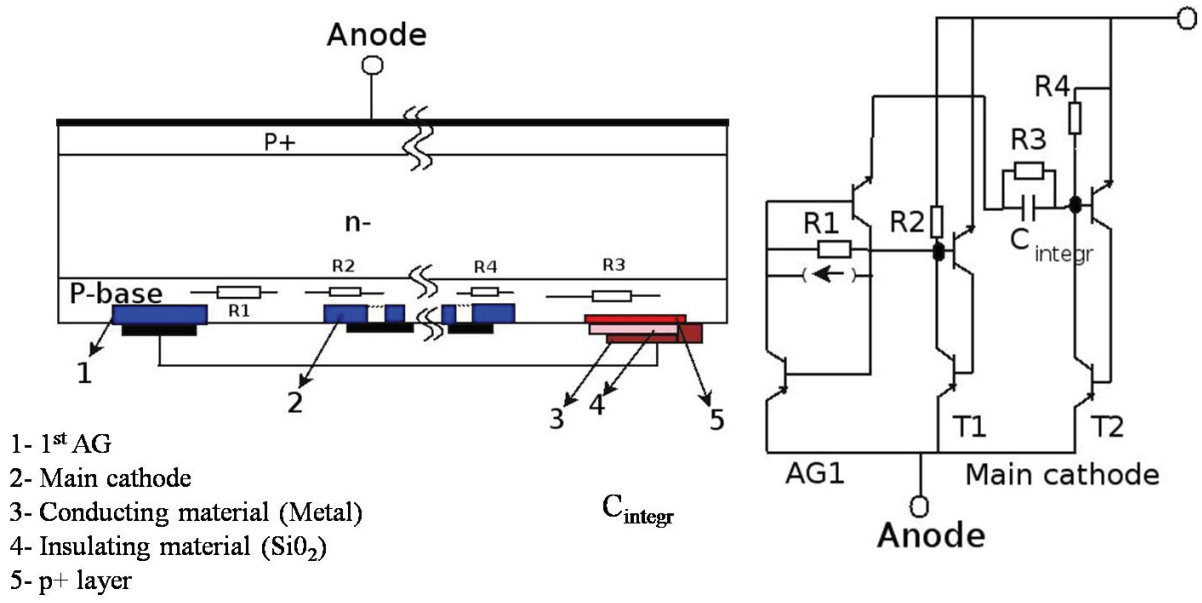
8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

8.4.2.2 Method 2:

In principle, method 2 is same as method 1 other than the capacitance is not integrated in the AG1 area but outside the main cathode (Figure 62) thereby not increasing the AG1 area which may make it susceptible to fault dv/dt triggering.

The capacitance is integrated by sandwiching an insulating material (for e.g. SiO_2) between a p^+ layer and a metal contact. Since the capacitance is integrated outside the main cathode area, the area consumed by capacitance integration is not critical anymore.

The ballast resistance is shown as R3 in Figure 62. The value of R3 can be tailored by varying the p-doping concentration under the integrated capacitance area.



Note: In this method, integration is done outside the main cathode. It can be a suitable method of integration for the HTT in LTT-HTT concept

Figure 62 Integration method-2 to save the area in the AG1 thereby avoid any possible fault dv/dt triggering

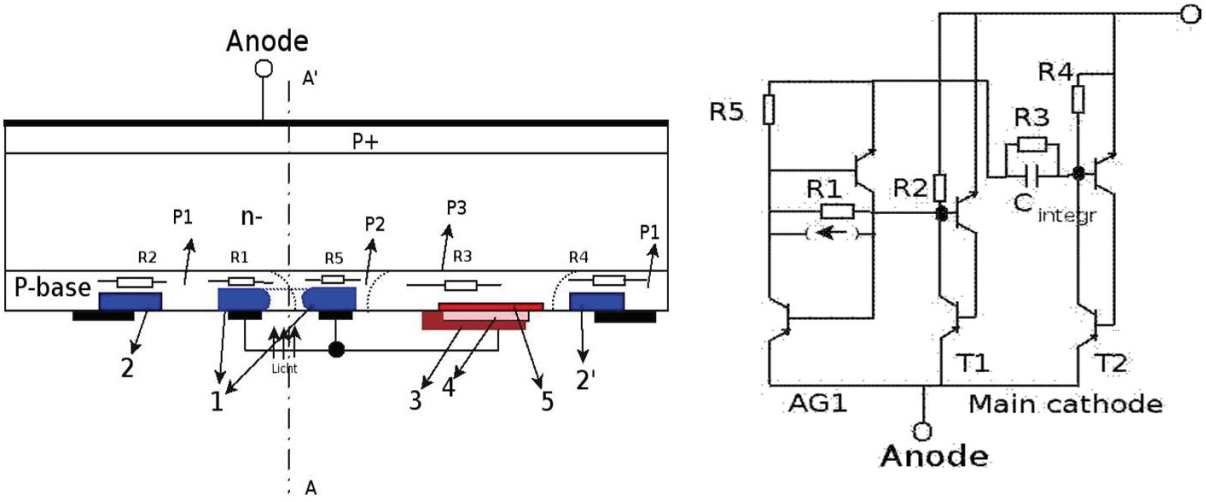
8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

8.4.2.3 Method 3:

In this method, only a part of the AG1 ring is used to integrate the RC network thereby avoiding a tendency towards fault dv/dt triggering. Figure 63 shows the intersection of the gate structure of such a thyristor. A-A' is the virtual axis of symmetry of the thyristor since the thyristor loses its symmetry in this method. Figure 64 shows the realization of method-3 gate structure with a so-called "Key-hole" structure.

The part of the AG1 ring connected to the integrated capacitance has a shunt resistance R5. The rest of the ring has a shunt resistance R1. R5 has to be much greater to R1 so that the triggering of AG2 by AG1 occurs via R1. R3 is the ballast resistor in parallel to C_{integr}.

When the AG1 is triggered, AG2 is triggered via R1 and the current is the AG1 is limited by the RC ballast network formed by C_{integr} and R3. Since only a part of the AG1 ring area is used to integrate the RC network, the tendency towards a fault dv/dt triggering is reduced.



1- 1st AG ring
2, 2'- 2nd AG
3- Conducting material (Metal)
4- Insulating material ($Si0_2$)
5- p+ layer

Note : R5 >= R1
Typical values : R1= 100 Ω
R3=200 Ω
R5= 300 Ω
C= 10nF

Figure 63 Integration method-3 which can be realized by the so-called "Key-hole structure"

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

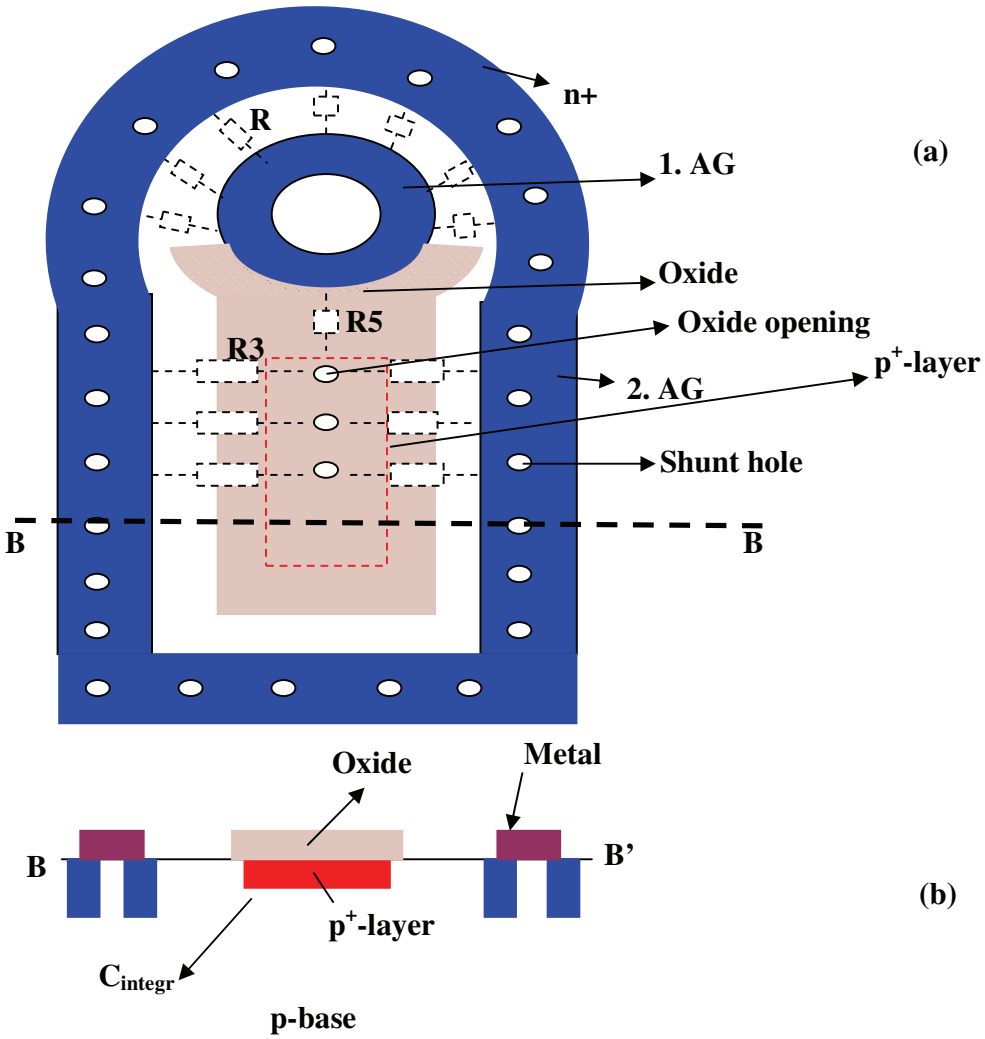


Figure 64 **Realization of method-3 gate structure with a so-called key-hole structure (before metal coating)**

8. Investigated ideas to reduce the temperature in the inner AGs without using a lateral resistance between the inner AGs and outer AGs and thereby reducing the minimum trigger voltage of the thyristor

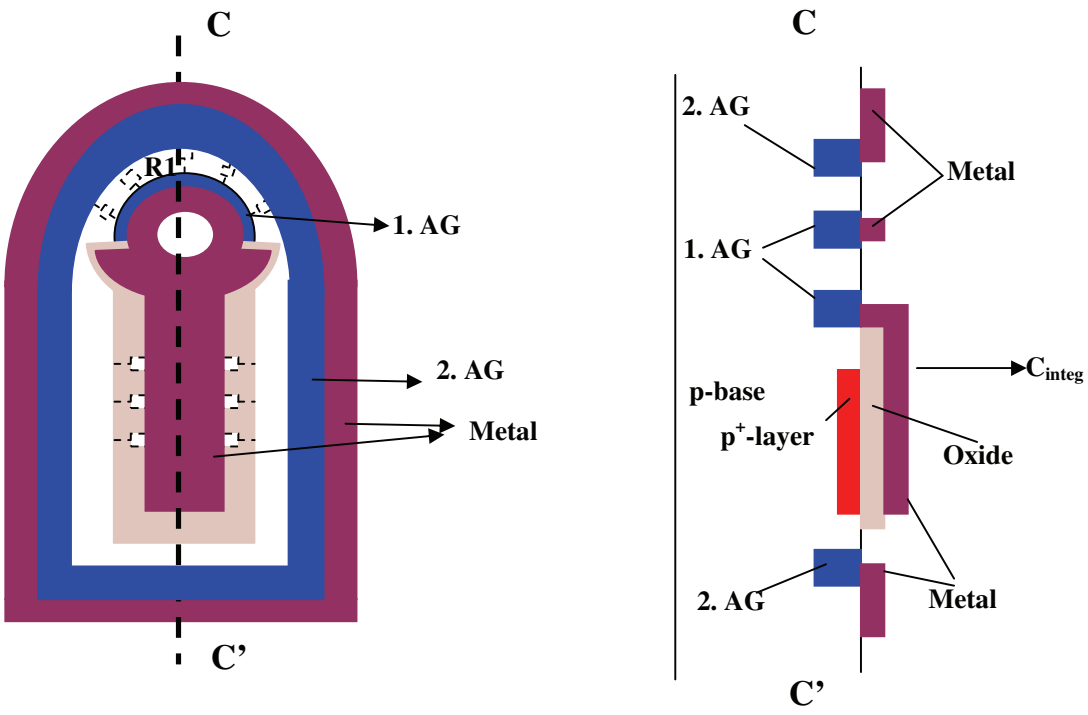


Figure 65 Key-hole structure after metal coating

9 Concept of LTT-ETT to avoid fault reapplied dv/dt triggering

A novel concept of using a LTT as a pilot thyristor to trigger an ETT is investigated. The schematic of the LTT-ETT concept is shown in the Figure 66. The LTT includes three AGs. The cathode of the AG3 is connected to the gate and cathode of the ETT via resistors R2, R1 respectively. AG2 and AG3 are connected by a resistor R3 to protect the AG1 and AG2. The idea of this concept is to force the LTT to be a replica of ETT in both electrical and thermal states during the conduction and reverse recovery state. Therefore, when a positive dv/dt pulse within the window of fault reapplied dv/dt triggering occurs, the LTT triggers first for the LTT has the rest plasma profile as that of the ETT and has a lower area compared to the ETT. Homogeneous carrier lifetime profiles in LTT and ETT is assumed here.

Necessary conditions to be fulfilled in the LTT-ETT concept for a safe reapplied dv/dt triggering

- Condition 1: LTT and ETT are in the same electrical state during conduction and reverse recovery states
- Condition 2: LTT and ETT are in the same thermal state during conduction and reverse recovery states
- Condition 3: LTT and ETT have the same carrier lifetime killing profiles
- Condition 4: Each AG is triggered homogeneously across its area

9.1 Measures taken to fulfill the necessary conditions:

- Condition 1: LTT and ETT are in the same electrical state during conduction and reverse recovery states. Cathodes of LTT and ETT are connected via a non-linear resistor, R1 (lower resistance at lower voltages and high resistance at higher voltages). In the on-state (lower voltages), lower resistance of R1 ensures that the LTT and ETT are at the same or nearly the same electrical state. At triggering voltages (high voltages), higher resistance of R1 ensures that the triggering current mainly flows through R2 to the gate of the ETT. Non linear resistor can be integrated by a p^+-p^- -p^+ structure in a thyristor.

9. Concept of LTT-ETT to avoid fault reapplied dv/dt triggering

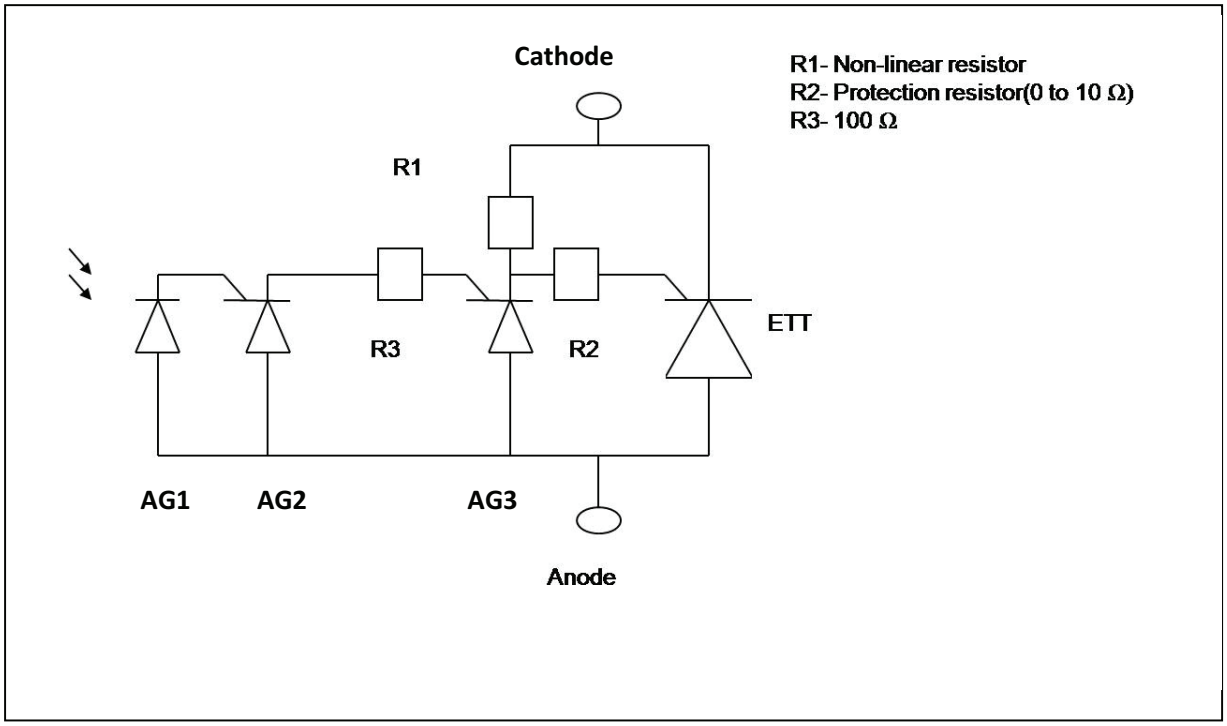


Figure 66 Pilot LTT connected to an ETT

- Condition 2: LTT and ETT are in the same thermal state during conduction and reverse recovery states. Ensuring the same thermal state for LTT and ETT can be ensured by embedding both LTT and ETT in the same housing, i.e. same cooling. Since this problem is not in the scope of the present work, it is not dealt with here.
- Condition 3: LTT and ETT have the same carrier lifetime killing profiles. Same carrier lifetime profiles have to be used in LTT and ETT. A higher carrier lifetime in LTT can even be better since it causes a higher concentration of rest plasma in LTT. Therefore, in a reapplied dv/dt scenario, LTT is triggered before ETT
- Condition 4: Each AG is triggered homogeneously. While it is necessary that the LTT is triggered before ETT in a reapplied dv/dt scenario, the triggered AGs in LTT have to trigger aerially homogeneously. If only a part of AG is triggered, it can cause current filamentation in that particular AG. To ensure homogeneous triggering in an AG, a structure as shown in Figure 67(a) can be used. Each AG is radially broken into several n+ emitters. In the Figure 67(a), AG3 is radially broken into 120 n^+ emitters. When one or more of 120 n^+ emitters trigger, the triggered n^+ emitter trigger their neighboring n^+ emitters leading to a radially

homogeneous triggering. The time taken for the triggering to distribute homogeneously has to be smaller than the time required for current filamentation.

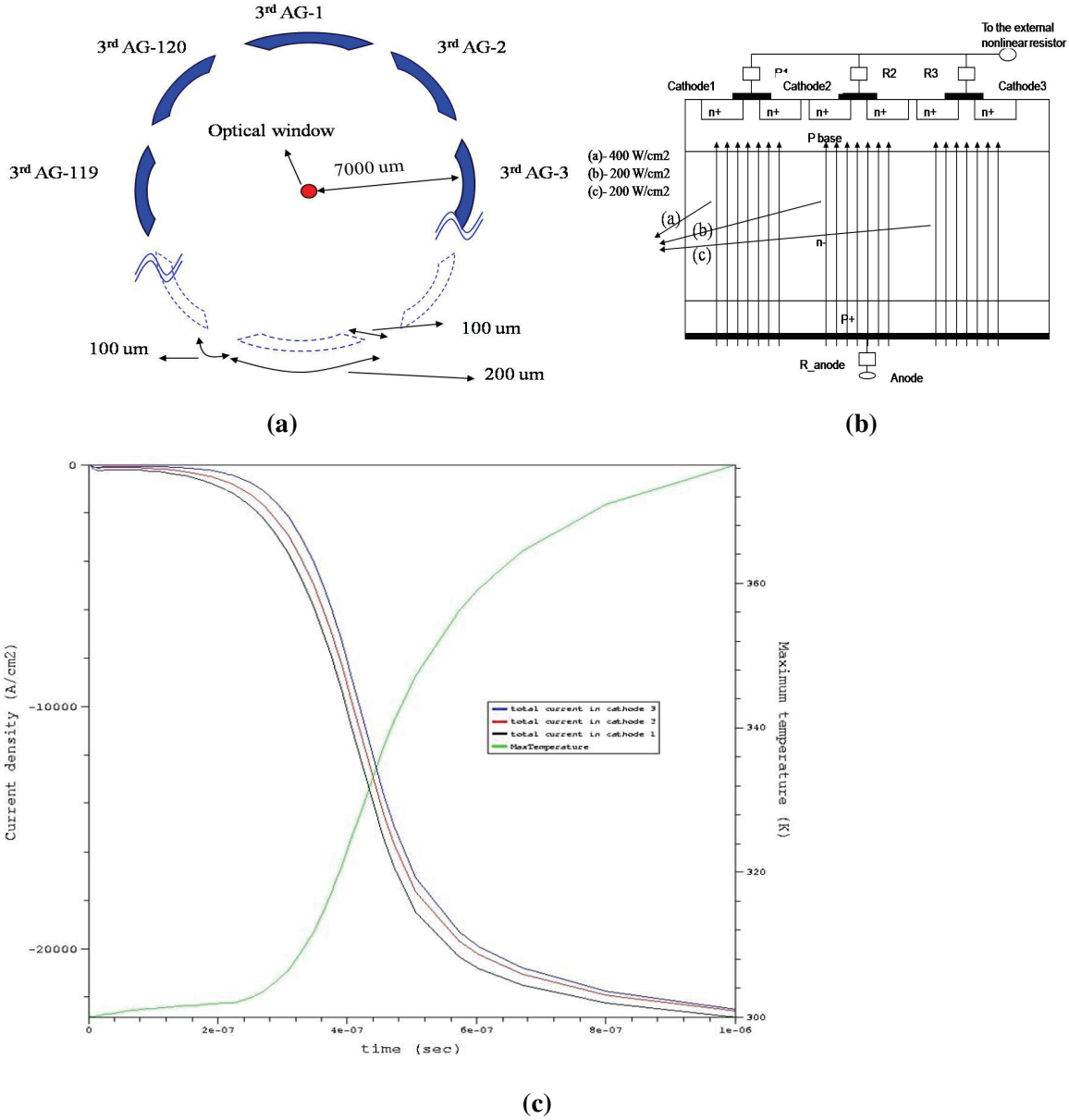


Figure 67 **(a) AG structure to ensure a homogeneous current distribution**

(b) Simulation model

(c) Current development in AG1, 2, 3; Maximum temperature over time

A simulation model is created to calculate the speed of triggering distribution and the increase in device maximum temperature. The n^+ emitters in Figure 67(b) represent the neighboring n^+ emitters in Figure 67(a). Cathodes 1, 2, 3 are connected via resistors R1, R2, R3 to the external non-linear resistor R1 (in Figure 66). Resistors R1, R2, R3 (in Figure 67 (b)) are scaled to an equivalent resistance of 1,2e4 Ω according to the consideration that the resistor R2 (in Figure 66) be 1 Ω. Cathode 1 is triggered with the minimum trigger current from 7kV forward voltage between cathode and anode. Figure 67(c) shows that cathodes 2 and 3 are triggered by cathode 1 with negligible increase in the maximum device temperature at the thyristor operating current densities.

10 Summary

1.

a. Usage of LTTs in high voltage switching applications like HVDC and SVC simplifies/avoids the control circuitry and thereby offers robust power systems with lower production cost.

b. Integration of protection against all possible fault triggering mechanisms (including reapplied dv/dt) is possible. Therefore, LTTs offer a genuine alternative to ETTs in very high voltage switching applications.

2.

a. Dynamic punch-through reduces turn-on delay in symmetrical thyristors. Kirk effect displaces the hot spot during triggering from cathode side to anode side in asymmetrical thyristors

b. Tandem 13kV thyristor offers an increase of 5kV in blocking voltage with only doubling the on-state losses, without any significant difference in switching losses compared to an 8kV thyristor.

c. Anode shunting is the better alternative solution for the problem of blocking at high temperatures in Tandem 13kV thyristors. A weak anode shunting density, which causes only a negligible increase in the on-state losses, is sufficient to ensure blocking at high temperatures.

3.

a. An integrated lateral resistance is necessary to protect the inner AGs and thereby to increase the di/dt capability of a thyristor. However, heat distribution across the integrated lateral resistance shall be homogeneous.

b. Homogeneous heat distribution is achieved by a non-linear resistance structure which also provides an enhanced protection to the inner AGs without increasing the minimum triggering voltage and therefore results in a higher di/dt capability.

c. Negative resistance (Snap-back) phase of the non-linear resistor is forbidden. A method to eliminate snap-back is investigated.

4.

a. Several novel gate structures with the aim of increasing the di/dt capability of thyristors are investigated.

    - Reducing the p^+ emitter efficiency or completely eliminating the p^+ emitter in the AG1 region.

Reducing the p+ emitter efficiency or completely eliminating the p^+ emitter in the AG1 region reduced the PNP transistor current gain in AG1 and subsequently the current density in the AG1 region to improve the di/dt capability of the thyristor.

- Reduced Current Gain (RCG) AG

  A Reduced Current Gain (RCG) AG1 is ballasted with a resistor to reduce its NPN transistor current gain and therefore the current density in the inner AGs during triggering. This resulted in an increased thyristor di/dt capability. A non-linear ballast resistor intensifies the above effect and shall be more effective in increasing the thyristor di/dt capability.

- Self Turn Off (STO) AG

  A Self Turn Off (STO) AG1 turns off completely after it has triggered the AG2 reducing the load of AG1 to the minimum and therefore increased the thyristor di/dt capability.

- Capacitive ballasting

  AG1 ballasted with a RC network also turns off the AG1 after it has turned the AG2 on. In principle, capacitive ballasting is very similar to the STO AG but a more elegant solution. Integration of RC ballast in an AG is possible. Several methods to integrate RC ballast are investigated in the present work. A different network of resistors, capacitors and inductances can lead to a similar or a better effect.

These novel gate structures are submitted at the German patent office for patent rights.

b. A concept of using an LTT as a pilot thyristor with a segmented n^+ emitter to trigger a main ETT is investigated with the aim of achieving protection against fault reapplied dv/dt triggering.

11 Proposals for future work

The most burning problem in the field of LTTs is fault reapplied dv/dt triggering. New concepts which are realizable with affordable economic investment deserve a thorough investigation. Presently, two concepts are pursued by the German industry to solve the fault reapplied dv/dt triggering problem.

11.1.1 Concept 1 (Using a LTT as a pilot thyristor to trigger the main thyristor (ETT)):

In the present work, problems like ensuring a homogeneous current distribution in the LTT, the network of resistors connecting the LTT and the ETT to with the aim of achieving thermal and electrical equilibrium between the LTT and the ETT are investigated. However, more investigations are to be done to ensure a thermal and electrical equilibrium between the LTT and the ETT.

11.1.2 Concept 2 (A full integration of protection against fault reapplied dv/dt triggering):

A gate structure to integrate protection against reapplied dv/dt is proposed. Due to patent related problems, it is not discussed at all in the present work. However, this new gate structure is to be thoroughly investigated and optimized. Candidates interested in such a work shall correspond with the company IFBIP (Infineon Bipolar), Warstein, Germany for further details.

Appendix A

12 Profile of the lateral protection resistor to achieve homogeneous heat energy distribution

The differential resistance between 2nd and 3rd AGs

$\Delta R = \Delta r * R_{\blacksquare} / 2\pi * r$

Where,

"r" is the radius

Δ r is the differential radius

"$R_{\blacksquare}$ "is the sheet resistance

"Δ R" is the differential resistance

Equation 12.1 **Differential voltage drop $\Delta V = i * \Delta R$**

Equation 12.2 **Differential power loss/area, $\frac{\Delta P}{2\pi r * \Delta r} = i^2 * R_{\blacksquare} / 4\pi^2 r^2$**

This implies that for a homogeneous differential power dissipation per area, sheet resistance must be proportional to the square of the radius ($R_{\blacksquare}=k*r^2$)

12.1 Comparison of temperatures across the graded ($R_{\blacksquare}=k*r^2$) lateral resistance and homogeneously doped ($R=k*r$) lateral resistance

12.1.1 Case of graded lateral resistance ($R_{\blacksquare}=k*r^2$)

Equation 12.3 **Resistance of the lateral resistance, $R = \int R_{\blacksquare}(r)\, dr/2\pi r =$**

$$\int \frac{K * r^2}{2\pi r} dr = \frac{K * (r_2^2 - r_1^2)}{4\pi}$$

where

r_2 is the outer radius of the lateral resistance

r_1 is the inner radius of the lateral resistance

=>R= $\frac{K(0.6^2 - 0.2^2)}{4\pi}$

For R=100Ω; k=4000 $\frac{\Omega}{cm^2}$

At $R_{\blacksquare}$ (at 2mm) = 160 Ω/■

At ($R_{\blacksquare}$ at 6mm) =$1.44*10^3$ Ω/■

At 4kV voltage drop across the lateral resistance, current i=4kV/100 Ω = 40A

Equation 12.4 **Differential power dissipation/area,**

$$\frac{\Delta P}{\Delta r * 2\pi r} = \frac{(40A)^2}{4\pi} * 4000 \frac{\Omega}{cm^2} = 1.6*10^5 \frac{W}{cm^2}$$

Equation 12.5 **Differential power dissipation /volume,** $\frac{\Delta P}{\Delta V} = 5*10^7 \frac{W}{cm^3}$

Equation 12.6 **Differential energy/volume,** $\frac{\Delta E}{\Delta V} = 5*10^7 \frac{W}{cm^3} * 1\mu\text{sec} = 50 \frac{W\text{ - sec}}{cm^3}$

The triggering time of the AG3 when triggered from 4kV is 1μsec after which the lateral protection resistor is unloaded. Therefore,

Equation 12.7 **Temperature increase, ΔT=** $\frac{\Delta E}{\Delta V * \Theta} = \frac{50 \frac{W\text{ - sec}}{cm^3}}{1.7 \frac{W - \text{sec}}{cm^3 K}} = 30K$

Where, Θ is the specific heat of Silicon.

12.1.2 Case of homogeneously doped lateral resistance (R=k*r)

For a homogeneous doped lateral resistance, sheet resistance, $R_{\blacksquare}$ is constant.

In the case of lateral protection resistor between AG2 and AG3, $R_{\blacksquare}$ =600 Ω/■

Equation 12.8 **Differential power dissipation/area,** $\frac{\Delta P}{\Delta r * 2\pi r} = 6*10^5 \frac{W}{cm^2}$

Comparing Equation 12.2 and Equation 12.8,

Homogeneous lateral resistance will result in at least 4 folds higher temperature closer to the inner AG region than the lateral resistance graded according to $R_{\blacksquare}=k*r^2$.

Appendix B

13 Introduction to Double sided (Egawa) and single sided ("half-Egawa") instabilities

Egawa and "half-Egawa" effects are basically types of dynamic avalanche. Dynamic avalanche is avalanche caused by increase and decrease in electric field due to an influence of mobile holes and electrons respectively in addition to the applied voltage. These instabilities can result in negative resistance regions leading to a current filamentation thereby a possible destruction of the device.

13.1 Double sided (Egawa) instability

Egawa instability (Reference 12) can result in failure of P-I-N structures under negative high voltage pulses even if the voltage pulse has not sufficient energy to cause hazardous temperatures. The electric field profile in the intrinsic region of a P-I-N structure is nearly flat (shown in thick dotted lines in Figure 68, top) until the condition for avalanche generation is reached. Once the avalanche condition is reached, electron-hole pair generation occurs both at P-I, N- I junctions. The generated electrons are driven to the positively biased N-region and the holes generated are driven to the negatively biased P-region. To observe the influence of these mobile carriers on the electric field profile, apply Poison equation to the I-region.

Equation 13.1 $$\frac{df}{dx} = \frac{q}{\varepsilon}(p_m - N_A^- + N_D^+ - n_m)$$

where,

p_m-mobile hole concentration

n_m-mobile electron concentration

N_D^+- ionized donor concentration

N_A^--ionized acceptor concentration

In an intrinsic region, $N_A^- = N_D^+ = 0$

The mobile carriers change the flat electric field profile into a parabolic shape (shown in thin dotted lines in Figure 68, top) (Reference 12). This phenomenon can reduce the voltage

(space integral of electric field) sustained by the intrinsic region with increasing current leading to a snap-back or a negative slope in I-V characteristics.

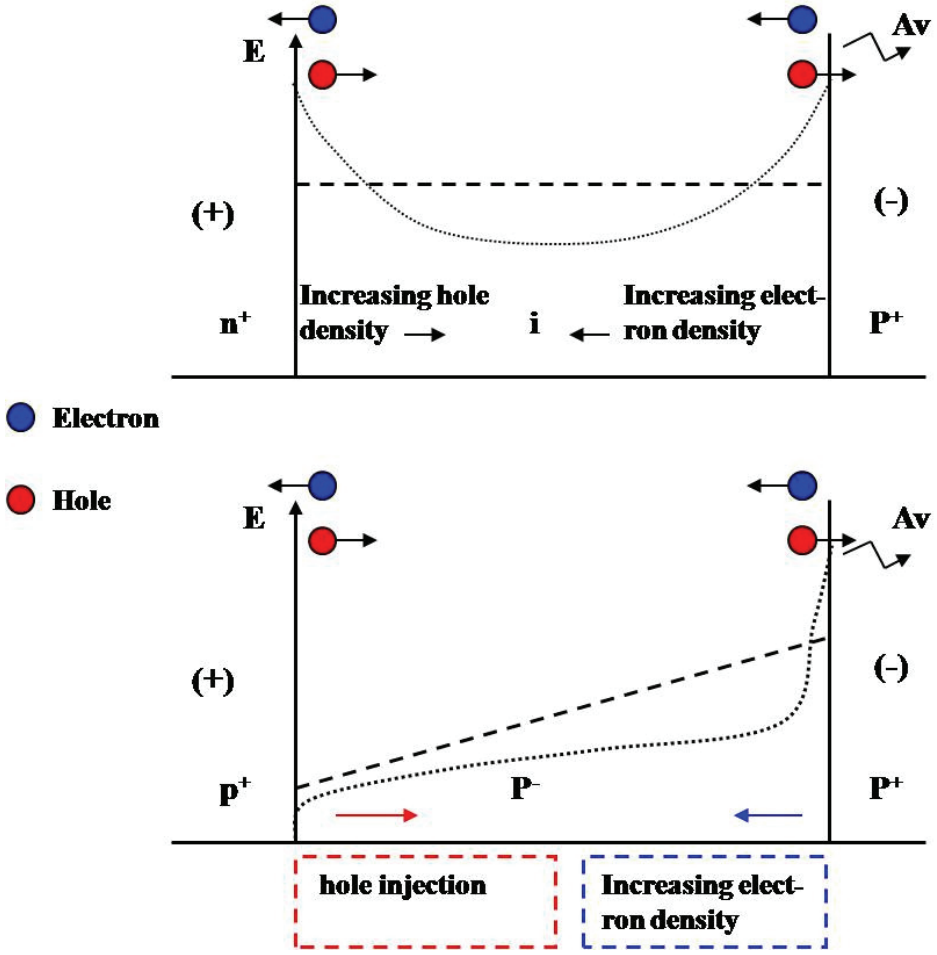


Figure 68 Egawa and "half-Egawa" instabilities

13.2 Single sided ("Half- Egawa") instability

"Half-Egawa" instability can be observed in symmetric structures like p^+-p^--p^+ structures or n^+-n^--n^+ structures. In the current work, p^+-p^--p^+ structures are investigated.

In a p^+-p^--p^+ structure, voltage is supported by the p^- region. Electric field profile in a p^- region with constant acceptor concentration has nearly a constant slope (shown in thick dotted lines in Figure 68(a), bottom). The injected hole concentration from the positively biased p^+ in addition to the hole concentration due to impact ionization at the positively biased p^+-p^- increases the height of electric field at the negatively biased p^+-p^- junction. The influence of

mobile carriers on the shape of electric field can be understood by applying Poison equation to the p^- region.

Equation 13.2

$$\frac{df}{dx} = \frac{q}{\varepsilon}(p_m - N_A^-) = \frac{q}{\varepsilon} * \Delta p_{inj}$$

Where, Δp_{inj}- injected hole carrier concentration from the positively biased p^+ region.

Electrons generated due to impact ionization at the negatively biased p^+ -p^- junction, reduce the height of electric field in the p^- region. Although the peak electric field increases at the negatively biased p^+ -p^- junction, the spatial integral of electric field can reduce if the p^- region is higher in volume compared to the electric field peak. Such a condition results in a snap-back in I-V characteristics of a p^+-p^- -p^+ structure.

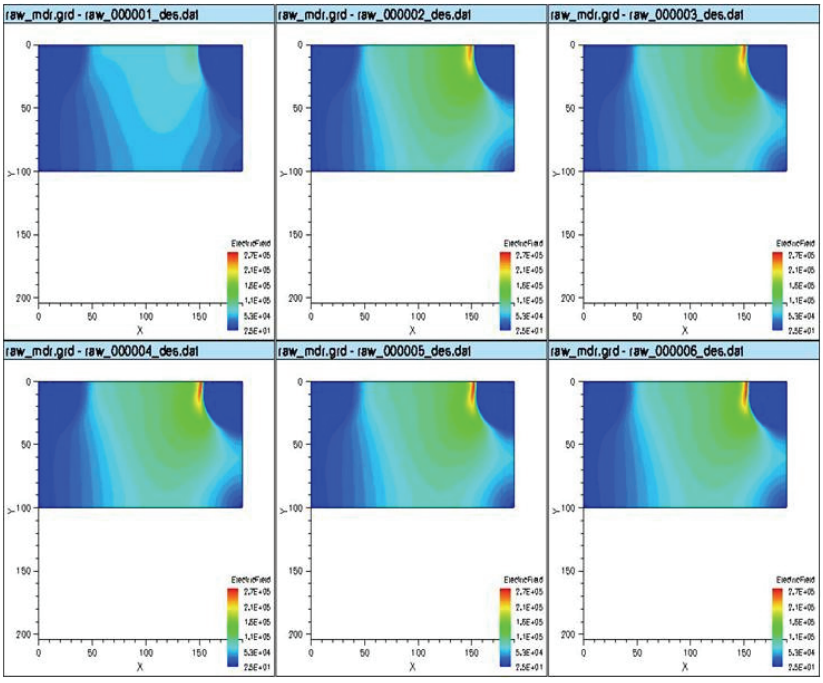


Figure 69 Simulation of a p^+-p^- -p^+ structure to illustrate "half-Egawa" effect. Development of electric field at the outer p^- -p^+ with increasing current is to be observed

13. Introduction to Egawa and half-Egawa instabilities

APPENDIX C

14 Dependence of avalanche break-down voltage on the curvature of the junction (Reference 14)

In the case of very high current rectifiers and thyristors where single devices are made from an entire wafer, it is common practice to use beveling technique to terminate the edges. However, in LTTs with integrated BOD (protection against forward over-voltage), edge termination of the p-base is used to reduce the avalanche breakdown voltage of the BOD. The most widely used edge termination is based on the use of planar diffusion technology.

Planar diffusion is based on the ability to selectively introduce dopants into the semiconductor surface by using either an oxide layer as a mask against dopant diffusion or by using a photo resist layer to block the dopant during ion implantation. When the junction is fabricated by diffusing the dopant in a local region, it can be treated as a parallel plane inside the diffusion window.

However, the dopant also diffuses laterally at the edges of the diffusion window as illustrated in Figure 70. The lateral diffusion of dopants at the edges of diffusion windows has been analyzed and shown to extend to about 85% of the vertical depth x_j. For purposes of breakdown analysis, an approximation can be that the lateral diffusion is equal to the junction depth. From this assumption, it can be concluded that the junction takes a cylindrical contour at the edges of the diffusion window and a spherical contour at the corners of the diffusion window. The depletion layer of the junction follows theses contours. The electric field distribution at the edges differs from the parallel lines representative of the parallel-plane portion. Since charge balance between the two sides of the junction must be established, the junction curvature leads to electric field crowding as illustrated in Figure 71. The higher electric field at the junction edges leads to larger impact ionization at the edges. Consequently, the breakdown of planar diffused junction can be expected to occur at the edges rather than in the parallel-plane portion.

14. Dependence of avalanche break down voltage on the curvature of the junction

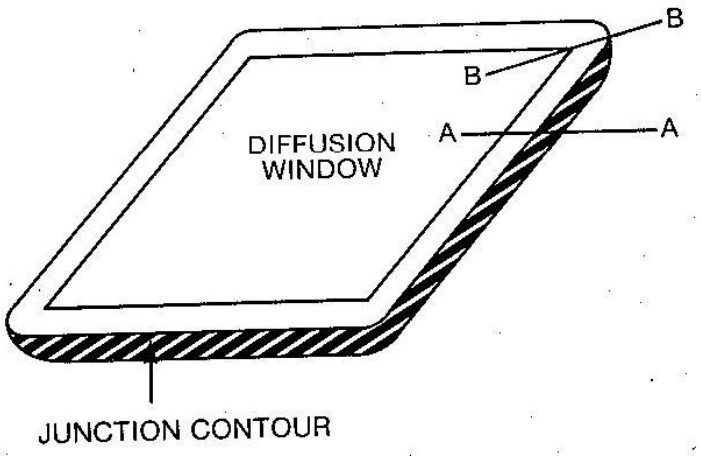


Figure 70 Planar junction formed by diffusion through a rectangular diffusion window

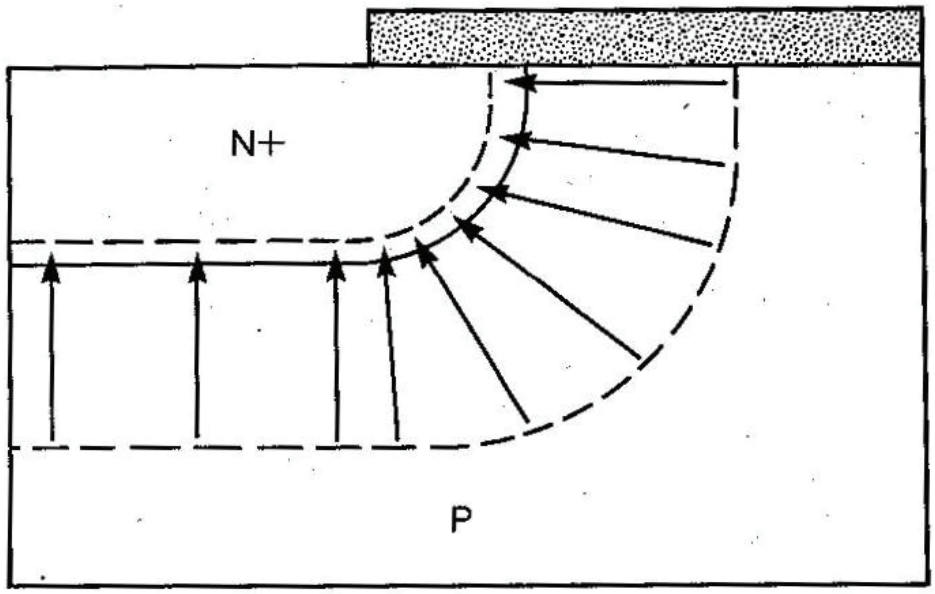


Figure 71 Electric field crowding at the edge of a cylindrical junction

14.1 Cylindrical Junction:

Consider the edge of the planar diffused junction shown in Figure 70. A cross section of this edge at *A-A* is illustrated in Figure 72. Here it is assumed that the lateral diffusion is equal to the vertical junction depth. The resulting cylindrical junction has a radius r_j. The depletion layer extends from this junction on the lightly doped side to a radius r_d. For the case of a highly doped diffused region, the depletion layer width on the diffused side can be neglected. Inside the depletion layer, Poisson's equation can be set up in cylindrical coordinates:

Equation 14.1
$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dV}{dr}\right) = -\frac{1}{r}\frac{d}{dr}(rE) = \frac{qN_A}{\varepsilon_s}$$

Where, the potential distribution *V(r)* and the electric field distribution *E(r)* are defined along a radius vector *r* extending into the depletion layer. The lightly doped side of the junction has homogeneous doping concentration N_A. Integration of this equation once with the boundary condition that the electric field must drop to zero at the edge of the depletion layer (i.e., at r_d) gives the electric field distribution:

Equation 14.3
$$E(r) = \frac{qN_A}{2\varepsilon_s}\left(\frac{r_d^2 - r^2}{r}\right)$$

As in the case of the parallel-plane junction, the maximum electric field occurs at the metallurgical junction:

Equation 14.4
$$E_m(r_j) = \frac{qN_A}{2\varepsilon_s}\left(\frac{r_d^2 - r_j^2}{r_j}\right)$$

This maximum electric field for the cylindrical junction can be substantially larger than the electric field in the parallel-plane portion. This can be illustrated easily for the case where the junction radius of curvature r_j is much smaller than the depletion layer width r_d. The maximum electric field is given approximately by

Equation 14.5
$$E_{m,CYL}(r_j) \cong \frac{qN_A}{2\varepsilon_s}\frac{r_d^2}{r_j}$$

Where, the subscript CYL refers to the cylindrical region of the junction. The corresponding maximum electric field in the parallel-plane portion is:

Equation 14.6 $$E_{m,PP}(r_j) = \frac{qN_A}{\varepsilon_s} r_d$$

Taking a ratio of these expressions, we obtain

Equation 14.7 $$\frac{E_{m,CYL}}{E_{m,PP}} \cong \frac{r_d}{2r_j}$$

This equation, valid for shallow junctions with small radii of curvature, indicates that the peak electric field at the cylindrical junction edge is substantially greater than in the parallel-plane portion. It also demonstrates that the effect of the cylindrical edge termination on the electric field becomes worse with increasing reverse bias applied to the junction. Avalanche breakdown is then confined to the edge because of the very strong dependence of the impact ionization coefficient on the electric field.

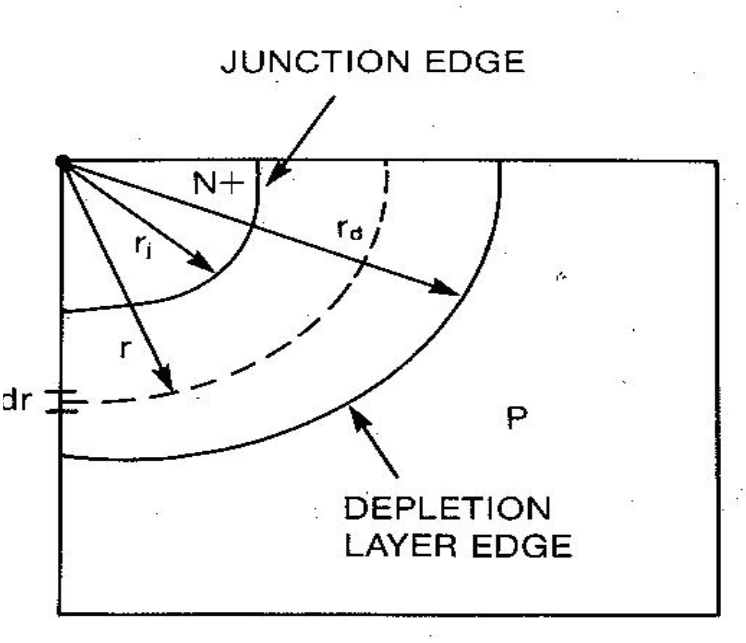


Figure 72 Depletion layer at edge of a cylindrical junction

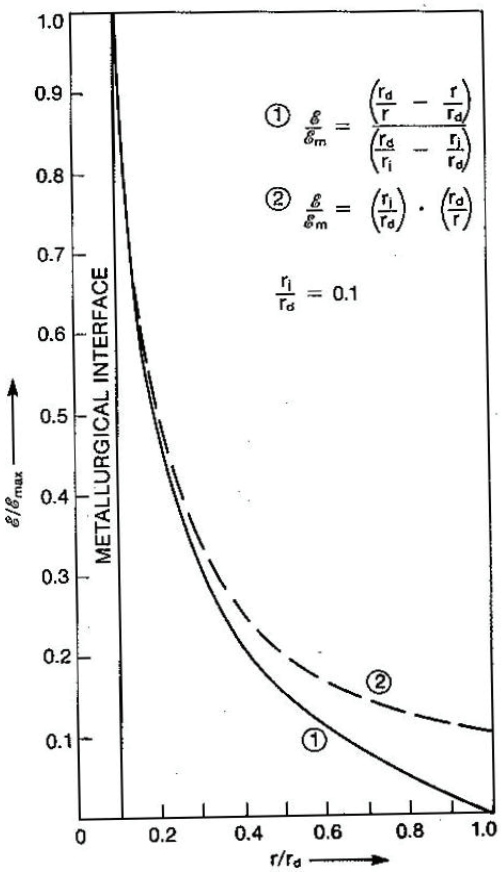
The potential distribution at the cylindrical junction termination can be obtained by integrating Equation 14.3:

Equation 14.8 $$V(r) = \frac{qN_A}{2\varepsilon_s}\left[\left(\frac{r_j^2 - r^2}{2}\right) + r_d^2 \ln\left(\frac{r}{r_j}\right)\right]$$

Using the boundary condition that the potential at $r=r_d$ must equal the applied reverse bias voltage; the depletion layer width can be derived from this equation.

To analyze the breakdown voltage of the cylindrical junction, it is necessary to solve the ionization integral by use of the electric field distribution given by Equation 14.3. A closed-form analytical solution cannot be derived by using Equation 14.3. However, a closed-form analytical solution can be obtained by utilizing an approximation to the electric field distribution that is based on the assumption that the impact ionization occurs primarily at the high electric field region close to the metallurgical junction. This assumption allows the approximation

Equation 14.9 $$E(r) = \frac{K}{r}$$



14. Dependence of avalanche break down voltage on the curvature of the junction

Figure 73 Comparison of hyperbolic electric field distribution to the actual electric field distribution of a cylindrical junction

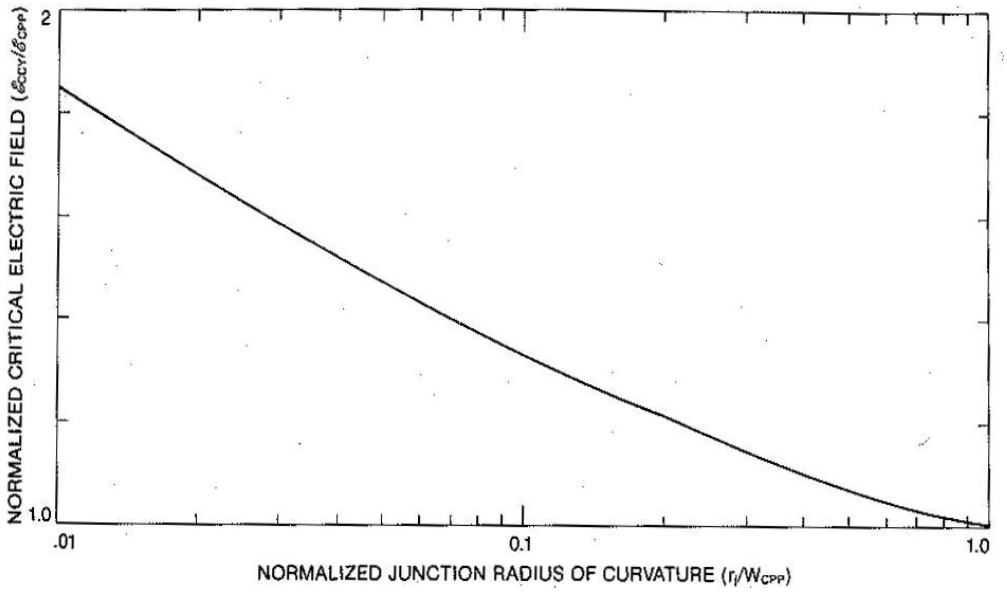


Figure 74 Normalized critical electric field for a cylindrical junction as a function of the normalized radius of curvature

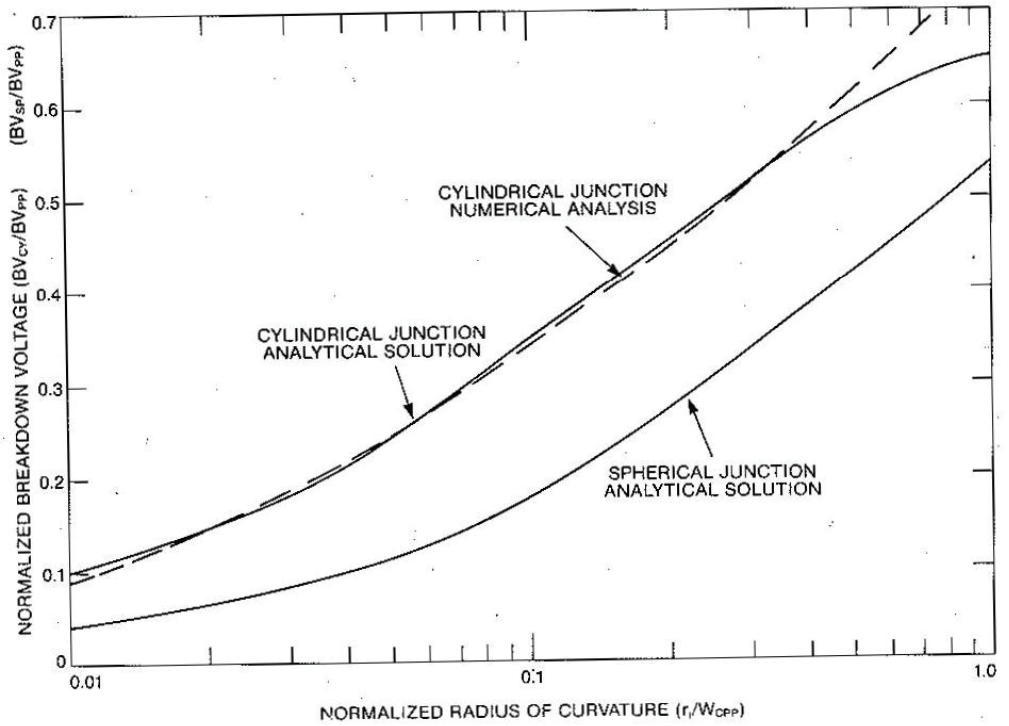


Figure 75 Normalized breakdown voltage of cylindrical and spherical junctions as a function of the normalized radius of curvature

This hyperbolic variation in the electric field distribution is compared with the actual field distribution in Figure 73. The important point to note is the similarity in the field distribution near the metallurgical junction for the two cases. However, the hyperbolic field distribution implies a depletion layer that extends to infinity. Thus the ionization integral must also be evaluated from r_j to infinity when Equation 14.9 is used. Solving the ionization integral, using the ionization coefficient given by Equation 14.10, an expression for the critical electric field at breakdown for the cylindrical junction can be derived (Equation 14.11):

Equation 14.10 $$W = 9.1\times10^{5} G^{-7/15}$$

Equation 14.11 $$E_{c,CYL} = \left(\frac{3.25\times10^{35}}{r_j} \right)^{1/7}$$

Equation 14.12 $$E_{c,PP} = 4010 N_A^{1/8}$$

It is useful to normalize this parameter to the critical electric field at breakdown for the parallel-plane case. Equation 14.12 and Equation 14.11 yield

Equation 14.13 $$\frac{E_{c,CYL}}{E_{c,PP}} = \left(\frac{3W_{c,PP}}{4r_j} \right)^{1/7}$$

This relationship is plotted in Figure 74. It provides a general expression for the critical electric field of cylindrical junctions irrespective of the specific background doping level.

Using the critical electric field at breakdown for the cylindrical junction, an expression for the breakdown voltage can be derived. It is useful to normalize the breakdown voltage of the cylindrical junction to the breakdown voltage of the parallel-plane case to obtain a general expression that is independent of the specific background doping level:

Equation 14.14 $$\frac{BV_{CYL}}{BV_{PP}} = \left\{ \frac{1}{2} \left[\left(\frac{r_j}{W_c} \right)^2 + 2 \left(\frac{r_j}{W_c} \right)^{6/7} \right] \ln \left[1 + 2 \left(\frac{W_c}{r_j} \right)^{8/7} \right] - \left(\frac{r_j}{W_c} \right)^{6/7} \right\}$$

This expression is plotted in Figure 75. It has been shown that the breakdown voltages obtained by using this equation are in good agreement with those calculated by numerical techniques for a wide range of radii of curvature and background doping level, as long as the radius of curvature is smaller than the depletion width at breakdown for the parallel-plane case and the background doping level is below 1 x 10^{16}/cm^3. This covers most of the practical junctions used for power device fabrication.

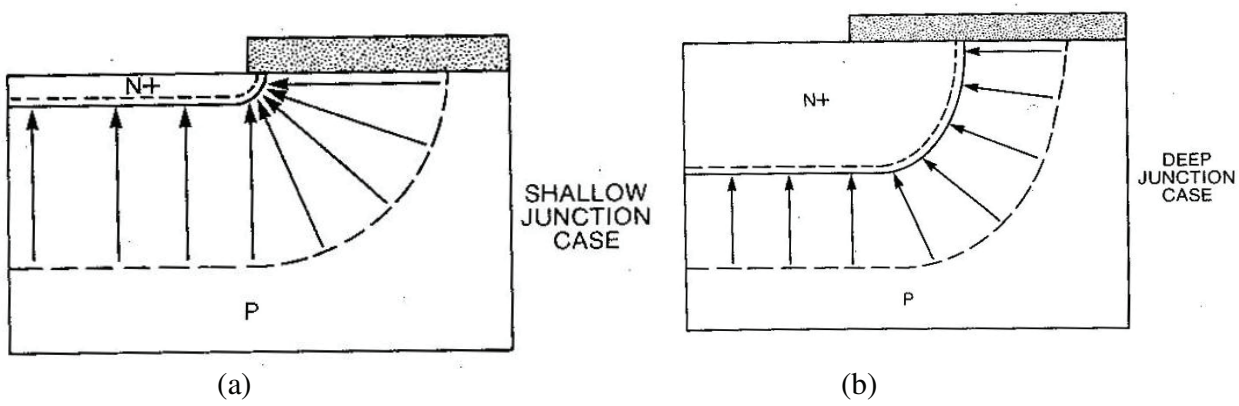


Figure 76 Electric field crowding at the edges of (a) shallow and (b) deep junction

Numerical solutions for the avalanche breakdown of cylindrical junctions have been obtained, including the effect of the diffusion profile. It has been shown that normalization of the critical electric field and breakdown voltage to the corresponding values for a semi-infinite diffused junction also results in condensation of all the data into a single curve. This curve is shown by the dashed lines in Figure 75. To obtain this curve, the radius of curvature was normalized to the depletion layer width at breakdown on the lightly doped side of the junction for the parallel-plane case. An empirical expression that fits the curve is

Equation 14.15

$$\frac{BV_{CYL}}{BV_{PP}} = \left[0.871 + 0.125 \ln\left(\frac{r_j}{W_{c,PP}} \right) \right]^2$$

From Figure 75, it can be seen that Equation 14.14, which was obtained from the closed-form analytical solution, provides nearly identical results.

From the preceding analysis and Figure 75, it can be seen that the avalanche breakdown voltage of planar diffused junctions is always smaller than for the semi-infinite (parallel-plane) case. As the radius of curvature (i.e., the diffusion depth of the junction) increases, the breakdown voltage increases and begins to approach the parallel-plane case. The reason for this can be pictorially illustrated by comparing the electric field distribution of a shallow junction with that of a deep junction for the same background doping level. These cases will both have the same depletion widths on the lightly doped side for a given applied reverse-bias voltage as shown in Figure 76. However, the electric field lines show much greater crowding, indicating a higher local electric field for the shallow junction because the positive charge in the N^+ diffused region, on which the field lines terminate, is located at a point close to the surface instead of being spread out along a wide junction contour as in the case of the deep junction. The enhanced crowding of the electric field lines for the shallow

junction is responsible for its lower breakdown voltage compared to the deeper junction. From Figure 76 it can also be deduced that the crowding of the electric field lines is not determined by the absolute junction depth, but by its size relative to the depletion layer width. This is why normalization of the junction depth to the depletion layer width is effective in producing the elegant general expressions for breakdown of cylindrical junctions provided in Equation 14.14 and Equation 14.15. It can be further concluded that shallower junctions can be used for the fabrication of low-voltage devices whereas high-voltage devices will require the extra processing steps that are usually necessary to obtain deep junctions.

For typical high-voltage devices, the depletion layer widths range from 20 to 50 µm, whereas practical planar process technology limits the junction depths to less than 10 µm. The ratio (r_j/W) for practical devices is typically less than 0.5 and may range down to less than 0.1. It is apparent from Figure 75 that a cylindrical junction termination would yield breakdown voltages of less than half of the parallel-plane case under these circumstances. Methods to overcome this problem by using field rings and field plates are described later in the chapter.

14.2 Spherical Junction:

A planar junction formed by diffusion through a rectangular window is shown in Figure 70. A cylindrical junction forms at the edges illustrated by the cross section taken at *A-A*. At the corners of the diffusion window the junction takes the form of one-quarter of a spheroid with a radius of curvature equal to the junction depth, if the lateral diffusion is assumed to be equal to the diffusion depth. The crowding of the electric field lines at the corners can be intuitively expected to be worse than at the edges because the field lines approach a point from three dimensions instead of a line from two dimensions. The breakdown voltage of this region of the planar junction can be analyzed by solution of Poisson's equation in spherical coordinates:

Equation 14.16
$$\frac{1}{r^2}\frac{d}{dr}\left(r^2\frac{dV}{dr}\right)=-\frac{1}{r}\frac{d}{dr}\left(r^2E\right)=\frac{qN_A}{\varepsilon_s}$$

Integrating this equation and using the boundary condition that the electric field is zero at the edge of the depletion layer (r_d), the electric field distribution can be derived:

Equation 14.17
$$E(r)=\frac{qN_A}{3\varepsilon_s}\left(\frac{r_d^3-r^3}{r^2}\right)$$

The maximum electric field for the spherical junction occurs at the metallurgical interface and is given by

Equation 14.18
$$E_m\left(r_j\right)=\frac{qN_A}{3\varepsilon_s}\left(\frac{r_d^3-r_j^3}{r_j^2}\right)$$

As in the case of the cylindrical junction, this maximum electric field is substantially greater than in the parallel-plane portion. If a junction with small radius of curvature compared with the depletion width is considered, the electric field can be approximated by

Equation 14.19
$$E_{m,SP}\left(r_j\right)\cong\frac{qN_A}{3\varepsilon_s}\frac{r_d^3}{r_j^2}$$

Normalization of this expression to the maximum electric field in the parallel-plane portion of the junction gives

Equation 14.20
$$\frac{E_{m,SP}}{E_{m,PP}}=\frac{1}{3}\left(\frac{r_d}{r_j}\right)^2$$

The maximum electric field at the spherical portion of the junction is thus substantially greater than in the parallel-plane portion. This difference in the electric field increases as the reverse bias increases because the depletion width increases. Avalanche breakdown at the corners of the planar diffusion will supersede breakdown at the parallel-plane portion.

A comparison with the cylindrical portion of the junction is also useful. Use of Equation 14.5 and Equation 14.19 gives

Equation 14.21

$$\frac{E_{m,SP}}{E_{m,CYL}} = \frac{2}{3}\left(\frac{r_d}{r_j}\right)$$

Thus the maximum electric field in the spherical portion of the planar diffused junction is larger than that at the cylindrical portion. Consequently, the planar junction will break down first at the corners where the spherical junctions are formed.

The breakdown voltage of a planar diffused junction formed using a rectangular diffusion window can be obtained by integrating Equation 14.17:

Equation 14.22

$$V(r) = \frac{qN_A}{3\varepsilon_s}\left[\left(\frac{r_j^2 - r^2}{2}\right) + r_d^3\left(\frac{1}{r_j} - \frac{1}{r}\right)\right]$$

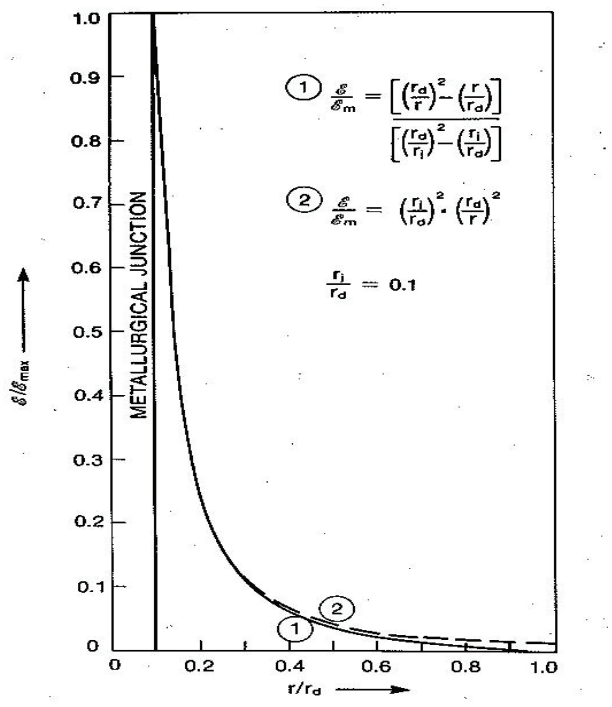


Figure 77 **Comparison of the electric field distribution used to obtain analytical solution (dashed lines) for the breakdown of spherical junctions with the actual (solid line) electric field distribution**

The depletion layer width can be obtained from this equation by using the boundary condition that the voltage at $r=r_d$ must be equal to the applied potential across the junction. To obtain the avalanche breakdown voltage, it is necessary to solve the ionization integral by use of the electric field distribution given by Equation 14.17. A closed-form analytical solution has been derived by using the approximation

Equation 14.23
$$E(r) = \frac{K}{r^2}$$

This is based on the fact that the impact ionization is confined close to the metallurgical junction. The electric field distribution described by Equation 14.23 is compared with the actual distribution in Figure 77. As in the case of the cylindrical junction, the similar field distribution near the metallurgical junction, where the impact ionization is predominant, allows the use of this approximation. Performing the ionization integral from r_i to infinity by use of Equation 14.23 gives the critical electric field for breakdown of spherical junctions:

Equation 14.24
$$E_{c,SP} = \left(\frac{7.0 \times 10^{35}}{r_j} \right)^{1/7}$$

Normalization of this field to the critical electric field at breakdown for the parallel-plane case gives

Equation 14.25
$$\frac{E_{c,SP}}{E_{c,PP}} = \left(\frac{13}{8} \frac{W_c}{r_j} \right)^{1/7}$$

This relationship is plotted in Figure 78. It provides a general expression for the critical electric field at breakdown for the spherical junction irrespective of the background doping level. The breakdown voltage of spherical junctions can be derived from the critical electric field at breakdown. Normalization of this voltage to the parallel-plane case gives a general expression that is independent of the background doping level:

Equation 14.26
$$\frac{BV_{SP}}{BV_{PP}} = \left(\frac{r_j}{W_c} \right)^2 + 2.14 \left(\frac{r_j}{W_c} \right)^{6/7} - \left[\left(\frac{r_j}{W_c} \right)^3 + 3 \left(\frac{r_j}{W_c} \right)^{13/7} \right]^{2/3}$$

14. Dependence of avalanche break down voltage on the curvature of the junction

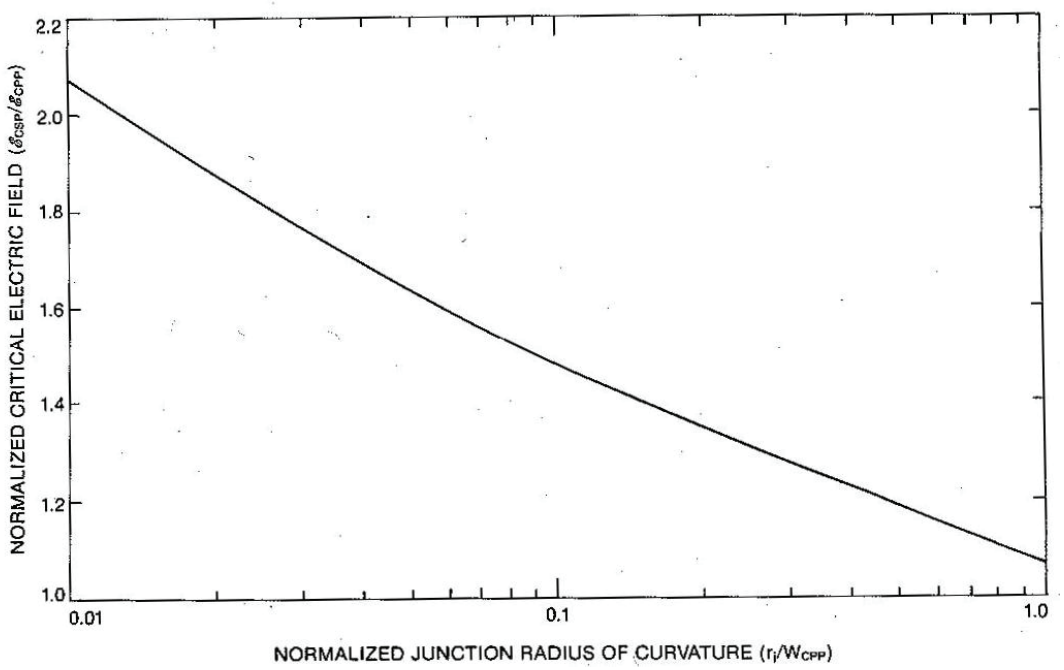


Figure 78 Normalized critical electric field for breakdown of a spherical junction

This expression is plotted in Figure 75 for comparison with the cylindrical junction. In general, the breakdown voltage of the spherical junction is found to be about a factor of 2 times lower than that of the cylindrical junction. The creation of spherical junctions at device terminations must, therefore, be avoided. Since the spherical junction is caused by the presence of sharp corners, as at the edges of the rectangular diffusion window in Figure 70, such junctions can be avoided by rounding the devices edges. However, this results in loss in the active junction area by

Equation 14.27 $\textbf{Area loss} = (4-\pi)\,R^2$

Where, "*R"* is the radius of curvature of the corner. To obtain the full benefits of rounding the corners during mask design, it is essential to make the radius of curvature *R* several times larger than the depletion width at breakdown.

Index of figures

List of symbols

BV_{BD}- Breakdown voltage

E_{BD}- Electric field at break down

I_C- collector current

I_E- emitter current

I_{CO}- leakage current

I_{CS}- reverse saturation current

I_A- anode current

I_G- gate current

μ_n- mobility of electrons

μ_p- mobility of holes

τ- Life time

tt- Carrier transit time

α- Common base current gain

β- Common emitter current gain

α_f- base transport coefficient in forward bias

α_r- base transport coefficient in reverse bias

$R_{\blacksquare}$- Sheet resistance

V_T- $\frac{KT}{q}$

K - Boltzmann constant

T - Absolute temperature

q- Unit charge

ε- Absolute permittivity

f - Electric field

N_A^- - ionized acceptor concentration

N_D^+- ionized donor concentration

n_m- mobile electron concentration

p_m- mobile hole concentration

Θ - Specific heat

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Abbreviations

AG	Amplifying Gate
LTT	Light Triggered Thyristor
ETT	Electrically Triggered Thyristor
GTO	Gate Turn OFF thyristor
MCT	MOS Controlled Thyristor
HVDC	High Voltage DC transmission
SVC	Static VAR Compensation
PD	Partial Discharge