

Dissertation

Timo Schary

Capacitive Surface-Micromachined Pressure Sensors
on Fused Silica

Contributions to Micromachining on Fused Silica

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Capacitive Surface-Micromachined Pressure Sensors on Fused Silica

Contributions to Micromachining on Fused Silica

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Dipl.-Ing. Timo Schary
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Referent: Prof. Dr.-Ing. Wolfgang Benecke
Korreferent: Prof. Dr.-Ing. Walter Lang

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Abstract

Miniaturized capacitive pressure sensors fabricated by means of surface micro-machining on fused silica are presented. The special non-conductive substrate is selected to eliminate all parasitic capacitances to the bulk. This renders the presented sensor a floating two-terminal capacitor with low offset capacitance and offers design freedom for electrical tracks and bond pads. The presented transducer can be cost-effectively fabricated and integrated into systems as a non-polar pressure dependent capacitance. Prototypes have lateral dimensions of $0.6 \times 1.2 \text{ mm}^2$ and a thickness of 0.5 mm which can be reduced to 0.17 mm on wafer level. The measured average normal- and touch mode sensitivities of $2 \text{ pF}/\text{bar}$ and $1.8 \text{ pF}/\text{bar}$, respectively, provide enough output swing for ambient pressure monitoring with a 1/10 mbar resolution using a discrete AD7745 readout circuit on PCB.

Processing on fused silica is discussed in detail with a focus on surface micromachining. Substrate material related process challenges are addressed such as high film stress levels as well as viscous and elastic deformation. The substrate's general features are a high thermal stability, a good electrical and thermal insulation, and a high transparency. In contrast to other glasses such as Pyrex[®], silica has a high softening temperature of 1600 °C enabling long-term processes at temperatures up to 800 °C. This feature is utilized and LPCVD films are used as functional layers. Silicon rich nitride and in situ boron-doped poly-silicon are important films of this work and are discussed in detail. It is shown that the stress homogeneity of nitride and its insulation quality improves on silica. The stress of crystalline as-deposited in situ boron-doped poly-silicon can be reproducibly annealed to low tensile levels. Both benefits are ultimately caused by the silica's thermal expansion coefficient of $0.5 \times 10^{-6} \text{ 1/K}$. It is lower than the coefficient of silicon therefore thermal stress levels of all common deposits increase on fused silica. High stress leads to film thickness limitations and the requirement of highly selective wet chemical etch procedures. These are tuned to pattern LPCVD TEOS oxide and poly-silicon on SiN_x with either high selectivity ($\text{TEOS}:\text{SiN}_{1.04} = 1.6 \times 10^3$) or with reproducible undercut.

Analytic formulas tailored for surface micromachined circular plates are presented. Topography, stress, and a limited displacement magnitude are incorporated by means of normalization. The presented approach leads to a new solution for plates in touch-mode. The transducer capacitance is derived accounting for a dielectric stack with surface roughness, and concentrically decreasing insulation thickness. The presented theory is concluded with a discussion of general characteristics of capacitive circular plate transducers in normal- and touch-mode.

The fabricated sensor prototypes are simulated with SPICE demonstrating that the complex geometry can be adequately represented by a lumped discrete three components model. Simulation data is compared to wafer and package level test results. The presented data indicates a small offset and sensitivity spread over the wafer and high achievable fabrication yields. Hysteresis is shown to be a general issue in touch-mode operation and is related to surface forces. Touch-mode hysteresis, sensitivity, and absolute magnitude of capacitance are demonstrated to greatly depend on the sealing procedure and surface roughness of the electrode insulation.

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Nomenclature

Greek Symbols

α	thermal expansion coefficient
$\bar{\alpha}$	thermal expansion coefficient (average)
α_F	thermal expansion coefficient of film
α_ϵ	temperature coefficient of permittivity
α_{Si}	temperature coefficient of silicon band gap
α_S	thermal expansion coefficient of substrate
β	apparent gap widening (effect of dielectric)
γ	plate support compliance
γ_σ	stress gradient (average)
Γ_σ	stress gradient (average, normalized)
δ	ratio of film and substrate thickness
ϵ_{At}	error of <i>Atkinson's</i> equation
ϵ_k	error of stress indicator k
ϵ_n	error of stress indicator n
ϵ_{FS}	error of stress measurement on fused silica
ϵ_{Si}	error of stress measurement on silicon
ϵ_{St}	error of <i>Stoney's</i> equation
ϵ	permittivity
ϵ_0	permittivity of free space
ϵ_{cSi}	permittivity of crystalline silicon
ϵ_i	permittivity of insulation
ϵ_{Nit}	permittivity of silicon nitride
ϵ_{Nit0}	permittivity of silicon nitride (at $T = 20^\circ\text{C}$)
ϵ_{pSi}	permittivity of poly-silicon
ϵ_r	permittivity of rough interface material
ϵ_{reff}	permittivity of rough interface (effective average)
ϵ_s	permittivity of sealant
ϵ	strain
$\Delta\epsilon$	difference of strain
$\epsilon^{(beam)}$	strain of indicator beam
ϵ_e	strain (external)
ϵ_F	strain of film
ϵ_{FS}	strain of fused silica
ϵ_{Si}	strain of silicon
ζ	area ratio (voids/rigid matter)
η	dynamic viscosity
θ	stress gradient indicator angular tip displacement
ϑ	slope at plate support
κ	scaling coefficient (large deflection)
λ	mean free path
λ_{th}	thermal conductivity
λ_i	<i>Debye</i> length (intrinsic)
μ_{eff}	carrier mobility (effective)

ξ	ratio of film and substrate biaxial moduli
ρ_{SiO_2}	density of silicon oxide
ρ	density
ρ_{air}	density of air
$\rho_{\text{air}0}$	density of air (mean at sea level)
ρ_{Hg}	density of mercury
ρ_{b}	resistivity of bottom-electrode poly-silicon
ρ_{poly}	resistivity of poly-silicon
ρ_{SiN}	resistivity of silicon nitride
ρ_{t}	resistivity of top-electrode poly-silicon
σ_{CVD}	sticking coefficient
σ_{pSi}	conductivity of poly-silicon
σ	mechanical stress
σ_0	stress coefficient (bending)
σ_{a}	stress at annealing temperature
$\sigma_{\text{a}0}$	stress at annealing temperature (initial)
σ_{e}	stress (external)
σ_{F}	film stress
σ_{i}	intrinsic stress
σ_{M}	membrane stress
$\sigma_{\text{m}0}$	stress coefficient (membrane stress)
Σ_{M}	membrane stress (normalized)
σ_{mr}	radial membrane stress
σ_{mt}	transverse membrane stress
σ_{R}	radial bending stress
Σ_{R}	radial bending stress (normalized)
σ_{FS}	film stress on fused silica
σ_{Si}	film stress on silicon
σ_{t}	thermal stress
$\Delta\sigma_{\text{t}}$	difference of thermal stress on silicon and silica
$\sigma_{\text{t}(\text{FS})}$	thermal stress on fused silica
$\sigma_{\text{t}(\text{Si})}$	thermal stress on silicon
σ_{T}	transverse bending stress
Σ_{T}	transverse bending stress (normalized)
$\sigma^{(\text{yield})}$	yield stress
σ_{∞}	stress at $t \rightarrow \infty$
τ	viscous relaxation time scale
ν	<i>Poisson's number</i>
ν_{F}	<i>Poisson's number of film</i>
ν_{S}	<i>Poisson's number of substrate</i>
Φ	potential barrier
φ	phase difference
ψ_{M}	membrane stress function
Ψ_{M}	membrane stress function (normalized)
ψ_{s}	surface band bending
ω	angular frequency

Latin Symbols

a_θ	stress gradient indicator linear coefficient (angular tip displacement)
a_x	stress gradient indicator linear coefficient (lateral tip displacement)
A_r	area of rigid matter
$A^{(\text{skin})}$	area of skin
A_v	area of voids
b_θ	stress gradient indicator exponent (angular tip displacement)
b_x	stress gradient indicator exponent (lateral tip displacement)
$C^{(\text{down})}$	capacitance (down-sweep)
C_g	capacitance of gap (vacuum)
C_i	capacitance of insulation
$C^{(\text{max})}$	pressure dependent sensor capacitance (maximum)
$C^{(\text{mean})}$	capacitance (mean of up- and down-sweep)
C_n	pressure dependent sensor capacitance (normal-mode)
$C_n^{(\text{max})}$	pressure dependent sensor capacitance (normal-mode, $p + p_t$)
$C^{(\text{normal})}$	overall capacitance (normal-mode)
C_{nt}	capacitance of plate section <i>not</i> touching bottom-electrode
C_{offset}	sensor offset capacitance
C_p	parallel capacitance
$C_p^{(\text{corrected})}$	parallel capacitance (corrected for series resistance)
C_s	capacitance of sealant
C_{sensor}	pressure dependent capacitance (touch- and normal-mode)
C_t	capacitance of plate section touching bottom-electrode
$C^{(\text{touch})}$	overall capacitance (touch-mode)
$C^{(\text{up})}$	capacitance (up-sweep)
C_z	capacitance scale (zero pressure load, $r_b = r_{\text{max}}$)
c	capacitance (per unit area)
c_i	capacitance of insulator (per unit area)
c_{Si}	capacitance of depletion layer (per unit area)
C_f	constant relating grain boundary energy and force
C_H	stress indicator hinge correction coefficient
c_B	concentration of boron
c_H	concentration of hydrogen
D	flexural rigidity
d_c	diameter of silicon crystal (average)
d_{c_0}	diameter of silicon crystal (average, initial)
\mathcal{D}	diffusivity
\mathcal{D}_0	pre exponential coefficient (diffusivity)
d_S	diameter of substrate
E	electric field
E	<i>Young's</i> modulus
E_F	<i>Young's</i> modulus of film
E_F'	biaxial modulus of film
E_S'	biaxial modulus of substrate
E_A	activation energy

E_η	empiric activation energy of viscous relaxation
E_F	<i>Fermi</i> level (extrinsic)
E_f	<i>Fermi</i> level (intrinsic)
E_g	band gap
E_{g0}	band gap (at 0 K)
E_{kin}	kinetic energy
E_t	energy level of trap
E_B	barrier hight
E_{gb}	energy of grain boundary (average)
F	electric field (dimensionless)
f_s	electric field at semiconductor surface
G	shear modulus
g	acceleration of gravity
g_0	acceleration of gravity (45° latitude)
R_{air}	gas constant of dry air (specific)
h	altitude
h_b	wafer deflection
h_{b0}	wafer deflection (initial)
\mathcal{H}	thickness of transducer plate (normalized)
H	hysteresis
$H^{(max)}$	hysteresis (maximum within pressure range)
J	current density
J_1	current density (field enhanced excitation)
J_2	current density (field ionization)
J_3	current density (thermally excited hopping)
K	wafer curvature
k	<i>Boltzmann</i> constant
K_n	<i>Knudsen</i> number
$K^{(elastic)}$	scaling coefficient (elastic support)
$K^{(large)}$	scaling coefficient (large deflection)
ℓ	typical feature dimension
L_B	length of stress indicator beam
L_H	length of stress indicator hinge
L_P	length of stress indicator pointer
L_S	length of stress gradient indicator spiral
M	grain boundary mobility
M_0	grain boundary mobility (pre exponential coefficient)
m	mass
m^*	mass of charge carrier (effective)
m_u	mass (molecular)
m_n	mass of electron (effective)
m_p	mass of hole (effective)
M_{SiO_2}	mass of silicon oxide (molar)
m_0	bending moment coefficient
m_R	radial bending moment
m_r	radial bending moment (dimensional r)

M_R	radial bending moment (normalized)
$M_R^{(\text{elastic})}$	radial bending moment (elastic support, normalized)
m_T	transverse bending moment
m_t	transverse bending moment (dimensional r)
M_T	transverse bending moment (normalized)
$M_T^{(\text{elastic})}$	transverse bending moment (elastic support, normalized)
N	dopant density
n_{H_2}	amount of substance (hydrogen)
n_{SiO_2}	amount of substance (silicon oxide)
n	refractive index
n_{Si}	refractive index of silicon
$n_{\text{Si}_3\text{N}_4}$	refractive index of stoichiometric nitride
N	number of molecules
N_A	acceptor density
N_B	number of adsorbed boron atoms
N_{Si}	number of adsorbed silicon atoms
N_c	number of crystal bonds
N_D	donator density
N_f	number of free adsorption sites
n_i	carrier density (intrinsic)
N_c	density of states (conduction band)
N_n	number of nucleation bonds
N_v	density of states (valence band)
N_o	number of occupied adsorption sites
N_{o+f}	number of adsorption sites (total)
N_Q	surface charge density
N_S	stress indicator sprocket count
\bar{p}	carrier density (average)
p_b	carrier density within grain bulk
P_H	stress indicator hinge pitch
P_N	stress indicator nonius pitch
p_0	air pressure (mean at sea level)
p	pressure
P	pressure (normalized)
p_{cav}	pressure in sensor cavity
p_d	deposition pressure
$P^{(\text{elastic})}$	scaled pressure load (elastic support, normalized)
$P^{(\text{large})}$	scaled pressure load (large deflection, normalized)
$P^{(\text{max})}$	maximum pressure causing capacitance change (normalized)
$p_t^{(\text{real})}$	touch-down pressure of the real transducer
p_t	touch-down pressure
P_S	stress indicator sprocket pitch
Q	shearing force
q	elementary charge
Q_t	density of traps
q_i	insulator charge density

q_s	surface charge density
r_b	radius of bottom-electrode
R_b	radius of bottom-electrode (normalized)
r	radial distance
R	radial distance (normalized)
Δr	stress gradient indicator radial tip displacement
R^*	universal gas constant (molar)
R	gas constant (specific)
r_{\max}	radius of transducer plate
r_t	touch-radius of transducer plate
R_t	touch-radius of transducer plate (normalized)
R_0	rate coefficient
r_c	crystallization rate
r_d	deposition rate
r_{d-Si}	deposition rate of silane
r_n	nucleation rate
r_{re-c}	recrystallization rate
R_{CVD}	SiH ₂ Cl ₂ /NH ₃ -ratio
$r^{(earth)}$	earth radius (effective)
R_{cb}	contact resistance metallization/bottom-poly-silicon
R_{ct}	contact resistance metallization/top-poly-silicon
R_p	parallel resistance
$R_p^{(corrected)}$	parallel resistance (corrected for series resistance)
R_s	series resistance
$R_{\square top}$	resistance of top-poly-silicon (in ohms/square)
R_H	radius of stress indicator hinge
r_r	plate curvature (radial)
r_t	plate curvature (transverse)
r_x	plate curvature (x-plane)
r_y	plate curvature (y-plane)
S_i	sensitivity of stress indicator
$\bar{S}^{(normal)}$	sensitivity (average, normal-mode)
$\bar{S}^{(touch)}$	sensitivity (average, touch-mode)
t	time
T	temperature
T_0	temperature (mean at sea level)
$T^{(anneal)}$	annealing point of glass
T_a	annealing temperature
T_d	deposition temperature
$T^{(melt)}$	melting point
$T^{(soft)}$	softening point of glass
$T^{(strain)}$	strain point of glass
T_t	amorphous/crystalline transition temperature
$T^{(work)}$	working temperature of glass
T_z	absolute zero
t_F	film thickness

t_b	thickness of bottom-electrode
t_c	thickness of etch channel layer
t_i	thickness of insulation (within sensor cavity)
t_{res}	thickness of residuals
t_s	thickness of sealant (within sensor cavity)
t_{ss}	thickness of sacrificial layer (shrinked)
t_S	substrate thickness
u	molecule velocity
U_b	bulk potential (dimensionless)
U_s	surface potential (dimensionless)
V	volume
V_g	gate voltage
V_{ms}	work function difference
$V^{(cavity)}$	volume of sensor cavity
V_m	molar volume
$V^{(seal)}$	volume of sealant
V_t	temperature voltage
W_0	center deflection (normalized)
w_{gap}	travel range of transducer plate (no stress)
w_{max}	maximum possible plate deflection
$W^{(clamped)}$	deflection of midplane (rigid support, normalized)
$W^{(elastic)}$	deflection of midplane (elastic support, normalized)
$W^{(large)}$	deflection of midplane (large deflection, normalized)
W	deflection of midplane (normalized)
w	deflection of midplane
$W^{(simply)}$	deflection of midplane (simply supported, normalized)
$W^{(touch)}$	deflection of midplane (touch-mode, normalized)
w_{min}	minimum plate deflection at 0 bar
w_b	width of bottom lead
W_H	width of stress indicator hinge
W_P	width of stress indicator pointer
x	stoichiometric index of silicon nitride
Δx	stress gradient indicator lateral tip displacement
x_S	stoichiometric index of Si_3N_4
ϕ_m	metal work function
ϕ_{Si}	silicon work function
Z	impedance
z_{Hg}	mercury column height
z_{Hg0}	mercury column height (zero level)

*The farther backward you can look,
the farther forward you are likely to see.*

Sir Winston Leonard Spencer Churchill

1

Introduction

PRESSURE SENSORS have already been developed over decades. They are commercially available in all sizes, for almost every environmental condition and have been fabricated in a vast variety of technologies. The first successfully commercialized MEMS product was a piezoresistive pressure sensor and a large number of companies exist producing pressure sensors worldwide for low- and high-volume applications. Considering this the question arises: Why is there still the need to have another thesis about pressure sensors? What more is to be developed and to be improved? Maybe it's similar to the 90:10 rule: 90 percent improvement is attained with only 10 percent effort but the final 10 percent performance gain requires 90 percent of development time. So there is still enough to be improved and adopted to the changing society and market. This thesis is structured as follows:

- Chapter 1: Introduction** The chapter covers background information on the history of pressure sensors, provides data about possible markets and applications as well as a summary of relevant MEMS pressure sensor implementations. The present work is motivated and an outline is given.
 - Chapter 2: Micromachining on fused silica** Non-conductive substrate alternatives to silicon are discussed and fused silica is chosen for the present work. General technological aspects of processing on fused silica are presented together with process details relevant for the developed sensor.
 - Chapter 3: Capacitive pressure sensor** Design and process flow for the developed capacitive pressure sensor on fused silica are discussed. Analytical models for the transducer plate deflection in normal- and touch-mode are derived and compared to numerical simulation data. The electrical and physical sensor characteristics are matched to a *SPICE* model and a simplified equivalent circuit.
 - Chapter 4: Conclusion** The chapter concludes this thesis and summarizes the achievements but also the remaining issues. A new version of a capacitive pressure sensor was developed. Did it pay off and was it worthwhile?
- Appendices:** An extra section for each chapter of this work can be found in the appendix containing additional information.

The introduction of this chapter will put together the objectives of this thesis. But before going into technological details, the historical background of the physical quantity pressure and its measurement will be summarized. In addition, the history of MEMS pressure sensors will be briefly discussed and concluded with relevant examples of recent pressure sensors. Beside the technical view, this chapter tries to find out who requires the vast number of currently about 178 million MEMS pressure sensor units per year.¹

1.1 Torricelli, Pascal, v. Guericke, Boyle and many more

The existence of vacuum and the idea of air exerting a pressure on everything in touch with was accepted quite late in the middle of the 17th century. This might seem surprising, because pressure influences many of the phenomena encountered in daily life. What made it difficult to perceive? Pressure can not be seen or felt, it is experienced indirectly: vessels do swim in water or hot air moves upwards. The fact that many of the old and famous thinkers did not believe in the existence of a vacuum made it even harder to come up with the truth. *Aristotle* (384-322 BC) and *Plato* (427-347 BC) did not believe in emptiness [Gri03][Sch88]. *René Descartes* (1596-1650), who lived at the time when air pressure was measured for the first time and the existence of vacuum was proven experimentally, neglected the existence of a void.² He had the notion of a very fine and thin liquid filling up all existing gaps within substances and filling up the whole universe similarly. He maintained his assumption although it contradicted experiments of the physicists who worked on this topic and contributed to our current understanding of pressure and vacuum. *Galileo Galilei* (1564-1642) did not have the notion of air pressure, too. He neglected air pressure, when it was suggested to him, as reason for 'malfunctioning' water suction pumps which were not able to raise water higher than 9 m. *Galileo* believed in the water to be glued to the pump's piston. This glue, he believed, was due to nature's abhorrence of vacuum.³ In his eyes, the problem was that this glue had a finite resistance and started to measure its bond strength by experimenting with different liquids.

Evangelista Torricelli (1608-1647) was a late student of *Galilei* and replaced him in 1642 as professor of mathematics in Florence. *Galileo* introduced him to the head limit problem of water supply systems driven by suction pumps. After *Galileo's* death *Torricelli* came up with the idea, that the water is pushed up the pipe by the surrounding air. He thought of an equilibrium of forces, a balance of the water column weight and the pressure on its surface. He concluded that a heavier liquid than water must have a lower head limit inversely proportional to its density. *Torricelli* and *Vincenzo Viviani*, a second former student of *Galilei*, filled mercury in a tube which was sealed on one end. They flipped the tube over and placed the open end in a bath of mercury (see Fig. 1.1). *Torricelli* predicted the height of the liquid

¹ Data of the year 2004 taken from [Wic06].

² *Descartes* did only believe in a "vacuum existing in the heads of its inventors".

³ It was believed that nature exerts a force to prevent a vacuum in horror of the void. This phenomenon was called the 'horror vacui'.



Fig. 1.1: The first barometer invented by *Evangelista Torricelli* in 1643. The mercury column height \overline{DB} in a sealed glass tube standing upside down in a mercury bath *C* does not depend on the tip vacuum volume *E* (i.e. $\overline{DB} = \overline{DA}$) but is proportional to the ambient air pressure (picture is taken from [BS97]).

column to be approximately 1/14th of the water column height correctly, since mercury has roughly 14 times the density of water. He experimented with different tube tip geometries to prove the mercury column height's independence of the tube's geometry. *Evangelista Torricelli* invented the barometer in 1643 and created by the way the first controlled vacuum.⁴ The height of the liquid column that settles down in a closed pipe as developed by *Torricelli* is a measure for the ambient pressure and is named after him (see Appendix A.3 for the conversion between common pressure units).⁵

The experiments conducted by *Torricelli* were convincing and a few opponents admitted that the mercury could possibly be pushed up by air pressure, but still insisted on the 'horror vacui'. *Blaise Pascal* (1623-1662) repeated the experiments of his Italian colleague and tried to figure out new experiments to prove that the disbelievers were wrong. He introduced a number of new thoughts [Sam75]:

Blaise Pascal

1. Air has a weight and does not extend infinitely into space, hence, the weight of air is finite.
2. Air can be compared to the ocean. Its weight lasts on the whole surface of the earth and its local weight changes with altitude.
3. It can not be concluded that water is weightless from the fact that animals, living in water, do not feel its weight. Similarly, it can not be concluded that air is weightless.

⁴ The pressure in the tip of the tube was equal the vapor pressure of mercury at room temperature (approximately 10^{-3} mbar).

⁵ Although *Torricelli* invented the barometer, its name was coined later by *Robert Boyle*. Electronic scans of *Torricelli's* original work related to geometry can be found at [ECH07] and [The07].

4. Comparing a large pile of wool with air, and finding that the wool at the bottom of the heap is compressed, leads to the conclusion that air pressure also changes with altitude.
5. Wool taken from the bottom of the pile, and kept under pressure while carried to the top of the heap, will extend there when not confined anymore. Air should be expected to change its volume similarly.

Pascal deduced, if the mercury height measured with the barometer would change with altitude, it would prove the influence of the air's weight. At the same time, it would disprove all other hypotheses stating that the arising force is a unique and constant property of the sealed tube. *Pascal* conducted two illustrative experiments. The first, together with his brother-in-law *Florin Périer*. They measured the air pressure with barometers simultaneously at two different altitudes⁶ and proved the mercury height to be altitude dependent. *Pascal* proved the analogy of compressed wool to be correct with a second experiment. He carried a half inflated balloon up a mountain and back into the valley. While climbing uphill, the air in the balloon expanded but deflated to its initial size on the way back. Although *Pascal* demonstrated the altitude's dependence of air pressure and density, he did not derive an exact formula for this relation. It was *Robert Boyle* who took the next step towards the barometric formula.

Otto v. Guericke

In 1654, *Otto von Guericke* (1602-1686) mayor of Magdeburg demonstrated the power of air pressure and the feasibility of creating a vacuum with a suction pump [Sch88]. He studied the art of fortification, hydrology, and astronomy. The new copernican theories about the movement of the planets made him wonder, whether planets might follow their trajectories frictionless in a vacuum. Starting with a modified bellows pump, he emptied water filled barrels finding that pumping became increasingly harder the more water was sucked out. To his and his helpers surprise the remaining water started to boil and to fizz. The leaky wine barrels were changed to vessels made out of copper sheets which collapsed and crumbled impressively during successive experiments. *Guericke* spent some time improving the necessary pumps and valves and came up with an apparatus that got very trendy at meetings of the higher society: a bell jar that fitted on top of a vacuum pump [Fra84]. The astonished society could watch old wrinkled apples to look like as picked from the tree just minutes ago but to convert back to the crumbled one when air again flooded into the vacuum chamber. Beer started to foam enormously at lower pressures but the foam disappeared immediately when vacuum was released. The sound of a ringing bell could also be silenced in a vacuum chamber. Unfortunately, also a number of small animals needed to die under the curious watching eyes at this time.⁷ *Otto von Guericke* became famous with the so called 'Magdeburger experiments'. He measured the air pressure with a barometer and calculated the force that air exerts on a sphere with vacuum inside. He tested his calculation in 1654 in Magdeburg [Sch88]

⁶ *Pascal's* brother-in-law measured the pressure on top of peak Puy de Dôme while he took the reading 1000 m below in Chermont-Ferrand. The difference in mercury height was 85 mm. [BS97].

⁷ *Johann v. Muschenbroek* summarized this finding, "all animals die in a space with no air". *Boyle* expanded this later by making water sparkle under vacuum and deducing, "water is mingled with air and its inhabitants could not live without of the same" [Fra84].

with eight harnessed horses on each side of an evacuated split copper sphere⁸ in order to separate it (see Fig. 1.2). *Guericke's* experiments were impressive but his most

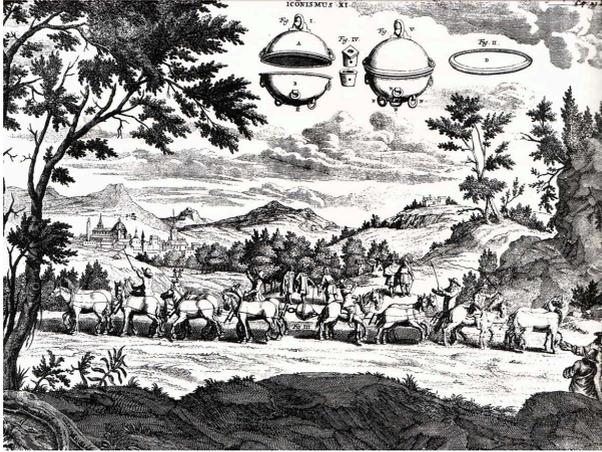


Fig. 1.2: In 1654 *Otto von Guericke* and *Gaspar Schott* demonstrated the power of air pressure with 16 harnessed horses trying to separate an evacuated copper sphere (picture taken from [Gue72]).

progressive insight was that no fitting or levers were necessary to transport forces implying a corpuscular structure of the matter.⁹

Robert Boyle (1627-1691) gained further insight when he experimented with entrapped air in tubes. He found that compressed air could carry higher mercury columns than the column of the barometer and concluded that air pressure is not necessarily related to the weight of air. One of *Boyle's* students recognized that the air pressure p was inversely proportional to its volume V and a first version of the perfect gas law was found in 1662 called *Boyle's law* [Sch88]: $pV = \text{constant}$.¹⁰

The first who found a quantitative relation of pressure and altitude was *Edmund Halley* (1656-1742) in 1686 (43 years after *Torricelli's* experiment). He provided two equations for an isothermal atmosphere [BS97]:

$$z_{\text{Hg}}(h) = z_{\text{Hg}0} \exp \left[- \frac{\rho_{\text{air}} h}{\rho_{\text{Hg}} z_{\text{Hg}0}} \right],$$

$$h(z_{\text{Hg}}) = \ln \left[\frac{z_{\text{Hg}0}}{z_{\text{Hg}}} \right] \frac{\rho_{\text{Hg}}}{\rho_{\text{air}}} z_{\text{Hg}0},$$

⁸ *Otto von Guericke* repeated his experiment with a larger sphere and 12 harnessed horses per side in 1663 in Berlin. The diameter of the sphere was one Magdeburg's cubit (equiv. to 57.6 cm) and the force necessary to separate it was about 26 kN (equiv. to 2.6 metric tons).

⁹ Electronic scans of *Guericke's* original work can be found at [Pöl07].

¹⁰ Electronic scans of *Boyle's* original work can be found at [ECH07] and [The07].

Robert Boyle

Boyle's Law

Edmund Halley

Jacques Charles
Joseph Gay-Lussac
Amedeo Avogadro
Ludwig Boltzmann
James Maxwell

with ρ_{air} , ρ_{Hg} the specific densities of air and mercury (at altitude $h = 0$ m) and z_{Hg} being the mercury column height (zero level height: $z_{\text{Hg}0} \equiv z_{\text{Hg}}(h = 0 \text{ m})$).

Many more contributors: *Jacques Charles* (1745-1823), *Joseph Gay-Lussac* (1778-1850), *Lorenzo Romano Amedeo Carlo Avogadro* (1776-1856), *Ludwig Boltzmann* (1844-1906), *James Clerk Maxwell* (1831-1879), were necessary to derive the perfect gas law in its present form

$$pV = kNT \quad \text{or} \quad pV = nR^*T \quad (1.1)$$

with the *Boltzmann* constant k , the number of molecules N and p , T , V denoting pressure, temperature and volume, respectively (or for its equivalent form n , R^* denoting the amount of gas and the universal molar gas constant). *Boltzmann* and *Maxwell* were the first to relate the macroscopic, thermodynamic quantities to the microscopic, molecular scale. They found the relation between the kinetic energy of gas molecules (i.e. the average of their squared velocity $\overline{u^2}$ and molecular mass m_u) and pressure: $pV = \frac{2}{3} E_{\text{kin}} = \frac{1}{3} m_u \overline{u^2}$.

Pierre-Simon
de Laplace

The French mathematician *Pierre-Simon de Laplace* (1749-1827) finally put all pieces together and derived the barometric formula for isothermal gases in its present form [BS97]

$$p(h) = p_0 \exp \left[- \frac{m_u g h}{k T} \right]. \quad (1.2)$$

The formula calculates the air pressure p as function of altitude h and temperature T with the zero pressure p_0 at altitude $h = 0$ m, *Boltzmann* constant k , acceleration of gravity g and the molecular mass of air m_u (for a derivation of the barometric formula and an extension for an atmosphere with a linear temperature gradient see Appendix A.2).

The pressure distribution in gases and liquids has been discussed. Before focusing on pressure measurement in Section 1.4, the preceding paragraphs will illustrate this physical quantity to get a better perception of the measurement task that needs to be mastered.

1.2 Making acquaintance with physical quantity pressure

As presented in the previous section, scientists had a hard time to develop today's perception of vacuum and pressure. It still remains not handy because in our daily life we are dealing with distance, force, temperature and speed. These are quantities for which we have developed an intuitive understanding. But for pressure, which is only perceived as popping ears in the airplane or during a scuba dive, or as an increased respiration rate during hiking in the mountains, there is hardly anything illustrative. Therefore, this section tries to give some conversion factors to develop an intuitive notion of the physical quantity pressure and the required performance of a pressure sensor.

The previous section focused purposely on the historic understanding of the pressure distribution in ambient air and water. These are the media in which we linger and many applications exist which rely on pressure measurement in air or water.

The presented sensor is designed and suitable for consumer application in which pressure sensors can be found e.g. as diving depth gages or as altimeters for hikers, climbers, and mountain-bikers. Other illustrative applications are weather stations in which the ambient air pressure needs to be measured, or washing machines in which the level of water must to be monitored. The demanded sensor performance depends on the type of application. In water, divers require a depth resolution of about 1 m but technical water columns need to be measured down to 1 mm height. In air, for outdoor sportsmen, a height resolution of 10 m is appropriate but a resolution better than 50 cm is necessary for indoor navigation systems of the future. Today's high performance pressure sensor systems offer an even higher resolution, they can detect height changes of only 10 cm.

In water *Pascal's law* can be used to calculate the pressure caused by the liquid column. It is in linear proportionality to the column height h , the liquid density ρ and the acceleration of gravity g :

$$p = \rho h g. \quad (1.3)$$

The resulting pressure p depends only on temperature through changes of the water's density ρ . The situation is more complex in air because temperature related density changes can not be neglected as e.g. the negative temperature gradient of the atmosphere. From rocket and satellite data a hypothetical and internationally agreed vertical distribution of atmospheric properties called the *Standard Atmosphere* was worked out in 1976. The resulting equation (A.4) has to be used to calculate the pressure variation for an altitude change Δh at sea level¹¹

$$p(h) = 101325 \text{ Pa} \left[1 - \frac{h}{44.331 \times 10^3 \text{ m}} \right]^{5.263}.$$

Pressure changes can be converted to equivalent water and air column heights by application of the latter formula and *Pascal's law* (1.3):¹²

pressure in terms of
water or air column

$$\begin{array}{llll} \Delta h_{\text{water}} = 1 \text{ m} & \cong & \Delta p = 98 \text{ mbar} & \cong & \Delta h_{\text{air}} = 817 \text{ m} \\ \Delta h_{\text{water}} = 1 \text{ mm} & \cong & \Delta p = 9.82 \text{ Pa} & \cong & \Delta h_{\text{air}} = 81.7 \text{ cm} \\ \Delta h_{\text{air}} = 1 \text{ m} & \cong & \Delta p = 12 \text{ Pa} & \cong & \Delta h_{\text{water}} = 1.22 \text{ mm} \\ \Delta h_{\text{air}} = 0.1 \text{ m} & \cong & \Delta p = 1.2 \text{ Pa} & \cong & \Delta h_{\text{water}} = 0.12 \text{ mm} \end{array}$$

Still the pressure variation of $\Delta p = 1.2 \text{ Pa}$, the detection limit of high performance altimeters remains abstract. It can be related to an equivalent temperature or density change with the perfect gas law and the constants of the *Standard Atmosphere*:

$$p = \rho RT \rightarrow \frac{\Delta p}{\rho R} = \Delta T, \quad \frac{\Delta p}{RT} = \Delta \rho.$$

¹¹ The model is developed in Appendix A.2 and Appendix A.2.1. All necessary input data is summarized in the coefficients given in Tab. A.2 of Appendix A.2.2.

¹² There are two of the common pressure units used in this comparison. For the conversion of the pressure units Pa, bar, at, torr, and psi refer to Tab. A.3.

Considering this formula and a cube of confined air, it is found that the same pressure variation is measured if the temperature is increased by only a fraction of a Kelvin

$$\begin{aligned}\Delta h_{\text{air}} &= 0.1 \text{ m} && \cong && \Delta T = 3.5 \times 10^{-3} \text{ K} \\ \Delta h_{\text{water}} &= 1 \text{ mm} && \cong && \Delta T = 27.9 \times 10^{-3} \text{ K}.\end{aligned}$$

The same cube of air with 10 cm edge length at 15 °C has a mass of $m = 1.225 \times 10^{-3}$ kg and the density change of the confined air after displacement of one side of the cube can be calculated to be

$$\Delta \rho_{\text{air}} = \frac{m}{V_2} - \frac{m}{V_1} = m \frac{V_1 - V_2}{V_1 V_2} = \frac{m}{V_1} \left(\frac{h_1}{h_2} - 1 \right),$$

where V_1 and h_1 , denote the initial cube volume and height being deformed to V_2 and h_2 . It follows for $\Delta h = (h_1 - h_2)$ that

$$\begin{aligned}\Delta h_{\text{air}} &= 0.1 \text{ m} && \cong && \Delta h = 1.2 \mu\text{m} \\ \Delta h_{\text{water}} &= 1 \text{ mm} && \cong && \Delta h = 9.5 \mu\text{m}.\end{aligned}$$

Therefore, the detection limit of 10 cm altitude change in air can be illustrated by displacing one side of a 10 cm cube by only $\approx 1 \mu\text{m}$ which is about 1/100th of the diameter of a human hair. This minute pressure variation needs to be detected at a high offset value of 1013.25 mbar according to the *Standard Atmosphere*

$$1013.25 \text{ mbar} \approx 1 \times 10^5 \text{ Pa} = 1 \times 10^4 \text{ kg/m}^2.$$

That is, the ambient air exerts a pressure equivalent to the force of 10 metric tonnes on every square meter of a surface in contact with it at standard conditions. The skin area of the human body can be estimated by using *Mosteller's* formula

$$A^{(\text{skin})} = \sqrt{\frac{\text{height} \times \text{weight}}{36 \text{ kg/m}}}.$$

This results for the author's geometry (height = 1.7 m and weight = 70 kg) in a surface area of about $A^{(\text{skin})} = 1.8 \text{ m}^2$ and a weight of 18 metric tonnes distributed over the body's surface.

This is an enormous weight, but on the other hand, the area of a single pressure sensitive plate of the presented sensor is only about $8 \times 10^{-9} \text{ m}^2$. The equivalent weight of air column on such a transducer is 80 mg. It must be sensitive to weight changes of $1 \mu\text{g}$ to sense altitude differences of 10 cm. This is unfortunately again not illustrative but impressive – and is outperformed by nature. The effective area of the human eardrum, a sensor for relative dynamic pressure, is about 55 mm^2 and the hearing threshold level is defined to be $20 \mu\text{Pa}$ at 1 kHz. If we calculate again the equivalent weight we find it to be roughly $0.1 \mu\text{g}$.

Hopefully, the challenges have been illustrated. Still the task itself is not defined

clearly and will be discussed in the proceeding section.

1.3 Who needs all these pressure sensors?

This section focuses briefly on the commercial impact of MEMS pressure sensors and identifies the major application fields and users. The given data is taken from the NEXUS market analysis I [Wec98] to III [Wic06] which provide an overview of the MEMS market development.¹³ The question, "Who needs all these pressure sensors?", may arise if the vast number of tens of millions (approaching hundreds of millions) MEMS pressure sensors is considered which are sold year after year. It is important to go after the answer to understand the future demands, needs, and wishes of the users necessary to define the development objectives of this field of MEMS.

Market analysts agree and predict a high overall growth rate of 15 % of the MEMS market for the next years (average annually growth of pressure sensor market: 9 %) [Wic06] [Elo07]. There is a large number of 178 million MEMS pressure sensors sold per year (data from 2004). With this unit count, pressure sensors rank first, in terms of market volume, under all sold MEMS sensors followed far behind by gyroscopes, accelerometers, flow- and infrared sensors. A summary of data given by [Wic06] with respect to pressure sensors is presented in Tab. 1.1. Obviously, the automotive sector and industrial process control dominates the market in terms of turnover. Although new high volume applications are entering the automotive market like tire pressure monitoring systems (TMPS), side airbag ignition units, and passenger occupation detection devices, its growth is predicted to remain moderate due to continuous pressure on prices. The winners and drivers of market growth will be the consumer market with electronics and household appliances. The analysts predict that pressure sensors will be found as altimeters in outdoor sports gear or in cell phones. It is expected that pressure sensors will be incorporated in 10 % of the cell phones by the year 2009. Besides altitude measurement and weather forecast capability, these phones can be used for indoor navigation or could send the floor level of a casualty (lateral position is already available as service) in case of an accident. Moreover, it is expected to find medical functionality, e.g. breathing rate and blood pressure sensors, integrated into consumer and sports equipment. Meteorological stations or scuba gear rely on small and cost-effective sensors. Similarly, liquid level detectors and water pressure sensors in household goods do. Additionally, flow meters based on differential pressure measurement are competing with thermal measurement principles. The trend in Europe to save energy, water, and to reduce noise, leads to an increasing number of incorporated sensors in consumer goods to achieve competitive advantages. Finally, all kinds of climate control systems (HVAC: humidity, ventilation, air-conditioning) fixed or mobile, will gain importance and market volume. In these applications pressure sensors are necessary for fan control, air volume measurement and filter pressure-drop monitoring.

Forecasts assume an increase in standard products, but the largest impact on the

market analysis data

¹³ The Nexus market analysis is based on the underlying data collected in more than 200 interviews with international experts.

Table 1.1: MEMS pressure sensor market figures of year 2004 and forecast for 2009. (Numbers in million USD for components available as first level packaged devices according to [Wic06])

market segment	turnover [M \$]		growth		market share	
	2004	2009	Δ [M \$]	Δ %	2004	2009
automotive industry	408	678	274	67 %	38 %	40 %
medical, live sciences	142	198	56	39 %	13 %	12 %
consumer electronics	12	96	84	700 %	1 %	6 %
industrial process control	469	595	126	27 %	43 %	35 %
defence, homeland security	14	29	15	107 %	1 %	2 %
household appliances	40	101	61	153 %	4 %	6 %
total	1085	1697	612	56 %	100 %	100 %

new applications

MEMS market will have new applications. The growing number of small sensor modules enables user-centric devices, e.g. set top boxes with built-in intelligence to sense the user's motions and emotions. Cell phones are a good example of user-centric devices with added capabilities. They have already assimilated PDA (PDA: personal digital assistant) functionality and are on the way to become an integrated gaming and media-platform. New human-machine input interfaces are under development, i.e. game control by acceleration sensors is entering the market but also pressure sensors may be used as input or emotional feedback sensors. In the context of new applications also wearable devices are recently extensively under research. They aim at productivity and efficiency improvement but also address the consumer market with integrated entertainment features.¹⁴

consumer market

Following the analyst's predictions, the consumer market is of special interest for this work. It is driven by system size and price. New applications are triggered by cost-effectively integrated sensor modules. The typical integrated consumer sub-component must have a standard package with a maximum size of $5 \times 5 \times 1.2 \text{ mm}^3$ with a sensor die smaller than $2 \times 2 \text{ mm}^2$ (i.e. 3.5k to 5.7k dice/6-inch wafer) and must be priced between USD1.5 and USD2.0, as sketched by [Elo07]. Consumer market product costs typically drop by 10 % to 15 % per year with effect on the incorporated MEMS components. Different strategies are followed to meet the cost requirements of the target market: monolithic CMOS integration, multiple functionality of the sensor component in the consumer product, loose specifications of the MEMS part, and the reduction of packaging costs by system design. It is agreed that packaging is a major challenge and in strong relation to the system costs [Mah06]. Consequently in situ or self-packaging methods, i.e. wafer level encapsulation offers advantages in the way that MEMS devices can be treated much more like standard ICs throughout the packaging procedure.

Small-sized sensor modules for consumer applications are required as conclusion

¹⁴ One example of pressure sensors in wearable sports gear can be found in [ATM07] and [Chi05]. It is a martial arts body protector for competitions which detects hits from the opponents and measures their impact force.

from the brief summary of the market analysis. Challenges are related to the downward price pressure. Furthermore, the focus on integrated and ready-to-use systems indicate the way for further research which may concentrate either on new packaging concepts or on new sensor implementations which simplify the system integration. This work follows the latter approach with the objectives and method of resolution as summarized in Section 1.5.

1.4 Micromachined pressure sensors

It is beyond the scope of this thesis to narrate and recall the history of micromachined pressure sensors but improvement of the state-of-the-art requires at least some knowledge about the past. This holds true especially in the case of micromachined pressure sensors. The MEMS development was triggered by the discovery of silicon's piezoresistivity in conjunction with solid state electronics development and a strong impact of market demand for cost-effective pressure sensors.

This thesis is concerned with the development of a micromachined pressure sensor. Any new kind of pressure sensor must compete with a well established piezoresistive pressure sensor technology which is ubiquitous in our daily live. Moreover, the piezoresistive pressure sensor can be called the progenitor to MEMS [Mal04]. Although it was not the first silicon sensor,¹⁵ it was at least the first mechanical silicon sensor. Therefore, extensive research has been conducted on improving, modeling, and integrating piezoresistive pressure sensors. Many groups developed capacitive pressure transducers but have failed to bring them to applications – but some succeeded. The intention of this section is to briefly review the historical background of MEMS and to figure out the reasons for the individual success of resistive or capacitive pressure sensors in cases of achieved commercialization. The historical data of this section is condensed in Tab. 1.2.¹⁶

1.4.1 A brief historical review

The development of solid state electronics and MEMS coincides. The first bipolar transistor was developed at Bell Laboratories by a group around *W. Shockley* in 1947. Research on piezoresistivity started as study about parasitic transduction but turned out to be the beginning of MEMS.¹⁷ *C. S. Smith* published in 1950 his work about piezoresistivity of silicon and germanium [Smi54]. Soon a number of researches realized the potential of piezoresistivity for strain gauges. The development of mechanical transducers made out of silicon was started.

the very beginning

Already nine years later in 1959, *Richard Feynman* had the imagination to suggest the development of micro-machines and micro-computers. During a talk, he

Richard Feynman

¹⁵ According to [Mid95] a light detector was first integrated in silicon in 1960 during the time when silicon planar technology was developed.

¹⁶ Table 1.2 represents the time line according to the data given in [Mid00] [Mid87] [Fey92] [Mid81] [Fuj97] [Bry96] [Tim05] [Bry06] [Pet82] [Pet95] [Mid95] [Ger05] [Pue93]. Although not consistent in some given dates (authors sometimes disagree who had been first to do something) it represents an illustrative overview.

¹⁷ *Bill Pfann* commented: "Now that we've studied the transduction effects in semiconductors for the purpose of getting rid of them, maybe they are useful." [Dau07]

proposed powerful computers which make decisions and do pattern recognition, rewritable mass storage devices for computers, a solid state LASER, micro motors, swallowable micro-machines for surgery, as well as evaporation and lithography as micro fabrication means [Fey92]. Also linked to the beginning of MEMS is *Kurt Petersen*. He reviewed the efforts of a number of researchers, from the very beginning until 1982, to use silicon as a mechanical material [Pet82]. At the time of publication many of the important bulk micromachining processes were already available. The primary goal of *Petersen* was to make the potential of MEMS apparent to a wide scientific community. He succeeded and triggered the foundation of many MEMS companies and research projects.

Kurt Petersen

MEMS technology has been developed rapidly because there were strong rational reasons for the approach [Bry96] [Bry06] [Fuj97]:

Why MEMS?

1. miniaturization (size is price)
2. multiplicity (batch fabrication)
3. mechanical properties (single crystalline silicon)
4. microelectronics (available infrastructure, possible systems integration).

The latter reason is accounted for many times but is not proven by market data. Only a small fraction of successfully commercialized microsystems are integrated monolithically.¹⁸

MEMS fabrication technology was to a great extent assimilated from integrated electronics but many MEMS specific technologies still needed to be developed costing a lot of money and time: wafer deep etching, double side wafer alignment, wafer bonding, sacrificial layer etching, hermetic sealing of cavities. Moreover, thickness control of IC fabrication was underdeveloped and the mechanical properties of the utilized materials were not precisely known. In addition, high-volume mechanical testing and packaging concepts, allowing the often required media interaction of sensors, were not developed by the electronics industry.

historic hurdles

Beside these obstacles there have been very favorable circumstances which strongly promoted MEMS development: the economical pull from MAP (MAP: manifold absolute pressure) sensors and disposable blood pressure sensors. Both are high volume applications which justified the necessary extensive research. In 1966 the US government announced the clean air bill to reduce fuel consumption. During the following years and the oil crisis of the 70th, the automotive industry focused their efforts to improve the gasoline combustion by means of MAP sensors to control the fuel to air ratio in the cylinder. Also blood pressure monitoring had the potential market to cause extensive research for replacing the expensive reusable pressure gauges which were common at this time.¹⁹

MEMS promoters

The invention of the bipolar transistor and piezoresistivity started the vast solid state electronics and MEMS development of the last 60 years.²⁰ A number of people quickly realized the potential of the piezoresistivity for strain measurement and

bulk micromachining

¹⁸ Only 8 % of the commercially available microsystems are actually integrated monolithically [Bry96].

¹⁹ Today, one to three disposable blood pressure sensors are required for every patient under anesthetization because of AIDS.

²⁰ It is difficult to follow the fast fluctuation of people and companies associated with the pressure sensor business and research during the first years especially during the time after 1980 in North America. This is partly

worked on the replacement of the 10 years earlier developed metal strain sensors. In 1961, the first piezoresistive pressure sensors implemented pieces of doped silicon which were glued to a metal plate. Later in 1962, a silicon plate with implanted resistors was used as transducer element for the first time but still was not structured three-dimensionally.²¹ In a next step, the silicon bulk material was first mechanically crafted or eroded to get rid of the adhesive which was used as attachment of the silicon transducer plate leading to unsatisfactory results. The performance of the sensors was significantly improved by the development of anisotropic wet chemical etching techniques for silicon (first reported in 1967) in combination with an electrochemically (1969) or dopant profile (1971) controlled etch stop. Also of great importance was the invention of field assisted (anodic) bonding of glass and silicon in 1968, which enabled the sealing of bulk micromachined cavities and the reinforcement of the sensor to improve its packaging. It can be observed that all common bulk micromachining technologies were developed during the first 10 years of MEMS development between 1961 to 1971. It took approximately 20 years more to add the remaining three important bulk machining means: epitaxial deposited transducer plates (1979), silicon fusion bonding (1988), and deep reactive ion etching (1993).

The first pressure sensor developments focused on piezoresistivity for its easier implementation and consequently on the application of bulk silicon as transducer material because of the high achievable gauge factors. Hence, surface micromachining is stronger related to capacitive transducers. This explains why surface micromachining techniques evolved later although considered best suited for miniaturization, batch processing, and monolithic integration. Sacrificial layer etching was conducted already in 1965 but was not employed for pressure sensor fabrication during the next 20 years. One problem that resistive pressure sensors had to deal with was their temperature dependency. A possible solution to expand the allowable temperature range was to replace the pn junctions in reverse bias of implanted resistors by a dielectric insulation. To do this, poly-silicon resistors were encapsulated in a deposited nitride membrane with a poly-silicon sacrificial layer underneath. First processes of this kind could not be called pure surface micromachining. The sacrificial layer was only used to allow the wet etchant to spread under the membrane and to finally form a self-aligned cavity anisotropically into the bulk silicon (front side bulk micromachining, 1987). Front side bulk micromachining lead already to considerably smaller devices but on the down side there are to name the worse and process dependent mechanical properties of the transducer layers, more complex geometries, and mechanical stress of the deposited layers. As monolithic integration has not been the technology driver in first place and overall dimensions were defined by the package, surface micromachining developed later when pressure on prices began to rise. Today, the most common surface micromachining technology employs poly-silicon as transducer material and silicon dioxide as sacrificial layer. The process was first presented in 1986 by Howe and Muller who fabricated a reso-

surface
micromachining

due to the entrepreneurship prevailing in the USA. Personal summaries of the beginning of MEMS industry are given in [Dat07], [Kel07] and [Mal04]. The latter is again compressed in [Ger05] with added information about technology and the development in eastern Germany at this time.

²¹ The plate was glued on top of a glass tube to measure differential pressure and was prone to packaging stress. It was commercially used as an altimeter in the first Douglas DC-10s [Mid00].

Table 1.2: Historic time line of relevant contributions related to micromachining and the miniaturization of pressure sensors.

year	invention/development/event	reference
1947	bipolar transistor by <i>J. Bardeen, W. H. Brattain and W. Shockley</i>	[Sho50] [Bar49]
1948	field-effect transistor by <i>W. Shockley and G. L. Pearson</i>	[Sho48] [Sho52]
1951	shadow mask for photofabrication	[Fuj97]
1954	piezoresistivity of silicon by <i>C. S. Smith</i>	[Smi54]
1959	MEMS/NEMS proposed by <i>R. P. Feynman</i>	[Fey92]
1957	first commercial planar transistor (<i>Fairchild Semiconductors</i>)	[Ger05]
1959	first integrated silicon circuit by <i>R. Noyce (Fairchild Semiconductors)</i>	[Ger05]
1960	light detector as first silicon sensor	[Mid95]
1961	silicon resistors glued on top of a transducer plate <i>A. D. Kurtz (Kulite)</i>	[Ger05]
1962	first silicon diaphragm pressure sensor with implanted resistors by <i>Tufte (Honeywell)</i>	[Tuf62]
1965	sacrificial layer etching (resonant surface transistor)	[Nat65]
1967	crystalline oriented anisotropic etching	[Fin67]
1968	first piezoresistive pressure sensors in bulk micromachined silicon by <i>Gieles (Philips Research)</i>	[Cie69]
	field assisted thermal bonding by <i>D. I. Pomerantz</i>	[Pom68]
1969	commercial sensor with isotropically structured plate and anodic wafer bonding (<i>Kulite</i>)	[Ger05]
	electrochemical etch stop	[Gre69]
1971	dopant dependent etch stop	[Boh71]
	first integrated piezoresistive pressure sensor by <i>E. M. Blaser and W. H. Ko</i>	[Ger05]
1973	first capacitive pressure sensor (<i>Robert Bosch</i>)	[Fro73]
1979	pressure sensor with epi-silicon plate	[Pet82]
1980	first integrated capacitive pressure sensor by <i>C. Sander et al</i>	[San80]
1982	silicon as mechanical material, review article by <i>K. E. Petersen</i>	[Pet82]
	first low-cost disposable blood pressure sensor commercialized (<i>NovaSensor</i>)	[Bry96]
1983	commercial integrated pressure sensors presented by <i>Toyota</i>	[Mid87]
1984	first million (cumulated) MEMS pressure sensors sold	[Bry06]
	first pressure sensor fabricated on a SOI (SIMOX) substrate (<i>Kulite</i>)	[Kur84]
	first surface micromachined resistive pressure sensor (poly-silicon plate on an oxide sacrificial layer)	[Guc84] [Guc88]
1986	surface micromachining of poly-silicon with silicon oxide as sacrificial layer by <i>Howe and Muller</i>	[How86]
1987	poly-silicon as sacrificial layer (combined surface bulk micromachining)	[Tim05]
	first integrated CMOS piezoresistive pressure sensor by <i>Ishihara</i>	[Ish87]
1988	silicon fusion bonding for pressure sensor fabrication (<i>Lucas NovaSensor</i>)	[Ger05]
	dissolved wafer process	[Spa88] [Hay00]
1991	front side micromachining (self-aligned anisotropically etched grooves)	[Sug91] [Shi92]
	first commercial surface micromachined poly-silicon sensor (integrated accelerometer, <i>Analog Devices</i>)	[Mad02]
1993	deep reactive ion etching	[Mur93]
1996	touch-mode operated capacitive pressure sensor	[Ko96a] [Ko97]
1988	(presumably) first commercial integrated capacitive pressure sensor (<i>Siemens</i>)	[Sch98] [Tim05]

nant bridge.²² This popular combination of materials is due to the good wet chemical selectivity of the sacrificial etch in this case and the conductivity of poly-silicon. Five years later in 1991 (see Tab. 1.2), the first entirely surface micromachined resistive pressure sensor was presented with a poly-silicon sacrificial layer and resistors embedded in a nitride membrane.

The first capacitive pressure sensor was reported in 1973 approximately 10 years after its resistive counterpart. During the 80th extensive research was started on micro transducers and many research groups world wide were developing MEMS. For this reason it is difficult to figure out the firsts but a comprehensive retrospective summary was given by [Pue93] in 1993. At the time when research was started it was agreed that capacitive pressure sensors would have the potential of low temperature coefficients, low power consumption, high stability, and high sensitivity. But 10 years later still no commercial device was on the market. Parasitic capacitances and noise pick-up could be identified as reasons from the electrical point of view. These difficulties are due to parasitics originating from the packaging and the lead transfer area of the sensor device. Parasitic capacitances gain more importance as the system scales down and the sensor signal capacitance decreases with the available surface area. The second kind of challenges were related to the fabrication technology for capacitive pressure sensors. On first sight, the technological approaches for capacitive absolute pressure sensors are very simple but also pose two issues: precise gap formation and the necessity of a hermetic lead transfer in case of bulk micromachined sensors which employ anodic bonding [Pue90]. The concept of monolithic integration prevailed to overcome the electrical problems but the necessary IC technologies were less compatible to the common bulk micromachining processes and the resulting sensing systems were complex (see [Pue93] for a survey). The first surface micromachined capacitive pressure sensors appeared in the end of the 80th. Presumably the first one with a poly-silicon diaphragm was presented by a group around *Winfried Mokwa* in 1990 (cited in [Pue93]), but it took again eight years more for the first commercial sensors to emerge (*Siemens* started its volume production in 1988, see [Sch98]).²³

A monolithic integration of pressure sensor and readout has been taken for granted but does not prevail until today. Expected advantages are a smaller system size, lower fabrication costs, and a simplified system packaging procedure. However, considerable drawbacks exist: longer and more complex processes decreasing the system yield, technological constraints for electronics and transducer, and the innovation cycles of the solid state electronics industry requiring a rapid adaption of the transducer process. The development requires higher costs for a less flexible systems. It becomes obvious that monolithic integration is only viable for very high volume applications. Therefore, it was *Toyota* to fabricate the first commercial resistive pressure sensor with integrated bipolar electronics (1983) for the automotive industry although the first scientific resistive prototype was presented already in 1971

capacitive
pressure sensors

integrated
pressure sensors

²² *Howe* and *Muller* [How86] are very frequently cited for their first surface micromachining process of poly-silicon on silicon oxide. However, two years earlier *Guckel* and *Burns* [Guc84] fabricated surface micromachined pressure sensors in a similar way.

²³ Similarly to the historical development of piezoresistive pressure sensors it took approximately 20 year for the technology to be commercialized.

(see Tab. 1.2). Capacitive transducers are susceptible to noise and parasitic capacitances and a monolithic integration of the readout was regarded the only possible option to cope with these difficulties. The first scientific prototype of a monolithically integrated capacitive pressure sensor system was presented in 1980 but today only very few commercial systems exist as supplied e.g. by *Infineon* (start of production in 1988) [Inf07b]. Improved sensor concepts, system packaging, and readout renders an MCM (MCM: multi chip module) design of capacitive pressure sensors feasible as e.g. demonstrated by *VTI Technologies* [VTI07b].

commercialization

Although strongly promoted, it took more than 20 years until the first cumulated million pressure sensors were sold in 1984, and it seems that this period is characteristic for the commercialization of a new technology (for further examples see [Bry06]). The semiconductor age was started in the USA and most historical reviews focus on the sensor development during the early years in North America but also groups in Europe and Asia were active in this new field of research. It comes that some achievements are associated with US groups and companies in a number of publication but earlier articles with their origin in Europe prove them wrong. Especially, a disagreement of reviews can be noted in case of the first integrated piezoresistive and capacitive pressure sensors. In 1968, employees of *Philips Research* in the Netherlands presented the first three-dimensionally bulk micromachined piezoresistive pressure sensor with implanted resistors and the first capacitive pressure sensor can be traced back to *Robert Bosch* published in Germany in 1973. Important companies during the early years in the USA were *General Electrics*, *National Semiconductors*, *Honeywell*, *GM Delco*, *NovaSensor* and *Kulite Semiconductor Products*.²⁴ *Toyota* was very active in Asia. Amongst the first in Europe besides *Philips* and *Bosch* was *Keller Druckmesstechnik*.²⁵ *Honeywell* marketed the first monolithic piezoresistive transducer (1966) and *Kulite* contributed significantly by introducing several technologies into the market: piezoresistive strain gauges (1961), anodic bonding and wet chemical cavity formation (1969), and the first SOI pressure transducer fabricated on a SIMOX substrate (SIMOX: separation by implanted Oxygen) in 1984. *National Semiconductors* started marketing the first high-volume silicon pressure sensors in 1974 and *GE Delco* was the first company which mass fabricated a pressure sensor for the automotive industry. *Lucas NovaSensor* introduced the first mass fabricated disposable MEMS blood pressure sensor (1982) and developed a silicon fusion bonded pressure sensor (1988).

1.4.2 Examples of present absolute pressure sensors

Pressure and temperature are the two most important measurands today. Consequently a lot of different conceptual and technological approaches have been implemented during the last 60 years. It is beyond the scope of this thesis to summarize the existing scientific work in the field of commercial MEMS pressure sensors and

²⁴ More US companies contributed which have merged or are less commonly known: *Micro Systems*, *IC Transducers* (later *Foxborow ICT*), *Endevco*, and *SenSym* (a comprehensive overview is given in [Ger05]).

²⁵ *Keller Druckmesstechnik* was founded by *Hannes W. Keller* who conducted research on piezoresistive pressure sensor for *Honeywell* during the very beginning.

this section focuses on a general categorization of available absolute pressure sensors.

Three major objectives have to be achieved by a sensor element:

sensor objectives

1. high sensitivity to the desired measurand (without being sensitive to anything else)
2. reliability/stability
3. cost-effectiveness.

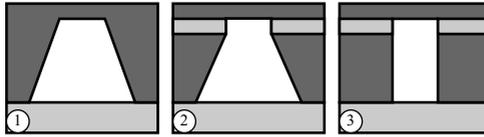
Many micromachined sensors are on the market because they outperformed their macroscopic opposer in all three performance categories. The first years of micro-machined sensor development focused on the first two aims with the result of many high performance sensing elements. Providing the existence of a sensor element, its cost scales with physical dimensions. Therefore, efforts were spent to further miniaturize existing detection principles. This thesis focuses on the miniaturization of a capacitive absolute pressure sensor and the following presentation of existing pressure sensors selects *miniaturized* examples out of a large number of realized elements. Only highly miniaturized, commercially available, absolute pressure sensors are presented and the choice is further confined to the dominating measurement principles: piezoresistive and capacitive detection. One possible breakdown of existing MEMS pressure sensors considers the transducer material and the necessary fabrication technology. Four different categories can be identified which are summarized in Tab. 1.3 and Fig. 1.3. This section gives examples for each of these sensor categories.

Table 1.3: Overview of micromachining approaches for the fabrication of pressure sensors.

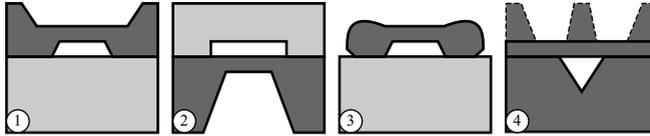
category	geometry definition	transducer material	typ. element size	miniaturization measures
A	1 × bulk etch	single-crystal	large	wafer thinning, Epi-Si, DRIE, electrochemical etch stop
B	2 × bulk etch	single-crystal	medium	Epi-Si, wafer thinning, wafer dissolval
C	surface etch	single-crystal	small	porosification, epitaxy, wet sacrificial layer etch, precise lithography & deposition
D	surface etch	poly-crystalline	small	wet sacrificial layer etch, precise lithography & deposition

Sensor category A: single-crystal plate, 1 × bulk micromachining

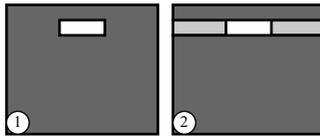
The sensor concepts depicted in Fig. 1.3(a) are of low relevance for capacitive pressure transducers but they are presented because they illustrate the most common designs of piezoresistive pressure sensors. The transducer plate is defined by an anisotropic wet etch step from the wafer backside. Geometric deviations of the plate are due to lithographic misalignment, wafer thickness variations, and timing of the



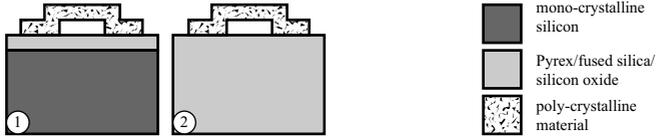
(a) Sensor category A (single-crystal plate, $1 \times$ bulk micromachining): 1) plate and cavity is formed by an anisotropic back side wet etching step. The etching can be either time, dopant or electrochemically controlled. 2) similar to 1 but the etch stop is defined by a stop layer 3) plate and cavity is formed by an anisotropic dry etch step from the back side.



(b) Sensor category B (single-crystal plate, $2 \times$ bulk micromachining): 1) cavity and plate are formed by two bulk micromachining steps of a silicon substrate. 2) similar to 1 but both substrates are bulk micromachined. 3) similar to 1 but unused transducer substrate material is wet chemically removed (dissolved wafer process). 4) front or back side anisotropic etching is combined with silicon fusion bonding.



(c) Sensor category C (single-crystal plate, surface micromachining): 1) cavity is defined by a porous silicon layer which is removed prior to the epitaxial growth of the transducer plate. 2) A SOI substrate or SIMOX technology is used. The cavity is formed by removing the insulation layer and is in a later step sealed by surface micromachining.



(d) Sensor category D (poly-crystalline plate, surface micromachining): 1) a poly-crystalline material is deposited by means of CVD or PVD onto a silicon substrate. The cavity is formed by a sacrificial etch step. 2) similar to 1 but processing takes place on a non-conductive substrate.

Fig. 1.3: Categorization of fabrication concepts for micromachined resistive and capacitive absolute pressure sensors.

etch procedure. These technological restrains result in a plate thickness of several microns and in order to achieve high sensitivity in rather large lateral plate dimensions of a few hundred microns. A resulting single-crystal silicon plate with a rigid support has to be named as advantages. The applied processes are well known and a number of etch stop techniques were developed to control the plate thickness pre-

benefits

cisely.

The drawback of a time consuming etch step with a significant impact on the sensor performance remains. Mask misalignment and wafer thickness deviations influence the plate geometry. The diaphragms have accordingly large lateral dimensions and the shape of the anisotropically etched cavity walls add to the overall lateral dimensions. One cross-sectional view of a classical low-pressure sensor with typical side wall geometry is given in Fig. 1.4(a). Wafer thinning might be used as miniaturization means but the thinning step prior to wafer bonding makes the substrate fragile.

drawbacks

Nevertheless, very small sensors have been fabricated. The thickness deviations of the transducer have been reduced by electrochemical etch stops or the application of silicon on insulator (SOI) substrates. The latter kind of substrate allows for deep reactive ion etching (DRIE) to form a sensor cavity with nearly vertical side walls resulting in a very small sensor die. A highly miniaturized sensor which employs DRIE technology is available from *Silicon Microstructures* and is depicted in Fig. 1.4(b). Very cost-effective sensor dice, as the latter one, and low-cost packaged dice for consumer applications as depicted in Fig. 1.4(c) are available. Besides low-cost implementations also very sensitive high performance sensor systems as depicted in Fig. 1.4(d) are obtainable either as MCM implementation from *Intersema* or fully integrated e.g. from *Robert Bosch* as presented in Fig. 1.4(e) and Fig. 1.4(f).

Sensor category B: single-crystal plate, $2\times$ bulk micromachining

Most of today's bulk micromachined capacitive absolute pressure sensors fit into category B. Sensors of this type have a silicon transducer plate which is bonded onto a second substrate. Either both substrates are bulk micromachined or the transducer substrate is two times bulk etched.

Numerous pressure sensors of category B, corresponding to Fig. 1.3(b), exist because of several advantages related to this approach. Single-crystal silicon as transducer material ensures reproducible mechanical properties of high quality combined with a low plate stress. Moreover, silicon is resistant to many medias and the open cavity on the wafer back side could be used as pressure port without additional protection (wiring and depositions on the wafer front side are protected by bonded glass). A commercial example which corresponds to sketch ② of Fig. 1.3(b) is the miniaturized pressure sensor from *Silicon Microstructures* presented in Fig. 1.5(a). It was designed for catheter tip application. Additional advantages of type B sensors are rigid plate supports and the possible thinning of the transducer substrate prior to the back side anisotropic wet etch.

benefits
(resistive sensors)

Two out of the ordinary miniature examples of category B use silicon fusion bonding after front side anisotropic cavity formation as depicted in sketch ④ of Fig. 1.3(b). Such a sensor for blood pressure monitoring was developed by *Lucas NovaSensor* in 1988. A picture of this sensor is given in Fig. 1.5(b). Figure 1.5(c) shows a more recent development that employs silicon fusion bonding. It depicts a small surface mountable device supplied by *Endevco*.

silicon fusion bonding

Technology category B offers some features making it especially attractive for capacitive pressure sensors. Capacitive transducers rely on the reproducible fabrica-

benefits
(capacitive sensors)

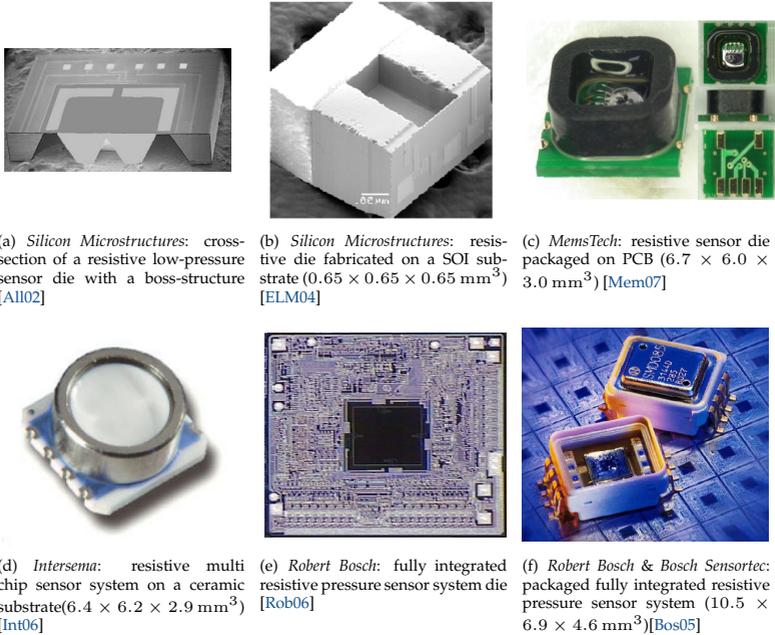


Fig. 1.4: Sensor category A (single-crystal plate, $1 \times$ bulk etch): Examples of existing sensors and sensor systems.

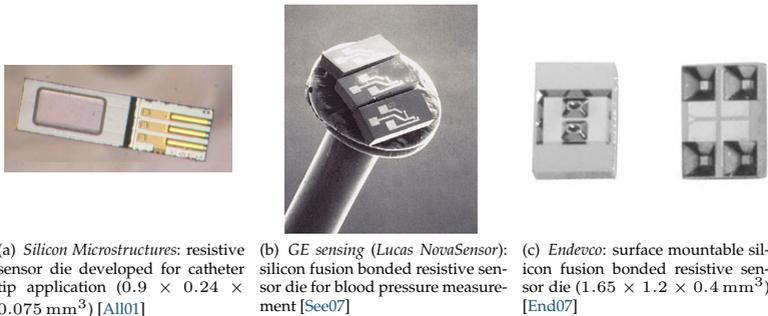
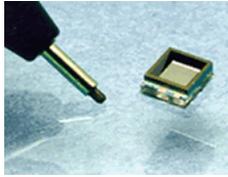
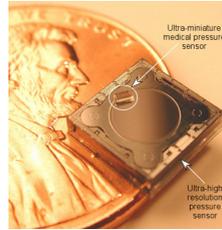


Fig. 1.5: Sensor category B (single-crystal plate, $2 \times$ bulk etch): Examples of existing resistive sensors.



(a) *Omron*: capacitive sensor die for blood pressure measurement ($2.9 \times 3.1 \times 0.9 \text{ mm}^3$) [Omi96]



(b) *Integrated Sensing Systems*: capacitive pressure sensor dice for vacuum and medical applications (smaller one: $0.5 \times 1.3 \times 0.3 \text{ mm}^3$) [Int07b]



(c) *VTI Technologies*: capacitive sensor die for automotive and consumer applications ($1.4 \times 1.4 \times 1.2 \text{ mm}^3$) [VTI07b]



(d) *VTI Technologies*: integrated capacitive pressure sensor system for consumer electronics ($\varnothing 6.2 \text{ mm}$; height 1.7 mm) [VTI07b]

Fig. 1.6: Sensor category B (single-crystal plate, $2 \times$ bulk etch): Examples of existing capacitive sensors and sensor systems.

tion of a gap between two electrodes. A two side bulk micromachining approach of a single wafer renders the electrode separation independent of the wafer thickness. Furthermore, the transducer wafer can be anodically bonded onto a non-conductive *Pyrex*[®] substrate which reduces the parasitic capacitance of the membrane support and counter electrode to a minimum. Consequently, a number of successfully commercialized capacitive pressure sensor elements are found to match the category's criteria. A picture of a small device fabricated by *Omron* is given in Fig. 1.6(a). It corresponds to sketch ① of Fig. 1.3(b). An even smaller die is available from *Integrated Sensing Systems* depicted in Fig. 1.6(b). The picture shows the miniaturized sensor, intended for wireless medical applications, on top of a larger version for ultra-low pressure detection. Both sensors are fabricated by means of a so-called dissolved wafer process illustrated in sketch ③ of Fig. 1.3(b). The third candidate is a bulk micromachined capacitive sensor developed by *VTI Technologies*, which is presented as die in Fig. 1.6(c) or as integrated MCM in Fig. 1.6(d). The latter system represents the state of the art in multi chip capacitive pressure sensor system integration. Besides its small outline it has a very low power consumption at a very high sensitivity and

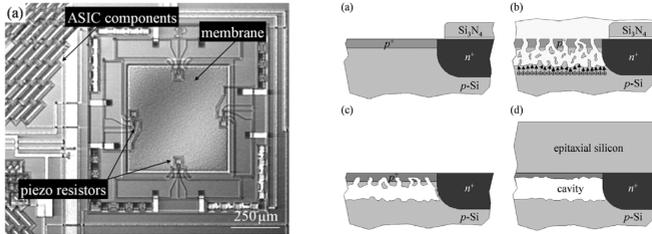
accuracy.

The technological challenge of this approach is the implementation of a reliable hermetic lead transfer and small die sizes.²⁶ The lead transfer area is origin of an undesired offset capacitance and is a potential source for leakage. *VTI Technologies* addressed this problem by implementation of a vertical back side contact as can be observed further below in Fig. 1.10(a).

Sensor category C: single-crystal plate, surface micromachining

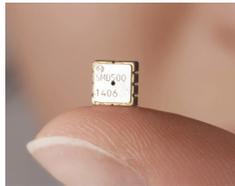
benefits

Category C of Fig. 1.3 is attractive for a pressure sensor design because it combines a rigid substrate with single-crystal transducer structures fabricated by a front side process without wafer bonding as vacuum sealing means. If necessary at all, device layer bonding takes place at the very beginning of the process to form an SOI substrate in case if no SIMOX (SIMOX: separation by implanted Oxygen) technology is adopted. This renders the concept most suitable for fully integrated systems.



(a) *Robert Bosch*: surface micromachined resistive pressure sensor with epitaxial silicon plate [Arm05]

(b) *Robert Bosch*: fabrication process sequence of the sensor element presented in Fig. 1.7(a) [Arm05]



(c) *Bosch Sensortec*: integrated resistive pressure sensor system ($5.0 \times 5.0 \times 1.6 \text{ mm}^3$) [Bos06]



(d) *Trionics Microsystems*: capacitive pressure sensor on a SOI substrate ($0.8 \times 1.0 \times 0.5 \text{ mm}^3$) [Ren00]

Fig. 1.7: Sensor category C (single-crystal plate, 1× surface etch): Examples of existing sensors and sensor systems. Process sequence depicted in Fig. 1.7(a): doping, porousification, thermal relocation and cavity formation, epitaxial growth of mono-Si and cavity sealing.

²⁶ Possible interference with intellectual properties: dissolved wafer process [Hay00]; touch-mode capacitive sensor: [Ko96a], [Ko96b].

Two technological implementations of this category need to be named: sensors fabricated either on SOI substrates or SIMOX technology, which correspond to sketch ② of Fig. 1.3(c), and epitaxial grown silicon on top of a porous silicon sacrificial layer. The latter technology was developed by *Robert Bosch* and is illustrated by figure sketch ① of Fig. 1.3(c). An example picture of this sensor in the pre-development stage can be found in [Arm05] and is given in Fig. 1.7(a) together with the corresponding process flow in Fig. 1.7(b). *Bosch Sensortec* supplies this resistive sensor with monolithic readout in a very small ceramic housing. This sensor system is depicted in Fig. 1.7(c) and can be regarded as state of the art in resistive pressure sensor system integration. It combines a very small outline with a very low power consumption at a high resolution and accuracy. A further implementation of a capacitive pressure sensor fitting into this category based on SOI technology is presented in Fig. 1.7(d). It is a sensor which was developed at *CEA-LETI* and is marketed by *Trionics Microsystems*.

Both technological approaches are not likely to be first choice for capacitive sensing elements. Reproducible gap heights may be hard to archive by porosification of silicon and the semiconducting substrate will create undesirable high parasitic capacitances in both cases which depend on light and temperature. Despite these difficulties, *Robert Bosch* has recently published information about conceptional studies aiming at the development of a capacitive pressure sensor with a vacuum cavity created by porous silicon removal [Kne07].

drawbacks

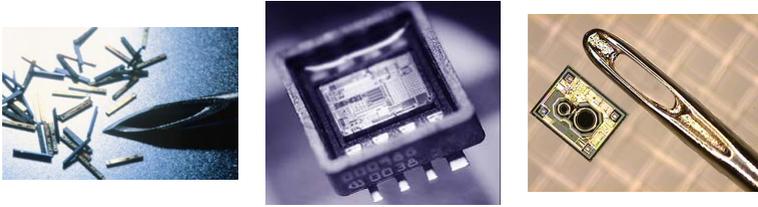
Sensor category D: poly-crystalline plate, surface micromachining

Sensors of category D, as depicted in Fig. 1.3(d) are fabricated by means of surface micromachining technologies. All layers are poly-crystalline and either chemical vapor deposited (CVD) or physical vapor deposited (PVD). The layer thicknesses are typically below three microns resulting in features of small lateral dimension. The degree of miniaturization is mainly determined by the accuracy of layer deposition and lithography. One of the smallest pressure sensors on the market is a surface micromachined piezoresistive die fabricated by *Silex Microsystems* (it is depicted in Fig. 1.8(a) side by side with a 1 mm cannula). Sensors of this category are considered most suitable for high volume production of low-cost elements. Furthermore, the comparably small features on top of a rigid substrate are less susceptible to packing stresses originating from the die attach area.

benefits

Besides these advantages there are serious drawbacks related to this technological concept. The development, adjustment and maintenance of the deposition processes is cost- and time-consuming. The determination and modeling of the mechanical material properties of the functional layers are difficult. Film stresses must be controlled. Furthermore, the geometry of the transducers become more complex due to stacked conformal depositions which make analytic and numeric transducer modeling more difficult. Complex shapes of the plate and plate support with an impact on the sensor performance are created. At first sight, surface micromachined sensors seem to be first choice for fully integrated sensor systems but micromachining often adopts specially tuned processes or different materials which are not part of the standard CMOS process and merging of microsystem and electronics becomes

drawbacks



(a) *Silix Microsystems*: resistive pressure sensor die for catheter applications ($1.3 \times 0.16 \times 0.1 \text{ mm}^3$) [Sil07]
 (b) *Infineon Technologies*: integrated capacitive pressure sensor system for automotive applications ($7.0 \times 8.6 \times 2.8 \text{ mm}^3$) [Inf07a]
 (c) *Kavlico*: integrated capacitive pressure sensor system for automotive applications [Kav07]

Fig. 1.8: Sensor category D (poly-crystalline plate, 1×surface etch): Examples of existing sensors and sensor systems.

challenging. These difficulties related to surface micromachined transducers can be overcome as demonstrated by a number of large companies which supply fully integrated pressure sensor systems. Amongst them are *Infineon* and *Kavlico* which have developed integrated capacitive pressure sensor systems for the automotive industry.²⁷ A monolithically integrated capacitive barometric air pressure sensor implementation from *Infineon* is depicted in Fig. 1.8(b). The sensor die presented in Fig. 1.8(c) is intended for a TPMS and was developed by *Kavlico*.

Many capacitive pressure sensors have been developed scientifically but the small number of commercial implementations emphasize the difficulties related to surface micromachining of poly-crystalline sensors. Traditionally, most of the implementations adopt silicon as substrate material. This might be related to the history of surface micromachining and the assimilation of deposition processes originating from integrated circuit fabrication. Of special interest as fabrication means are low pressure chemical vapor deposition (LPCVD) processes which exhibit a superior quality compared to alternative plasma enhanced and physical deposition processes, i.e. homogeneity, reproducibility and chemical composition. The standard LPCVD technologies have been developed for use of the IC industry on silicon and the deposition temperatures range from 450 °C to 800 °C. Currently, there is no technological implementation reported which utilizes the advantages of high temperature, high quality LPCVD processes for capacitive pressure sensors diaphragm formation on a non-conductive glass substrate with a high melting point. Such a device would correspond to concept 2 of Fig. 1.3(d). The resulting structure would be similar advantageous for capacitive transducers as the first two of Fig. 1.3(b) but would offer all the miniaturization and batch processing potentials of category D.

surface microma-
chining on insulat-
ing bulk material

²⁷ The historic manifold pressure sensor (MAP) was joined by barometric air pressure (BAP) sensors, tire pressure monitoring systems (TPMS), pressure sensors for side air bag ignition (SAB) and passenger occupation detection systems.

1.5 Challenges and scope of this work

The MEMS pressure sensor market today is dominated by piezoresistive sensors. A number of reasons can be identified for their success. Firstly, bulk micromachining was developed earlier and the first surface micromachined capacitive pressure sensor was presented eight years after his resistive counter player. Secondly, the system integration of capacitive sensors, i.e. packaging and interfacing, is more complex.

A comparison of both transducer principles shows up a number of advantages which should make the surface micromachined capacitive sensor first choice: small size, low power consumption, high sensitivity, robustness, high stability, and high achievable operation temperatures. It seems surprising that all these advantages did not lead to a larger number of capacitive pressure sensor systems. Careful consideration reveals that many of the advantages are lost during system integration. The system size is determined by the large and bulky housing with media separation. Also the stability and operation temperature range are often limited by the system package. The necessary readout is more complex, hence larger, more expensive and consumes power proportional to the number of integrated gates. Finally, the readout again limits the temperature range. Table 1.4 summarizes the benefits and drawbacks of piezoresistive and capacitive pressure sensor systems and illustrates, that the benefits of a capacitive die do not necessarily lead to an advantageous system.

resistive vs capacitive pressure sensors

Table 1.4: Comparison of piezoresistive and capacitive pressure sensor system characteristics with an assessment of the system’s components on the system’s overall performance. Magnitude of attribute impact: ⊕ (strong positive), + (positive), / (none), - (negative), ⊖ (strong negative).

attribute	piezoresistive system			capacitive system		
	sensor	housing	readout	sensor	housing	readout
system size	+	⊖	+	⊕	⊖	-
stability	+	⊖	+	⊕	⊖	+
sensitivity	+	-	/	⊕	-	/
robustness	-	-	-	+	-	-
power-consumption	-	/	+	⊕	/	-
temperature range	-	⊖	-	⊕	⊖	-
costs	+	⊖	+	⊕	⊖	-

The system integration can be regarded as ultimate cause for the defeat of capacitive pressure sensors against their resistive opponents. This holds true for industrial sensing systems requiring sophisticated media protection finally leading to expensive and bulky overall dimensions. Today’s MEMS technology and electronics have become cost-effective and have emerged in all kinds of consumer products. For this market segment the situation might change in a favorable way for capacitive transducers. The surrounding media is often air or sometimes water. In these cases coatings are sufficient as media separation resulting in a very small and thin system, which can be fabricated at a competitive price. CMOS technologies have developed

new pressure sensor market

dramatically and a growing number of capacitive readouts are on the market with a low-power consumption supporting the implementation of capacitive pressure sensor systems for hand-held battery driven products. Moreover, it is possible to figure out many new applications in which only pressure switches or a rough quantization of pressure is required. In these cases the data acquisition is greatly simplified and, due to the possible high sensitivity of capacitive transducers, the readout can be accomplished with almost no extra circuitry (provided that virtually all relevant consumer products have already built-in intelligence).

Table 1.5: Summary of development objectives and methods of resolution.

objective	resolution	comment
low-fabrication costs	surface micromachining	die size reduction
small die size	surface micromachining	small and thin sensors
low power consumption	capacitive detection	
mechanical robustness	touch-mode operation	bust pressure increased
high sensitivity	capacitive transducer	simplified readout
improved process control	fused silica substrate	improved stress control
simplified packaging	fused silica substrate	no parasitic capacitances
readout simplification	fused silica substrate	simplified equivalent circuit

former work

The presented work is based on former research projects related to capacitive pressure sensors and electrostatic actuators at the Institute für Mikrosensoren, -aktuatoren und -systeme (IMSAS) of the University of Bremen. Capacitive pressure sensors were developed with a device structure similar to the schematic cross-section given above in Fig. 1.9 ([Cat97], [Elb98], [Egg00b]). Issues during sensor operation were related to the parasitic capacitances to the bulk. Especially, the large diffusion capacitance of the implanted bottom-electrode depends on the whole fabrication process and is difficult to control. This capacitance and the MIS capacitor (MIS: metal-insulator-silicon) like structure of the membrane support on top of the conductive substrate made the sensor susceptible to light and temperature. Work on electrostatic actuators for display applications showed the general feasibility of surface micromachining of LPCVD layers on fused silica ([Pan05], [Kni06]). The development of the sensor presented in this thesis was initiated by a project with the objective to develop small transducer elements for remotely powered medical implants.²⁸ It intends to combine the achievements of both research activities, i.e. the capacitive pressure sensor development and the integration of electrostatic actuators on silica, to develop a fabrication process for a highly miniaturized surface micromachined capacitive pressure sensor on an insulating fused silica bulk.

Small cost-effective devices are required for new applications of the fastest growing consumer market. The development need to aim at a simplified sensor pack-

objectives and methods of resolution

²⁸ Arbeitsgemeinschaft industrieller Forschungsvereinigungen "Otto von Guericke" e.V. (AiF), PROgramm "INNOvationskompetenz mittelständischer Unternehmen", Projekt: "Entwicklung eines neuartigen Systems aus Implantat und Auswerteinheit zur Messung des intraokularen Drucks" Förderkennzeichen KF0430901KUL2.

age and readout to support the spreading of capacitive pressure transducers into this market segment. This work focuses on the die with the intention to improve package, readout, and costs by a special design of the transducer itself. Table 1.5 summarizes the goals and the respective methods of resolution: a capacitive surface micromachined transducer on a non-conductive substrate (fused silica) is proposed which will be small and cost-effective. It will have a high sensitivity due to its low offset capacitance caused by the non-conductive substrate. The equivalent circuit of the sensor shall become similar to a high quality floating capacitance which enables a straightforward data acquisition. Figure 1.9 illustrates the parasitic capacitances of a surface micromachined capacitive transducer on a conductive substrate in comparison to an element fabricated on an insulator. Besides the eliminated capacitances of the bottom-electrode, non from electrical tracks exists. This includes additional parasitic capacitances which may be created from bond wires or conductive adhesives towards the sensor bulk simplifying packaging and multi chip integration. The small dimensions of the surface micromachined die and transducer structures are expected to facilitate the packaging because thermal stresses in the package are proportional to the lateral die dimensions.

The concept should implement a dielectric insulation of both sensor electrodes. This measure guarantees reliable operation in case of an accidental contact of transducer plate and counter electrode during pressure overload. Sensors of this kind could also be run on purpose in touch-mode. After plate touch-down the characteristics are mainly determined by bending moments. Therefore, plate thickness and Young's-modulus have a high impact on the sensor performance but stress deviations arising from the fabrication or packaging process primarily cause shifts in the touch-down pressure. In addition, touch-mode sensors are expected to be highly sensitive having a near linear characteristic over a wide pressure range.²⁹ Touch-down operation is considered to improve the fabrication yield and to simplify the sensor readout due to the named advantages. These assumptions shall be tested in this work.

touch-mode operation

The objectives and development approaches are not new and today there are a number of micromachined pressure transducers on non-conductive substrates on the market which have already been presented with photographs and dimensions in Section 1.4.2. Figure 1.10 gives cross-sectional views of these sensors for comparison of their fabrication technologies to illustrate difference to the new approach discussed in this work:

similar sensor concepts on the market

- VTI Technologies [VTI07] has developed a bulk micromachined sensor which consists of an anodically bonded stack of three wafers as depicted in Fig. 1.10(b): The anisotropically wet-etched flexible plate is anodically bonded onto a non-conductive Pyrex[®] substrate which has electric vias. The second silicon substrate on the backside carries the electrical interconnects. The sensor die can be mounted in a reflow solder process.
- A similar structure achieved with a different technological approach is fabricated by Integrated Sensing Systems [Int07a]. The process leads to small and

²⁹ Extensive work on modeling of capacitive touch mode pressure sensors has been conducted by W. H. Ko and coworkers: [Ko97] [Wan98] [Wan99] [Ko99] [Men99]. Also a monolithic integration was developed by this group [Guo00].

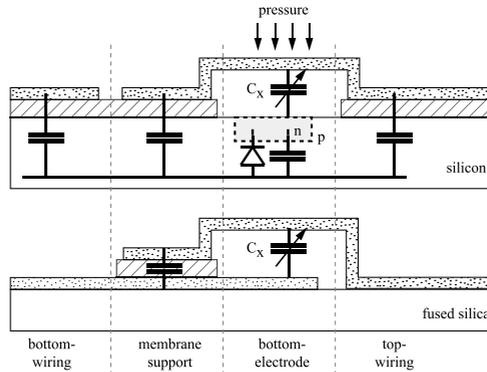


Fig. 1.9: Parasitics of capacitive pressure sensors fabricated on silicon compared to devices on fused silica.

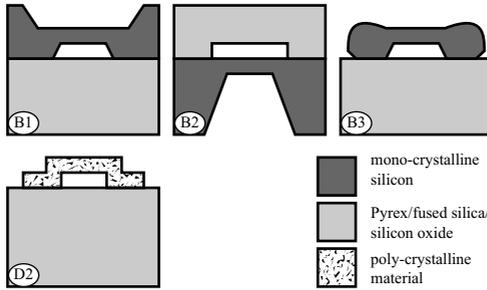
thin bulk micromachined capacitive pressure sensors: the transducer plate is again anisotropically wet structured into a silicon wafer which is anodically bonded onto a *Pyrex*[®] substrate [MA99] [Tad99] [Zha01]. All the unused silicon of the bonded wafer is in a later step dissolved leaving a *Pyrex* chip with a thin bulk silicon transducer. A cross-sectional view of the sensor is given in Fig. 1.10(c).

- *Omron Corporation* [OMR07] has also developed a miniature pressure sensor on a non-conductive *Pyrex*[®] substrate. Different to *VTI Technologies* no vias are implemented and the plate is supported in the center [Omi96]. A photograph of this sensors was already given in Fig. 1.6(a).

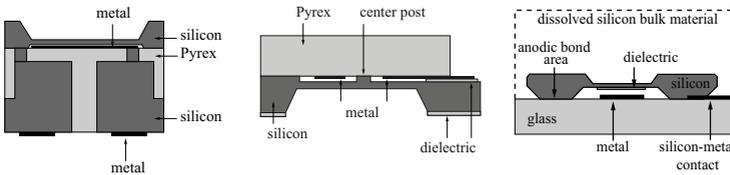
All three sensor implementations fit into sensor category B described above. It provides the opportunity to fabricate single-crystal transducers on a non-conducting substrate with a reproducible cavity height required by a capacitive transducer. By considering Fig. 1.10(a) and the current sensor market, it appears that a sensing element which employs surface micromachining on a non-conductive substrate is currently missing.

The choice of surface micromachining technology is straightforward to achieve the desired small system dimensions. However, considerable difficulties have to be expected: the system design and its modeling becomes challenging due complex conformal depositions causing as complex transducer geometries, the material properties depending on the deposition process must be controlled accurately, and some of these properties are in addition difficult to measure. These issues need to be addressed.

LPCVD technologies are inevitable for the wanted surface micromachining process because of their superior layer quality, homogeneity and reproducibility compared to PECVD (PECVD: plasma enhanced chemical vapor deposition) processes



(a) technological categories of capacitive absolute pressure sensors



(b) process implemented by VTI Technologies (according to [Ruo05]) (c) process implemented by Omron (according to [Omi96]) (d) process implemented by ISSYS (according to [MA99])

Fig. 1.10: Cross-sections of capacitive pressure sensors on non-conductive substrates as brought to market by VTI Technologies, Omron and Integrated Sensing Systems (ISSYS).

which might be run on *Pyrex*[®] substrates with a lower softening temperature. A new substrate material is necessary and non-conductive fused silica³⁰ of high purity was chosen for its high softening temperature of 1600 °C. It enables the deposition of all standard LPCVD layers but the low thermal expansion coefficient of fused silica will also lead to high tensile stresses in these layers which require process adaption. This technological hurdle is expected to offer an important benefit: the overall layer stress will be mainly determined by the expansion coefficient mismatches of the involved layers and can be processed reproducibly. The sensor design presented in this thesis eliminates all parasitics to the substrate by using fused silica wafers. The only remaining parasitic capacitance is caused by the transducer support overlapping the leads of the bottom-electrode (see Fig. 1.9). This capacitance is reduced to a minimum for the lead transfer area is only a fraction of the membrane support area. Moreover, its magnitude can be controlled by mask geometry and thickness of the dielectric bottom-electrode insulation. It is expected that the presented approach renders the offset capacitance independent of semiconductor effects, less sensitive to temperature, and unaffected by light.

fused silica as substrate material

Electronics on fused silica substrates have been already proposed many years ago

³⁰ Fused silica is amorphous silicon oxide of high purity and is lacking the metal ion impurities of other glasses.

[Sar94] but are still under evaluation [Xue05] for special applications, i.e. low-power, high-temperature, and RF circuits. Therefore, the presented sensor could only be integrated into a multi chip system. However, such an approach is considered to have many advantages with respect to system flexibility and commercialization:

- Readout and sensor can be optimized separately.
- The readout design can be updated frequently to benefit from the rapidly changing and improving CMOS fabrication technology while the expensive sensor process remains unchanged.
- Off-the-shelf readouts can be used reducing development costs and risks.
- The system yield can be increased by shorter and less complex processes and a system assembly with pre-tested known-good-dice.
- An adjustment of the sensor performance to customer requirements can be accomplished easier and will be less costly.

The same sensor die and core packaging process, i.e. sensor die-attach and encapsulation, can be combined with multiple specialized readouts. Therefore, individually differing systems with only as much intelligence integrated as necessary can be realized providing a means to reduce the costs for small and medium volume products. But a multi chip approach also opens up possibilities for high-volume products to meet demands of the drop in prices with continuous further development of the individual system components.

As conclusion, cost-effective, simple, and small sensor and system solutions are required. It is the goal of this work to improve the current state of the art by providing a miniaturized sensor element which allows the down-sizing of the overall system outline, which reduces the required readout complexity, and which simplifies the transducer packaging procedure in general.

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*We do not know one millionth
of one per cent about anything.*

Thomas Alva Edison

2

Micromachining on Fused Silica

A brief description of the micromachining techniques necessary for surface micromachining a pressure sensor on fused silica is presented throughout this chapter. Emphasis is placed on basic issues related to processing on fused silica. The point of view is not limited to the fabrication of the sensor which is presented in Chapter 3 but the described technological means are in close relation to the developed sensor structure. For this reason, Fig. 2.1 gives a cross-sectional view of a single sensor cell as will be presented in the preceding chapter. It illustrates the general design features to avoid confusion with some hints and remarks of this chapter which refer to the sensor process.

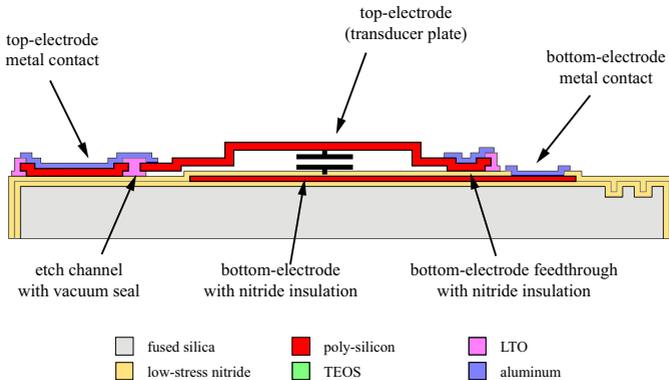


Fig. 2.1: Cross-sectional view of a single cell of the presented pressure sensor illustrating the basic design features.

The special kind of substrate material offers positive features for integrated electronics, capacitive sensors as well as optical MEMS devices, but there are also serious obstacles to be met. Some of these will be discussed together with more common

technological aspects not related to the choice of substrate but of special concern for the presented sensor. Finally, information on some aspects is given which seem to be insignificant but which cause a lot of trouble to identify and to work around.

Much effort is spent on the control and understanding of LPCVD layer formation during the development of a surface micromachining process. This is reflected in the discussion of these layers in the proceeding sections. Short names are assigned to the deposits for the sake of compact writing. Table 2.1 gives a summary of these names with brief comments on the ascribed layers. More details about the individual process condition can be found in Tab. B.11 in the appendix.

Table 2.1: Summary of short names assigned to the LPCVD deposits relevant for this work.

short name	brief description of the deposit
Nit-D20	silicon rich nitride, $\text{SiN}_{0.61}$, approx. -200 MPa stress on silicon
Nit-Z10	silicon rich nitride, $\text{SiN}_{0.96}$, approx. $+100$ MPa stress on silicon
Nit-Z20	silicon rich nitride, $\text{SiN}_{1.04}$, approx. $+200$ MPa stress on silicon
PBOR560	poly-Si, in situ boron-doped, deposition at 560 °C
PBOR600	poly-Si, in situ boron-doped, deposition at 600 °C
PBOR620	poly-Si, in situ boron-doped, deposition at 620 °C
PBOR560BT	poly-Si, highly in situ boron-doped, deposition at 560 °C
PBOR580L	semi-crystalline Si, moderately in situ boron-doped, deposition at 580 °C
aSiX585	semi-crystalline Si, un-doped, deposition at 585 °C
Poly4Zol	poly-Si, un-doped, deposition at 620 °C
TEOS4Z	high-temperature LPCVD oxide, TEOS source
LTO450Z4	low-temperature LPCVD oxide, DES source

content of
this chapter

This chapter starts with a discussion about alternative substrate materials which is concluded with the choice of fused silica for this work. Film stress on silica is a special concern and its composition as well as the applied measurement technologies are explained in detail. Related to this topic are also viscous deformation of layer and substrate, and the mechanical properties of the deposits. A simple means to measure the film's biaxial modulus is presented followed by results for relevance deposits.

LPCVD processes are discussed showing some special features which are related to the chosen substrate. The choice of functional layers is confined by the silica due to the stress shift caused by the substrate's low thermal expansion coefficient. For instance, only silicon-rich, instead of stoichiometric nitride, can be deposited in relevant thicknesses. But also the selection of the transducer layer for the presented sensors was particularly influenced by the substrate material. The sensitive plates are made out of in situ boron-doped poly silicon, a deposit which is highly compressive on silicon but tensile on silicon. It turns out that the fabrication of this special layer is complex, leading to an extensive presentation of fabrication concerns and resulting physical properties.

In first place, the stress is greatly influenced by the substrate, but also the dielectric

properties are affected as can be concluded for the discussion on silicon-rich nitride. Turning away from layer formation, lithography on silica and etching technologies are addressed. Lithography is influenced by the usually high stress levels on silica in combination with the, in comparison to silicon, lower modulus of the bulk. Wet etching and especially sacrificial layer etching of silicon oxide on silica poses strong demands on the selectivity of the used etchants and masking material. This chapter is finally concluded with a brief description of some of the few bulk micromachining tests which have been run on silica.

2.1 Introduction

CMOS technologies are successively improved with the objective of more shallow and planar devices [Gog04]. In contrast, the trend in MEMS is towards thicker structures with higher aspect ratio. Hence, the paths of MEMS and CMOS technologies indicate a significant divergence. In the past considerable efforts were focused on integrating transducers and electronics on a single die (especially capacitive transducers) resulting in strong technological restraints and high development costs combined with a low flexibility.¹ Today, only 8% of successfully commercialized systems are monolithically integrated [Bry96] and recent systems designed as multi chip modules (MCM) (resistive system:[Dan03], capacitive system: [VTI07]) demonstrate the technological and commercial competitiveness of the approach. Reasons for the success of MCMs are lower development costs, higher flexibility and the possibility to individually optimize the system components. CMOS processes, die level testing capabilities, and MEMS packaging technologies have been constantly advanced over the past years. This is motivation to continue the development of highly specialized processes for the fabrication of transducers, even on alternative non-silicon substrates, aiming at modular and optimized individual component.

reasons for
alternative
substrates

Considering capacitive pressure sensors as a mature example, many proposed devices can be found but only a few are commercially available. This is surprising because of the great demand for very small devices showing low power consumption, good temperature stability and high sensitivity. Four major challenges exist which seem to inhibit a successful commercialization of capacitive surface micromachined transducers:

challenges for
capacitive trans-
ducers

1. complexity and availability of proper read-outs
2. reduction and control of the transducer's parasitic capacitances to facilitate a simple electrical readout
3. parasitic capacitances and electric instabilities of the package hindering MCM integration
4. tight control of the mechanical properties of the surface-micromachined functional layers.

Non-conductive fused silica was chosen as substrate material for this work because it was considered to improve all the latter issues:

motivation for
this work

¹ One example of a successfully commercialized integrated capacitive sensor is presented in [Sch98] and an integrated resistive system is e.g. marketed by Robert Bosch [Rob06].

1. Transducers on silica can be designed as two-terminal floating capacitances and can be treated electrically like a standard capacitor.
2. All parasitic capacitances to the bulk disappear and the remaining capacitance is determined by the mask design.
3. The insulating substrate prevents any capacitive coupling of the package and bond-wires to the transducer bulk.
4. Stress control and homogeneity increases on silica due to the high influence of the thermal stress component (as extensively discussed in Section 2.2).

The following chapter focuses on how to make use of improved stress control and the design aspects are addressed in Chapter 3.

2.1.1 Non-silicon substrates for MEMS and electronics

This work suggests the development of a transducer on an insulating substrate. Today there are already a few non-conductive alternative substrate materials adopted having their individual benefits and drawbacks. The technology is commonly referred to as silicon on insulator (SOI) and processing on a non-conductive bulk material is a sub category of the broad field of SOI technology.² Possible non-conductive substrates are:

- **borosilicate glass:** glasses especially *Pyrex*[®] (Corning: 7740) have become very common and many devices today require anodic bonding of silicon and glass. *Pyrex*[®] is particularly suited for wafer bonding because of a thermal expansion which matches the one of silicon very well.³ The resulting structure is sometimes also referred to as silicon on glass (SoG). Borosilicate glass is a low-priced substrate material but its thermal elongation is matched to the cost of a low softening temperature of about $T^{(\text{soft})} = 830\text{ }^{\circ}\text{C}$. This limits the processing temperatures to roughly $500\text{ }^{\circ}\text{C} - 600\text{ }^{\circ}\text{C}$ if substrate deformation could not be accepted. Therefore, anodic bonding, PVD, PECVD and some lower temperature LPCVD processes can be run on *Pyrex*[®]. The LPCVD deposition of poly silicon on *Pyrex*[®] as masking material for deep wet etching has been reported [Ver03] [Ber00] but no high-temperature anneals can be conducted. Besides MEMS also the electronics industry uses glass very commonly as substrate material: today almost every solar cell is processed on glass, and furthermore thin film transistors for display applications must be placed on transparent substrates. Three technologies have been developed to obtain poly-silicon layers with acceptable electrical quality at a very cheap price on glass substrates without the need for a long high temperature anneal: solid phase recrystallization, laser crystallization (LC) of amorphous silicon

borosilicate
glass

² Reviews on SOI technology are given by [Pl600], [Ren00] and [Mok00].

³ The TECs given in Tab. 2.2 are temperature dependent. For stress-less bonding of silicon and *Pyrex*[®] their elongations at a certain temperature difference are matched. The temperature dependency of *Pyrex*[®] is illustrated e.g. in [Gre88].

and low-temperature metal induced crystallization (MIC, also sometimes referred to as stress assisted recrystallization).⁴ Most of the mechanical capacitive transducers, which can be found, are utilizing the merits of the SoG concept for accelerometer fabrication (see e.g. [Cha05]).

- **sapphire:** the idea of processing on a sapphire (single crystal aluminum oxide Al_2O_3) substrate dates back to the early 60th [Man64]. Till today, silicon on sapphire (SoS) technology draws a lot of attention due to its potentials for IC and MEMS development.⁵ Epitaxial growth of silicon on a perfect insulator can be utilized for the fabrication of very fast circuits with a very low power consumption due to the achievable extremely small junction capacitances. Transistor footprints can be downsized because there are no insulating well regions necessary anymore. Further advantages include high insulation resistivity, low susceptibility to radiation, and high allowable operation temperatures. IC processing on SoS is very similar to other SOI processes.⁶ The two most important drawbacks of sapphire are the high substrate costs and the difficult device layer fabrication related to the lattice mismatch of silicon and sapphire leading to a very high number of stacking faults during epitaxial growth. A solution to this problem is solid phase crystallization of the grown layer.⁷ The technology was for years limited to aerospace and defence applications but today there is a growing number of commercial circuits available (e.g. RF switches).

sapphire

SoS technology is also applied in MEMS. There are a number of piezoresistive pressure sensors available on the market which are fabricated on sapphire. The implemented sensor technology comprises a single crystal sapphire transducer plate with silicon piezoresistors. The single crystal transducer exhibits no hysteresis or degradation and the dielectrically insulated resistors can withstand high temperatures in comparison to implanted piezoresistors in silicon. The sapphire itself melts at $T^{(\text{melt})} = 2050\text{ }^\circ\text{C}$, about $600\text{ }^\circ\text{C}$ degrees above the melting point of silicon. Sensors of this kind are high priced transducers especially designed for high temperature and high precision applications such as pressure measurement in injection moulding tools (examples can be found at [CRA07] or [SEN07]).

The most important drawback of sapphire, with respect to surface micromachining, is the large TEC of $(5-9) \times 10^{-6}\text{ K}^{-1}$, which leads to a very high compressive thermal stress component of deposited standard LPCVD layers (for comparison, $\alpha_{\text{Si}} = 2.616 \times 10^{-6}\text{ K}^{-1}$). Fabricated plates or supported beams will buckle due to the compressive stress if deposited my means of LPCVD. The mismatch is large and a tuning of the standard layers may not be applicable to achieve depositions with tensile stress. Metals with their comparably higher TECs may remain as possible surface micromachining materials.

- **mono-crystalline quartz:** quartz (mono-crystalline SiO_2) is available as wafer

mono-crystalline quartz

⁴ MIC might be an interesting means for film stress reduction on fused silica. Literate sources on MIC are: [Wan01][Has04] (nickel), [Gal02] [Hsu04] (aluminium induced crystallization (AIC)).

⁵ An extensive review on electronic SoS devices is presented in [Cri87].

⁶ A brief introduction to SoS processing can be found in [Nak04].

⁷ Substrates of this kind are common and marketed by *Peregine* under the name $\text{UTSi}^{\text{®}}$ [Per07].

blank. It is expensive but due to its piezo-electric properties often used as bulk oscillator material or as substrate for surface acoustic wave (SAW) devices. Also a passive tire pressure monitoring system (TPMS) has recently been developed using SAW technology on quartz (see [Tra07] or [Fre05] for technical details). Regardless its electromechanical properties, quartz is often adopted as substrate for chemical or biological microanalysis systems. Quartz and similarly fused quartz is an inert and non-conductive material, which has a very low absorption in the UV range, has no luminescence, and is suitable for electrophoresis (see also literature cites for fused silica below).

Wet chemical processing of quartz is as common as low-temperature surface micromachining, but similar to sapphire it is difficult to fabricate layers with tensile stress on mono-crystalline quartz due to its large TEC of approximately $(8-13) \times 10^{-6} \text{ K}^{-1}$. This renders the material not suitable for surface micromachining of free standing clamped plates and membranes fabricated by means of LPCVD. Additionally, there is a phase transition taking place at $573 \text{ }^\circ\text{C}$ which confines the applicable range of process temperatures. The technologies for bulk micromachining of plates and cavities are available. Bonding of quartz to quartz and quartz to silicon have been reported for either general hermetic encapsulation or for wafer level packaging of resonant transducers [Ran99].

fused quartz &
fused silica

- fused quartz and fused silica:** the generic term for all silica glasses is vitreous silica. Historically, opaque and transparent materials were called fused silica and fused quartz, respectively. The opaque material was fabricated by means of melting sand whereas transparent silica glass was made out of quartz. Today, all vitreous silica is transparent due to advances in raw material beneficiation and the term fused quartz is used for sintered natural occurring crystalline silica. If silica glass is synthetically fabricated, it is referred to as fused silica. Both materials are similar and of high purity when they come in semiconductor grade. Significant differences are measurable only for the optical properties. Whereas both glasses are highly transparent for small wave lengths (UV range), fused silica has a high absorption at wave length $2.73 \mu\text{m}$ due to hydroxyl ions incorporated during the synthetic pyrolysis. Synthetic silica should be preferred as substrate material for micro-mechanical transducers because its mechanical and thermal properties can be controlled more precisely.⁸

Most commonly, silica substrates can be found in biomedical and micro fluidic applications because of their inertness, UV transmission characteristics, fluorescence freeness, and suitability for electrophoresis.⁹ Fused quartz is chosen as structural material because of its high softening temperature $T^{(\text{soft})} = 1600 \text{ }^\circ\text{C}$ and its low TEC of $\alpha \approx 0.5 \times 10^{-6} \text{ K}^{-1}$ which enables the material to withstand high temperatures and temperature gradients (e.g. LPCVD furnace tubes are made out of fused quartz). Therefore, its is straightforward to use

⁸ Information on fused silica and quartz can be found on the manufacturer's web pages (see e.g. [Mom07], [Gid07], [Mac00] or [Sch07b]).

⁹ Examples of micro fluidic devices in silica can be found in [Ver03], [Flu96], [Bec98] or [Zhu06].

fused silica as substrate material for surface micromachining of high temperature LPCVD layers.

Scientific work has been conducted on surface micromachined optical switches on fused silica able to operate in transmission [Pan05] [Kni06]. The intention was to benefit from the thermal and optical properties of this special substrate. It comes that former micromachining on fused silica focused on biomedical and optical applications but, to the best knowledge of the author, no work was concerned with mechanical sensors.

Table 2.2: Mechanical and thermal properties of non-conductive substrate materials.

property [unit]	silicon	Pyrex [®]	fused silica	sapphire	quartz	fused quartz
$\alpha@20\text{ }^\circ\text{C}$ [10^{-6} K^{-1}]	2.616	3.25	0.5	5– 9	7.87– 13.37	0.4– 0.7
$T^{(\text{strain})a}$ [$^\circ\text{C}$]	–	510	980	–	–	990– 1120
$T^{(\text{anneal})b}$ [$^\circ\text{C}$]	–	560	1080	–	–	1100– 1215
$T^{(\text{soft})c}$ [$^\circ\text{C}$]	–	821	1600	–	–	1580– 1730
$T^{(\text{work})}$ [$^\circ\text{C}$]	–	1252	1180	–	–	–
$T^{(\text{melt})}$ [$^\circ\text{C}$]	1414	–	–	2050	1657– 1710	–
E [GPa]	129.5– 186.5	62.75	72	345– 460	76.5– 97	70– 78
ν [1]	–	0.2	0.17	–	–	0.17
G [GPa]	57.5– 79.0	26.1	31	145	44	31
$\sigma^{(\text{yield})}$ [GPa]	2.8– 6.8	–	1.25	–	–	1.1
λ_{th} [W(m K) ⁻¹]	156	–	1.31	23.1– 25.2	6.5– 11.7	1.2– 4.0
price	low	low	moderate	high	high	moderate
diameter [mm]	50– 300	50– 300	50– 200	25– 100	25– 200	50– 200
references	[Hak02] [Mad02]	[Cor05]	[Sch07]	[Mat07b]	[Mad02]	[Mom07] [Mat07a]

^a The stain point is defined to be at dynamic viscosity $\eta = 10^{14.5}$ Poise = $10^{13.5}$ Pa s. It is the temperature at which the internal stresses are substantially relieved after four hours [Mac00].

^b The anneal point is defined to be at dynamic viscosity $\eta = 10^{13.0}$ Poise = $10^{12.0}$ Pa s. It is the temperature at which the internal stresses are substantially relieved after 15 minutes [Mac00].

^c Glass deforms under its own weight at softening temperature. This takes place approximately at a dynamic viscosity of $10^{7.6}$ Poise = $10^{6.6}$ Pa s [Mac00].

2.1.2 Fused silica as non-conductive substrate material

This work is concerned with the fabrication of free standing structures fabricated by means of high temperature surface micromachining. Considering the discussion of possible substrate candidates given in the itemization of Section 2.1.1 and the material data summarized in Tab. 2.2, fused silica can be regarded as an attractive substrate for surface micromachined capacitive transducers. This section will focus in more detail on fused silica as substrate material with the intention to summarize possible merits and expected difficulties related to this material.¹⁰

Fused silica wafers offer some benefits for transducer development with respect to the transducer design and the required processing technology:

- No parasitic capacitances to the substrate exist due to its non-conductivity. This results in a simplified electrical transducer model that in turn is simplifying the development of a readout. The transducer performance becomes independent of the pad and wiring layout resulting in a more flexible design. Large conductive areas become feasible simplifying the chip mount and permitting interconnects with conductive adhesives which do not create difficult to control parasitic capacitances. Furthermore, no bulk contact needs to be implemented and through-wafer vias can be fabricated with no undesired capacitance to the bulk material. Metal tracks can be replaced by wider lines of doped poly-silicon in cases if operation at high temperature is required or if corrosion of metal may take place.
- Most of the standard LPCVD processes can be run on fused silica substrates because of its high softening temperature of $T^{(\text{soft})} = 1600\text{ °C}$. These LPCVD processes guaranty, compared to PECVD and PVD layers, a good uniformity, a high electrical and mechanical quality, a very good step coverage, and a tight thickness control [Sto96a].
- The stress control of LPCVD layers is improved. Beside tight margins for film thickness deviations a precise and reproducible control of the film stress is a major fabrication concern. The adoption of fused silica substrates raises the thermal film stress component of common LPCVD layers (see Section 2.2 for more information). The thermal component of the stress is of higher reproducibility and therefore lowers the overall impact of the intrinsic stress deviations. That is, the stress homogeneity of depositions is generally increased.
- The choice of possible materials for the fabrication of free-standing structures is wide. Fused silica substrates with their low TEC lead to tensile stress of layers which have compressive stress on silicon and which are accordingly not often used in surface-micromachining. Oxides can be deposited with tensile stress at high temperatures (e.g. from a TEOS source, tetra-ethyl-ortho-silicate) or as low-temperature oxide (LTO e.g. from a DES source, di-ethyl-silane). Also crystalline deposited poly-silicon, no matter if large or small grained, has tensile stress.¹¹

¹⁰ Technical data about fused silica can be found e.g. at [Sch07] and [Pho07]

¹¹ The selected transducer material of this work is in-situ boron-doped poly-silicon having a high compressive stress on silicon.

- Fused silica has a lower absorbance in the UV range. This is advantageous if (bulk or surface micromachined) structures need to be fabricated on transparent substrates either for optical sample analysis or for optical switches in transmission as demonstrated by [Pan05] or [Kni06]. There are also a couple of very simple advantages of transparent substrates when it comes to optical inspection during fabrication, assembly and operation.
- Besides its transparency fused silica substrates do not fluoresce like e.g. *Pyrex*[®]. This property becomes important if fluorescent samples need to be analyzed like the case in many micro-fluidic bio-medical applications. In addition, the chemical inertness of fused silica (silicon dioxide) is advantageous for the latter kind of application because the fluid channel crafted into the bulk do not need an additional coating.
- Fused silica offers good thermal insulation properties having a thermal conductivity of approximately 1/100th the conductivity of single crystalline silicon. This is advantageous if thermal actuators or sensors are developed as described in [Buc06]. The commonly adopted thermal insulation of the transducer structures on flexible and fragile membranes could be replaced by the rigid silica bulk material resulting in a robust sensor design.

Besides these advantages there are some serious drawbacks to be considered:

drawbacks of
silica substrates

- In comparison to fabrication on silicon the film stresses of deposited layers are shifted towards higher tensile levels. This increase is due to the low TEC of fused silica and thickness limits exist to avoid cracks. Advantageous are layouts with rounded corners to prevent stress concentrations.
- An important issue is the possible plastic deformation of the substrates occurring during long-term annealing at temperatures above 800 °C. The high softening temperature of 1600 °C indicates the temperature at which the substrate deforms under its own weight. However, if layers are deposited onto the substrate, which pose a stress on it, plastic deformation of the bulk may occur already at lower temperatures.¹²
- Only few bulk-micromachining processes are available for fused silica. Deep reactive ion etching requires special equipment to increase the etch rate and the selection of mask material becomes difficult. Also the convenient anisotropic wet etch to form geometrically well defined cavities is not available and the choice of mask material becomes again difficult if deep isotropic wet etching of the bulk is performed.
- Some issues exist during lithographic pattern transfer. LPCVD layers on the substrate have commonly a high tensile stress leading to wafer curvature and alignment difficulties. Even if all layers remain symmetrically on both sides of the substrate and no curvature can be observed, the film stress leads to lateral displacement resulting in concentric shift of the alignment keys. Finally, automatic wafer-aligners may have troubles with the transparency of the substrate.

¹² Information on viscose deformation of oxide can be found in [Fit89] and [Car02]. The viscosity of fused silica at $T^{(\text{strain})} = 980 \text{ }^\circ\text{C}$ is approx. $31.6 \times 10^{12} \text{ Pa s}$ (see Tab.2.2).

- From a mechanical point of view the amorphous bulk material is less attractive than single crystal silicon. All transducers, either fabricated on the substrate or made out of the bulk itself, are of lower mechanical quality and creep, plastic deformation and a lower yield strength have to be expected.
- Identical film stress levels on silica lead to generally larger deformation on silica than on silicon. This is due to the fact that the *Young's* modulus of silica is roughly half the modulus of silicon.
- Fused silica is more brittle in comparison to silicon. This has consequences for the practical substrate thicknesses during processing and for wafer dicing. Sawing of silica leads to a faster degradation of the dicing blade, the trenches are wider and chipping on the edges is more distinct. Also adhesion on the dicing tape is an issue due to higher forces during the dicing procedure.

This section concludes the argumentation on special choice of substrate material. Besides the expected technological constraints, silica was finally chosen and the following sections will focus on the encountered technological consequences.

2.2 Film stress on fused silica

All layers, no matter if chemical or physical vapor deposited, or electroplated are under stress after deposition. The adjustment of film stress is a general issue during mechanical transducer fabrication. Especially, the control of the film stress on fused silica is a major challenge, but can turn into a benefit at the same time. For this reason the following section will provide some details about stress on silica and the stress measurement techniques employed during this work.

The stress of any deposited layer is the sum of a thermal σ_t and an intrinsic stress component σ_i

$$\sigma = \sigma_t + \sigma_i. \quad (2.1)$$

σ_i is related to the layer composition and can vary strongly depending on the deposition parameters. It is especially difficult to achieve a good uniformity of σ_i over the boat during the growth of in-situ boron-doped poly silicon and low-stress nitride. In contrast σ_t depends solely on the mismatch of the thermal expansion coefficients of film and substrate α_F and α_S , respectively. In most cases, α_S of the substrate is well known and α_F of the film changes little compared to the variations of σ_i . The application of fused silica as substrate material is suggested in this thesis. Its low TEC of approximately $0.5 \times 10^{-6} \text{ K}^{-1}$ increases σ_t of all standard layers in comparison to a deposition on silicon, which has a TEC of $2.616 \times 10^{-6} \text{ K}^{-1}$. As consequence, the impact of σ_t on the film stress is increased and stress is rendered more reproducible and homogeneous over the reactor load during LPCVD processing (see Section 2.3.1 for an example). The next sections will be concerned with measurement, interpretation, and adjustment of film stress on fused silica.

2.2.1 Stress measurement by means of wafer curvature

Wafer curvature measurements were performed by using a *Eichhorn and Hausmann MX203 Wafer Geometry Gauge* which employs a capacitive detection principle. The technique is based on *Stoney's* equation and enables the measurement of tensile and compressive film stress. *Stoney's* equation relates the change of wafer curvature, to the stress exerted by a thin film on the surface of the substrate. The curvature K , more precisely the change of curvature, can be expressed in terms of initial, i.e. unstressed, radius of curvature r_0 and the radius in the stressed state r . Important to note is, that the calculation does not require the knowledge of the film's mechanical properties. Only the thickness of the layer and the mechanical properties of the substrate must be provided as input:

Stoney's
equation

$$\sigma_F = \frac{E_S' t_S^2}{6 t_F} K \quad \text{with } K = \left(\frac{1}{r_0} - \frac{1}{r} \right) \quad (2.2)$$

Substrate thickness t_S and the radii of curvatures are measured capacitively. The achievable accuracy depends on four parameters: accurate knowledge of the layer thickness t_F , accurate knowledge of the mechanical properties of the substrate, i.e. its biaxial-modulus $E_S' = E_S/(1 - \nu_S)$. Furthermore, the equation's accuracy depends on the ratio of thicknesses $\delta = t_F/t_S$, and the ratio of the elastic moduli of deposit and substrate $\xi = E_F'/E_S'$. The impact of the latter ratios on the approximative formula was analyzed by [Kle00] showing that the systematic error of *Stoney's* approximation can be expressed as

accuracy of
Stoney's equation

$$\epsilon_{St} = \delta \frac{1 - \xi \delta^2}{1 + \xi \delta^3}. \quad (2.3)$$

This error is below 1% for all the deposited layers of this work and is not of special concern. However, it may become relevant if thinned substrates are used or if very thick layers are deposited. For these case, an extension of *Stoney's* equation is presented in Appendix B.1.3.

In course of this work, major problems were related to the required accurate knowledge of the layer thicknesses, which, especially in the case of poly-silicon, could only be measured with an estimated error of approximately $\pm(5 - 10)\%$. A *Zeiss MCS400* spectroscopic interferometer, a *PLASMOS SD2300* monochromatic ellipsometer (wave length: 632.8 nm), and a *Tencor Instruments alpha-step 200* surface profiler were available for thickness measurement. The interferometer requires the optical properties as input which could not be updated frequently. These properties deviate due to process changes and result in a thickness uncertainty of up to $\pm 10\%$. The expected deviation is based on spectroscopic ellipsometry measurements of some LPCVD film samples with a *Woollam M2000*. These indicate a process dependent change of the refractive index of $\pm 5\%$ for in situ boron-doped and $\pm 10\%$ for non-doped poly silicon. As a result, besides the systematic error of ϵ_{St} an additive uncertainty of up to $\pm(5 - 10)\%$ must be expected due to the error in t_F .

error caused by
film thickness
measurement

For practical purposes *Stoney's* equation can be re-written expressing the stress in terms of the commonly measured wafer bow, i.e. wafer deflection h_b at the substrate

wafer bow center. If radius of curvature r is much larger than the substrate's diameter d_S , the wafer bow can be approximated by $h_b = d_S^2/8r$ [Fli01] and with (2.2) the stress can be expressed as

$$\sigma_F = \frac{E_S' t_S^2}{3 t_F} \frac{4(h_{b0} - h_b)}{d_S^2}. \quad (2.4)$$

The measured change of wafer deflection due to the stress exerted by the layer under test is denoted by $(h_{b0} - h_b)$. The expected error is the sum of the systematic error caused by *Stoney's* approximation and statistic measurement deviations

$$\frac{\Delta\sigma_F}{\sigma_F} = \epsilon_{St} \pm \sqrt{\left[\frac{\Delta t_F}{t_F}\right]^2 + \left[\frac{\Delta h_b}{h_b}\right]^2 + \left[\frac{2\Delta t_S}{t_S}\right]^2} \quad (2.5)$$

where substrate thickness measurement errors can be neglected for most practical cases being smaller 1%.

An in situ boron-doped poly-silicon layer is considered as example. It is assumed to have a total stress of 200 MPa and a thickness of $t_F = 500$ nm. This layer would cause a change of bow of $16.6 \mu\text{m}$ on a 10 cm silicon substrate with (100) orientation¹³ and a bow change of $34.6 \mu\text{m}$ on a silica substrate of identical diameter. As consequence, the errors equate to

$$\epsilon_{Si} \approx \pm \left(0.01 + \sqrt{\left[\frac{25 \text{ nm}}{500 \text{ nm}}\right]^2 + \left[\frac{1 \mu\text{m}}{16.6 \mu\text{m}} + 0.01\right]^2} \right) \times 100 \% = \pm 10 \%$$

$$\epsilon_{FS} \approx \pm \left(0.01 + \sqrt{\left[\frac{25 \text{ nm}}{500 \text{ nm}}\right]^2 + \left[\frac{1 \mu\text{m}}{34.6 \mu\text{m}} + 0.01\right]^2} \right) \times 100 \% = \pm 7 \%$$

with a reproducibility of the *MX203* gauge equal to $\pm 1 \mu\text{m}$ for h_b plus additional 1% of the reading.¹⁴ It can be noted, that fused silica leads to a higher accuracy caused by the lower modulus of the material (see Tab. B.1) and the therefore larger wafer bow.

An additional difficulty poses the non-conductive fused-silica substrate. The capacitive measurement principle requires a conductive bulk and the silica wafers need to be coated with a thin conductive layer which does not interfere with the deposition of the layer under test and all required subsequent annealing steps.¹⁵

The possibility to measure the stress of layers with unknown mechanical proper-

¹³ It is important to note the invariance of the biaxial modulus E_S' for arbitrary directions of the {100} and {111} planes in crystals with a cubic lattice [Bra73] (although E and ν itself change within the {100} planes [Wor65]). This requires the use of (111) or (100) wafers for curvature measurement whereas the latter one should be preferred for its lower modulus.

¹⁴ It must be noted that the reproducibility determines the overall accuracy of the stress measurement because the stress always results from the difference of two readings. The absolute accuracy of the curvature measured with a *MX203* is worse ($\pm 5 \mu\text{m}$ plus additional 1% of the reading).

¹⁵ For this work, the silica substrates were pre-coated with a 100 nm in-situ boron-doped poly-silicon layer which was annealed asymptotically for 12 h@800 °C. A 100 nm low-stress nitride layer (Nit-D20) acted as

exemplary calculation of measurement error

capacitive curvature measurements on silica

advantages wafer curvature

ties or even layer stacks is an advantage of wafer curvature based measurements. Furthermore, many stress values can be sampled successively from a single sample during an interrupted annealing procedure to analyze the stress evolution of the material under test.

2.2.2 Thermal stress and viscous deformation

The thermal expansion ε and TEC α of silicon and fused silica can be approximated with the polynomials

$$\varepsilon = \frac{\Delta L}{L_0} = \sum_{i=0}^3 \varepsilon_i T^i, \quad \alpha = \frac{d\varepsilon}{dT} = \sum_{i=0}^2 \alpha_i T^i \quad [T] = \text{°C}. \quad (2.6)$$

The actual coefficients ε_i and α_i are given in Tab. B.2 and Tab. B.3. They correspond to curve fits of the data presented in [Tou77] and [Oka84].¹⁶ For comparison, discrete data of the substrates used in course of this work (*Lithosil Q1*[®], see [Sch07]) as well as thermal strain calculated with (2.6) are depicted in Fig. 2.2.

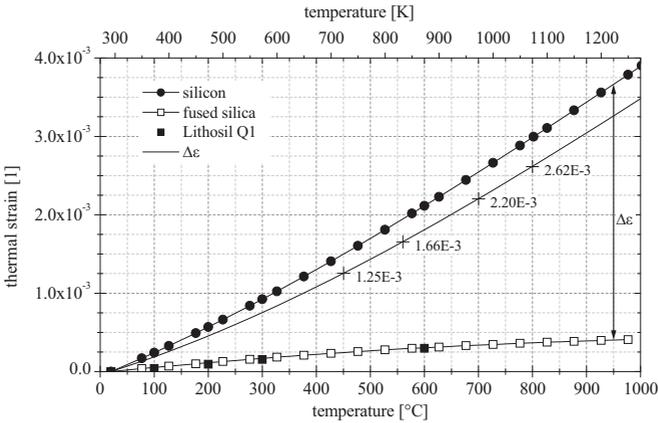


Fig. 2.2: Thermal strain of silicon and fused silica according to data of [Sch07], [Oka84] and [Tou77]. Full lines represent the result of interpolation (2.6) and the coefficients summarized in Tab. B.2.

Thermal strain of film and substrate are defined as the integral over their TEC α

protection layer between conductive coating and deposit under test.

¹⁶ Precaution is necessary if literature values are used for stress calculation on fused silica because the thermal material properties depend on the substrate's fabrication process and can deviate considerably.

from deposition temperature T_d to temperature T

$$\varepsilon = \int_{T_d}^T \alpha \, dT = \bar{\alpha}(T - T_d). \quad (2.7)$$

$\bar{\alpha}$ denotes the average TEC which is only valid for a specific temperature range. The thermal stress in (2.1) at temperature T can be calculated if the biaxial modulus of the film E_F' and the thermal expansion of film and substrate ($\varepsilon_F, \varepsilon_S$) are known

$$\sigma_t = E_F' \int_{T_d}^T [\alpha_F - \alpha_S] \, dT \quad (2.8)$$

$$\sigma_t = E_F' \left(\varepsilon_F(T) - \varepsilon_F(T_d) - [\varepsilon_S(T) - \varepsilon_S(T_d)] \right). \quad (2.9)$$

It is more appropriate to use the difference of elongations rather than the difference of TECs to calculate σ_t of LPCVD layers because the TECs commonly change significantly within the relevant temperature range up to 1000 °C. The formula

$$\sigma_t \approx E_F' (\alpha_F - \alpha_S)(T - T_d)$$

represents only a rough approximation if the room-temperature TECs are used. This becomes apparent if the 40 % change of α_{FS} is considered within the temperature range of 20 °C–500 °C and the 60 % alteration within the range of 20 °C–800 °C. Silicon shows an even stronger change of 60 % and 70 % for the same temperature ranges. Linear σ_t versus T plots, as reported by many researchers (see e.g. [Ret80], [Smo85], or [Sin78]), are misleading in implying a constant TEC of the layer but in fact the difference $\alpha_S - \alpha_F$ must be constant to yield a linear σ_t and this is remarkable if the strong TEC changes in α_S are considered.

The positive difference between the thermal strain of silicon and silica (see $\Delta\varepsilon$ illustrated in Fig. 2.2) leads to a positive shift of the thermal layer stress of deposits on silica in comparison to their formation on silicon. This increase can be calculated with (2.9)

$$\Delta\sigma_t = \sigma_{t(FS)} - \sigma_{t(Si)} = E_F' (\varepsilon_{FS} - \varepsilon_{Si}) = E_F' \Delta\varepsilon \quad (2.10)$$

where $\sigma_{t(Si)}$ and $\sigma_{t(FS)}$ denote the thermal stress on silicon and fused silica. Therefore, $\Delta\sigma_t$ increases monotonously with $\Delta\varepsilon$ as deposition temperature increases and the impact of $\Delta\varepsilon$ is scaled by the biaxial modulus of the deposit. The measured shifts in σ_t on fused silica as well as the related thermal strain are illustrated in Fig. 2.3. It can be observed that layer stress increases by roughly 800 MPa and 350 MPa for silicon nitride and poly-silicon, respectively. As-deposited CVD oxides show a comparably small increase in thermal stress of approximately 55 MPa which rises during anneal proportional to the chosen temperature T_a , i.e. $\Delta\sigma_{t(\text{oxide})}$ is proportional to

temperature de-
pendency of TEC

increased thermal
stress on silica

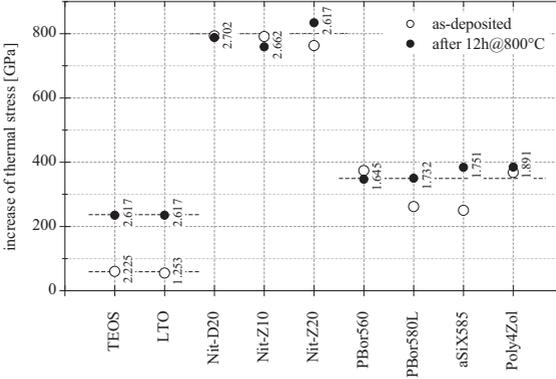


Fig. 2.3: Increase of thermal stress $\Delta\sigma_t$ of CVD deposits on fused silica in comparison to their formation on silicon due to the difference in thermal elongation $\Delta\varepsilon$ (corresponding values for $\Delta\varepsilon \times 10^3$ are given at each data point). CVD oxides show a shift of $\Delta\sigma_t$ proportional to the annealing temperature due to viscous deformation.

$\Delta\varepsilon$ at T_a . The latter change is related to viscous deformation of deposited silicon oxide at higher temperatures as e.g. reported by [Fit89] and [Car02].

Viscous deformation of silicon oxide may also be an issue for the fused silica substrates itself. The viscous relaxation of silicon oxide was modeled by [Ire82] (see also [Kob88] [Fit89]). The strain rate $\dot{\varepsilon}$ is proportional to the difference of actual stress σ and asymptotically approached stress σ_∞ at $t \rightarrow \infty$. Furthermore, strain rate scales inversely with viscosity η yielding

$$\dot{\varepsilon} = \frac{1}{G} \dot{\sigma} = \frac{1}{\eta} (\sigma_\infty - \sigma) \quad (2.11)$$

$$\dot{\sigma} = \frac{G}{\eta} (\sigma_\infty - \sigma) = \frac{\sigma_\infty - \sigma}{\tau} \quad \text{with } \tau = \frac{\eta}{G}, \quad (2.12)$$

where τ represents a viscous relaxation time scale. While shear modulus $G = E/2(1+\nu)$ depends only weakly on temperature, the viscosity obeys an exponential Arrhenius law with a minimum viscosity η_0 and an empiric activation energy E_η

$$\eta = \eta_0 \exp[E_\eta/kT]. \quad (2.13)$$

Differential equation (2.12) is solved with an exponential function. Initial stress σ_0 relieves completely ($\sigma_\infty = 0$) within a time scaled by τ due to viscous flow

$$\sigma = \sigma_0 \exp[-t/\tau]. \quad (2.14)$$

Viscosity data of the substrate material used in the present work can be found in [Sch07]. Values for thermal oxide and LPCVD nitride are taken from [Car02]. All

viscous
deformation
of bulk silica

viscosity data is summarized in Fig. 2.4 together with the exponential fitting parameters for (2.13). Actual values for the viscous time τ can be found in Tab. 2.3. These values were calculated based on the material parameters presented in Fig. 2.6(b). It must be noted from the results presented in Tab. 2.3 that the relaxation time of 1.9 h for CVD oxide agrees well with the observed almost complete relaxation of TEOS and LTO during a 12 h anneal at 800 °C (see Fig. 2.6). It must be further noted that all long-time anneals on fused silica should be restricted to temperatures below 800 °C. This thermal limit for fused silica substrates is in agreement with the work of [Car02] and [Ret80]. On the other hand, the data of Tab. 2.3 shows that fused silica as well as oxide and nitride are well suited for applications with typical operation temperatures below 200 °C. Standard qualification procedures e.g. for the assessment of the high-temperature lifetime (1000 h@150 °C) will not lead to a detectable change of layer stress due to viscous deformation of the silica substrate.

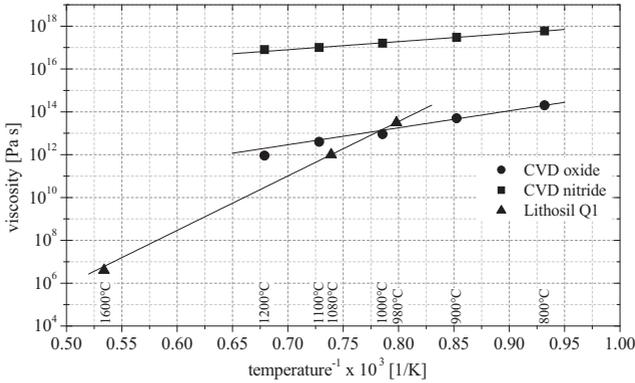


Fig. 2.4: Viscosity versus temperature of fused silica, CVD oxide, and CVD nitride. The full lines represent fits to (2.13) (CVD oxide: $\eta_0 = 8.224 \times 10^6$ Pa s, $E_\eta = 2.520 \times 10^{-19}$ J; fused silica (Lithosil Q1[®]): $\eta_0 = 1.604 \times 10^{-7}$ Pa s, $E_\eta = 8.084 \times 10^{-19}$ J; CVD nitride: $\eta_0 = 1.808 \times 10^{14}$ Pa s, $E_\eta = 1.201 \times 10^{-19}$ J).

viscous relaxation
during anneal

The magnitude of viscous deformation is proportional to the stress of the layer as can be seen from (2.14). Similarly, this consideration holds for the possible viscous deformation of the substrate due to stress induced by a deposit. Although small in magnitude,¹⁷ the stress level within the silica bulk is proportional to the layer stress. It follows that a stress relieve within the substrate leads to a relaxation of the layer's stress of the same percentage. It must be noted that the actual possible maximum change of layer stress due to substrate deformation $\Delta\sigma$ is equal to the total stress σ_a of the deposit at annealing temperature T_a for layers which *do not* deform viscously

¹⁷ The maximum stress, occurring at the substrate surface, evaluates with (B.1.4) to $\sigma < 1$ MPa for Nit-Z20.

by themselves. σ_a can be calculated with (2.9) and (2.6). By applying (2.14) we find

$$\Delta\sigma = \sigma_a - \sigma_{a_0} = \sigma_{a_0} \left(\exp[-t/\tau] - 1 \right) \tag{2.15}$$

where σ_{a_0} denotes the initial total stress at T_a .

Layers with a relaxation time well below that of the substrate will relax completely faster than substrate. They will show a stress after complete relaxation which composes solely of the thermal component equal to $E_F' \Delta\epsilon$. This is expected to be the case for CVD oxides as well as for amorphous silicon like aSiX585. For these layers an almost complete relaxation will take place for sufficiently high thermal budgets.¹⁸ The resulting stress in the case of amorphous silicon would be approximately 490 MPa and 570 MPa for 800 °C and 900 °C, respectively.

relaxation
CVD layers

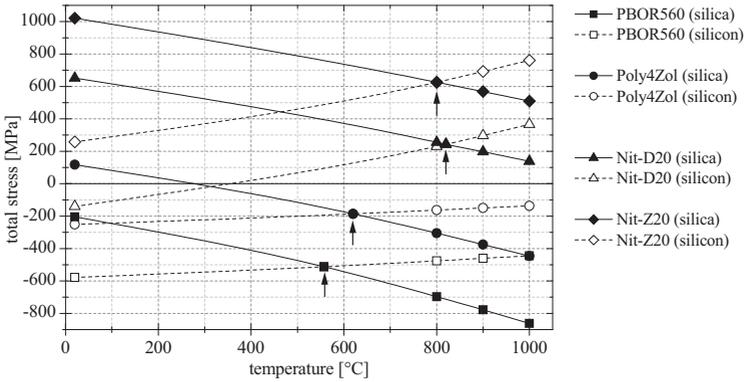


Fig. 2.5: Total stress of poly-silicon and low-stress nitride deposits on fused silica versus temperature (the poly-silicon layers were deposited on intermediate nitride layers). The individual stress at deposition temperature is indicated by arrows.

Some information about the thermal expansion of the deposits under test is necessary to deduce the magnitude of σ_a from room temperature stress data, i.e. to separate the intrinsic from the total stress. A mean $\bar{\alpha}_{SiN}$ of $2.21 \times 10^{-6} / K$ [Toi03] and an expansion for poly-silicon which is 15 % smaller than that of single crystal silicon was assumed for the illustrative comparison presented in Tab. 2.4. The chosen value for the expansion of poly-silicon agrees with the observations reported by other researches giving a TEC range of $0.75 \dots 0.85 \times \alpha_{Si}$ [Vol93][Suz77][Mur82][Elb98].¹⁹ The prediction of substrate deformation due to strained poly-silicon layers is further complicated by recrystallization during anneal. This morphological change reduces the intrinsic stress component of the layer. As consequence, the total stress σ_a during anneal decreases and similarly does the magnitude of plastic substrate deformation.

stress at annealing
temperature

change of layer
morphology

¹⁸ Information on the viscosity of amorphous silicon can e.g. be found in [Wit93] or [Vol93].

¹⁹ There are also a smaller number of literature sources which state a larger TEC like e.g. [Sha01].

The occurrence of the recrystallization was neglected during calculation of the data given in Tab. 2.4, therefore, the stated magnitudes represent an estimate of the maximum.²⁰

general trend of
stress change

From the data given in Tab. 2.4 can be concluded, that anneals below 800 °C do not cause a markedly deformation of the silica substrate. The amorphous oxide substrate can be regarded thermally stable below this temperature for common annealing durations. This changes already at a moderate 1 h anneal at 900 °C which might lead to considerable stress changes of the order of 100 MPa for the exemplary case of an in situ boron-doped poly-silicon layer (see Tab.2.4). It must be noted that the change of layer stress due to viscous flow of the substrate has a negative sign for nitride, but a positive for poly-silicon layers. This reflects the stress state of the layer at annealing temperature because the viscous flow always tends to relieve the actual stress. An illustrative comparison of layer stresses on silicon and silica versus temperature is depicted in Fig. 2.5. It can be seen, that for all applicable temperatures T_a the low-stress nitride remain tensile whereas the poly-crystalline silicon layers stay compressive *during* anneal. Extra data markers have been added indicating the individual deposition temperatures and the corresponding stress which is equal to the intrinsic stress of the deposit. The slopes of the deposits depicted in Fig. 2.5 change their sign if formations on silicon and silica are compared. This is typical for the majority of CVD deposits which have an thermal expansion with a magnitude in between that of silica and silicon.

real life
application

Although Tab. 2.4 and Tab. 2.3 highlight the problem of viscous relaxation, the prediction of actual stress shifts due to the viscous substrate is more difficult in practice. MEMS processes result in patterned layer stacks and their deformation is always proportional to the *local* stress within the substrate. Finally, any intermediate oxide layer requires extra consideration especially in the case of CVD oxide because they might act as a floating support during anneal and might change the resulting layer stress significantly (see next section for the discussion of an example). Also the simple model of viscous flow presented above may need to be modified as discussed in [Kob88].

²⁰ The assumption of a constant intrinsic stress is a good approximation at least for PBOR560 and moderate temperatures. Its composition does not change reasonably at 800 °C as further elaborated in Section 2.3.1 and Section 2.3.1.

Table 2.3: Viscous relaxation time τ for fused silica, CVD oxide, and nitride. The calculated values are based on the viscosity data given in Fig. 2.4, the mechanical properties summarized in Fig. 2.6(b), and equations (2.13) and (2.14). G denotes the shear modulus equivalent to $E/2(1 + \nu)$.

temperature	CVD oxide ($G = 28.7$ GPa)		fused silica ($G = 30.8$ GPa)		CVD nitride ($G = 95.6$ GPa)	
	η [Pa s]	τ	η [Pa s]	τ	η [Pa s]	τ
200 °C	4.7×10^{23}	4.5×10^9 h	9.2×10^{46}	8.3×10^{32} h	1.7×10^{22}	3.1×10^9 h
800 °C	2.0×10^{14}	1.9 h	8.0×10^{16}	723.5 h	6.0×10^{17}	1740.5 h
900 °C	4.7×10^{13}	27.3 min	7.6×10^{14}	6.9 h	3.0×10^{17}	872.1 h
1000 °C	3.0×10^{12}	1.8 min	1.5×10^{13}	8.2 min	1.7×10^{17}	487.1 h
1200 °C	5.3×10^{11}	18.5 sec	2.9×10^{10}	1.0 sec	6.6×10^{16}	192.6 h

Table 2.4: Summary of stress relaxation $\Delta\sigma$ during anneal due to viscous deformation of fused silica as well as total layer stress at annealing temperature σ_a . The magnitude of $\Delta\sigma$ (2.15) is proportional to σ_a . σ_t represents the thermal stress of the deposit on fused silica.

layer	stress at 20 °C			anneal 12 h@800 °C			anneal 1 h@900 °C			anneal 1 h@1000 °C		
	σ_t [MPa]	σ_a [MPa]	$\Delta\sigma$ [MPa]	$\Delta\sigma$ [MPa]	σ_a [MPa]	$\Delta\sigma$ [MPa]	$\Delta\sigma$ [MPa]	σ_a [MPa]	$\Delta\sigma$ [MPa]	$\Delta\sigma$ [MPa]	σ_a [MPa]	$\Delta\sigma$ [MPa]
Nit-D20 ^a	243	409	-4	-4	255	-27	197	138	-138	138	138	-138
Nit-Z20	626	395	-10	-10	626	-77	568	-509	509	509	509	-509
PBOR560 ^b	-512	308	11	11	-697	105	-778	861	-862	861	861	-862
Poly4Zol	-186	303	5	5	-305	51	-375	446	-446	446	446	-446

^a The TEC of silicon-rich nitride is approximated with $\alpha_{\text{SiN}} = 2.21 \times 10^{-6}$ /K given for the ranges of 25 °C–400 °C by [Tol03].

^b Poly-silicon is assume to expand 15 % less than single crystal silicon which leads to a $\sigma_t(\text{Si})$ of -65 MPa at 20 °C.

2.2.3 Young's and biaxial moduli

Stress measurement by means of wafer curvature, as described in Section 2.2.1, is independent of the film's *Young's* modulus and *Poisson's* number. These mechanical film properties are required if MEMS structures are to be modeled or if the separation of intrinsic and thermal stress component is required. Mechanical properties of thin-film functional layers depend on process conditions and are often not well known. A simple means to calculate the biaxial modulus $E_F' = E_F/(1 - \nu_S)$ from wafer curvature readings is therefore described in this section. The presented technique is based on simultaneous film deposited on two different substrate materials with well known thermal expansions like e.g. silicon and fused silica.²¹

Subtracting the film stress given by (2.9) for silicon σ_{Si} from the value on fused silica σ_{FS} yields

$$\sigma_{Si} - \sigma_{FS} = E_F'[\varepsilon_{FS} - \varepsilon_{Si}]. \quad (2.16)$$

The unknown intrinsic stress σ_i and the thermal elongation of the deposited film ε_F are canceled out. The assumption of identical intrinsic stress and elongation holds as long as the film growth conditions are identical, i.e. the layer on which the film is processed and the deposition conditions are identical. Therefore, an intermediate layer is required which needs to be deposited prior to the film of interest. A sandwich of a conductive poly-crystalline silicon layer covered by an amorphous low-stress nitride layer facilitates a later capacitive curvature measurement and was used in this work.

The desired mechanical properties can be obtained from (2.16):

$$E_F' = \frac{\sigma_{Si} - \sigma_{FS}}{\varepsilon_{FS} - \varepsilon_{Si}}. \quad (2.17)$$

ν_F might be extracted in a further step by proceeding in the same manner as described above, but by sampling the stress readings simultaneously from indicators as presented in Section 2.2.4 and Appendix B.1.5. The deflection of the micromachined indicators depend only on the *Young's* modulus and (2.17) changes to

$$E_F = \frac{\sigma_{Si} - \sigma_{FS}}{\varepsilon_{FS} - \varepsilon_{Si}}. \quad (2.18)$$

It is straightforward to calculate ν_F from (2.17) and (2.18), but it must be considered that the layer under test needs to be deposited on the same surface to cancel out the impact of different growth conditions. This may lead to difficulties because a selective sacrificial etch is required to release surface micromachined indicator struc-

²¹ The approach is similar to the one discussed in [Thu04]. They measured the change of film stress during heat-up of the samples to calculate the mechanical properties and TEC of the film under test. This method can be either used for a CVD layer or any other PVD film. The technique described here requires the deposition at higher temperatures and is consequently limited to pyrolytically deposited films. However, it has the advantage of only requiring a standard wafer geometry gauge which is not necessarily equipped with a heating stage.

biaxial
modulus

Young's
modulus

tures,²²

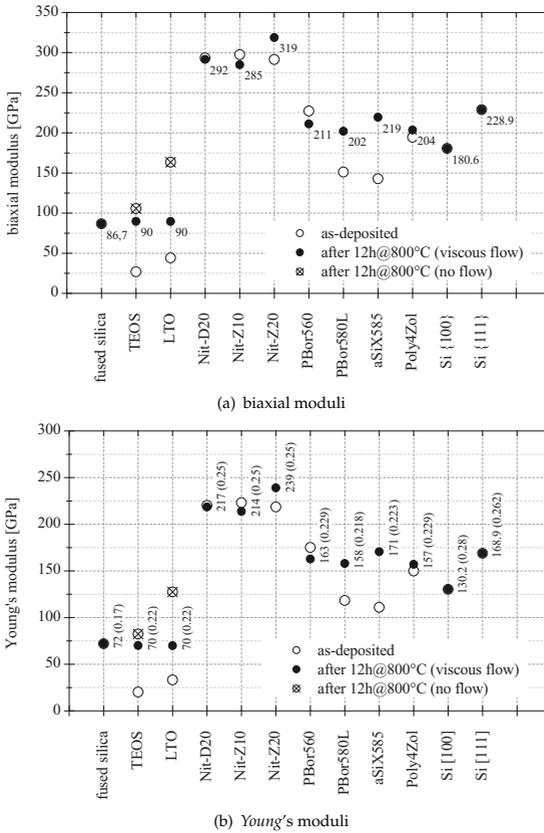


Fig. 2.6: Calculated biaxial and *Young's* moduli of various as-deposited LPCVD layers and after a 12 h anneal at 800 °C in N₂ atmosphere. The moduli of silicon (<001> direction) and silica are also added for the purpose of comparison. (*Poisson's* number is assumed to be constant during anneal and the assumed values are given in parentheses.)

The presented approach to measure the biaxial moduli is justified by its simplicity, but the results must be interpreted carefully with the error related to this technique in mind:

measurement error

²² Oxides should also be avoided as base layer because of their influence on the growth of poly-silicon and their viscous deformation during anneal. The stress of layers grown on oxide and nitride differ drastically (see results in Section 2.3.1).

$$\frac{\Delta E_F'}{E_F'} = \sqrt{\frac{\Delta\sigma_{Si}^2 + \Delta\sigma_{FS}^2}{(\sigma_{Si} - \sigma_{FS})^2}}. \quad (2.19)$$

This error gets more illustrative if the stress difference is substituted by (2.17)

$$\frac{\Delta E_F'}{E_F'} = \frac{\sqrt{\Delta\sigma_{Si}^2 + \Delta\sigma_{FS}^2}}{E_F'(\varepsilon_{FS} - \varepsilon_{Si})}. \quad (2.20)$$

That is, the results will be more accurate the stiffer the film is and the higher the deposition temperature is chosen increasing $\Delta\varepsilon$. This renders the approach applicable for LPCVD layers like poly-silicon and nitride, but suggests to treat results e.g. for oxides with care. The stress data is acquired by means of wafer curvature measurement with the errors $\Delta\sigma_{Si}$ and $\Delta\sigma_{FS}$ given by (2.5).

Results acquired by following the described procedure are presented in Fig. 2.6 (corresponding stress data is summarized in Tab. B.9 of Appendix B.1.7). Literature values for *Poisson's* number were taken to estimate the corresponding *Young's* from the measured biaxial moduli (TEOS: [Car02]; poly-silicon: [Elb98], low-stress nitride: [MS95]). The selection of a proper *Poisson's* number for poly-silicon followed the expected textures²³ and is further discussed in Section 2.3.1 and Section 2.3.1. The results after anneal are in good agreement with reported literature values²⁴ and are for this reason taken for all subsequent calculations. Viscous deformation of the substrate material in course of the deposition and annealing procedure can be neglected (see discussion in Section 2.2.2). Therefore, markedly changes in moduli value indicate a distinct change of layer morphology. This is the case for CVD oxides and semi-crystalline poly-silicon (aSiX585 and PBOR580L). In these cases the layer structures change from a softish and less dense state to a stiffer compact structure.

2.2.4 Stress measurement by means of indicator structures

Stress measurement with surface-micromachined indicators as described in [Sto96] and [Elb98] were performed. Their geometry is depicted in Fig. 2.7. The dry-etched structures are released during a sacrificial layer etch and displace proportional to the layers stress. The actual indicator displacement, measured as sprocket count N_S , is a function of the film's stress and modulus E_F . A formula for the layer stress is obtained by basic algebraic manipulation of (B.10):

$$\sigma_F = \frac{E_F}{S_i C_H} N_S. \quad (2.21)$$

S_i represents the indicator geometry and C_H the impact of the hinge deformation on the stress reading (values for S_i and C_H can be found in Tab. B.6 and Tab. B.5). The hinges are small beams which have a geometrical moment of inertia proportional to W_H^3 , where W_H denotes the hinge's width. It follows that the correction coefficient

impact of the
hinge geometry

²³ <111> for re-crystallized layers and <110> for crystalline grown deposits [Bis86] [Jou89]

²⁴ Literature sources providing data about mechanical properties of thin-films are e.g. [MS95](nitride), [MS95](poly), [Lee98](α -Si), or [Car02](TEOS).

C_H can be expressed as a function being proportional to W_H^3 . By following this consideration, the error of (2.21) equates to

$$\frac{\Delta\sigma_F}{\sigma_F} \approx \pm \sqrt{\left[\frac{\Delta N_S}{N_S}\right]^2 + \left[\frac{\Delta E_F}{E_F}\right]^2 + \left[-\frac{3\Delta W_H}{W_H}\right]^2}. \quad (2.22)$$

It becomes obvious that small changes in the hinge geometry have a huge impact on the indicated stress value.

As example, an in situ boron-doped poly-silicon layer with a modulus of $E_F = 155$ GPa is considered. The given modulus was calculated according to the technique described in Section 2.2.3, which results in estimated modulus error of about $\Delta E_F = 7.75$ GPa caused by erroneous curvature readings (see Section 2.2.1). An assumed stress of 200 MPa results in a deflection of $N_S = 6.32$ and 2.96 sprockets for indicator geometries k and n, respectively (see Appendix B.1.5 for geometry data). The indicator's nonius limits deflection miss-readings ΔN_S to about one tenth sprocket, which is negligible in comparison to the impact of lithography and dry-etching. These pattern transfer deviations must be expected to be about $\Delta W_H = 0.25 \mu\text{m}$. Consequently, the overall error of indicator geometries k and n equate to:

$$\epsilon_k \approx \pm \sqrt{\left[\frac{0.1}{6.32}\right]^2 + \left[\frac{7.75 \text{ GPa}}{155 \text{ GPa}}\right]^2 + \left[\frac{3 \times 0.25 \mu\text{m}}{3 \mu\text{m}}\right]^2} \times 100 \% = \pm 26 \%$$

$$\epsilon_n \approx \pm \sqrt{\left[\frac{0.1}{2.96}\right]^2 + \left[\frac{7.75 \text{ GPa}}{155 \text{ GPa}}\right]^2 + \left[\frac{3 \times 0.25 \mu\text{m}}{5 \mu\text{m}}\right]^2} \times 100 \% = \pm 16 \%$$

In contrast to wafer curvature measurements, the stress detection with pointer structures do not require the knowledge of the film thickness, but the stress calculation with formula (B.10) depends on *Young's* modulus only.²⁵ This is advantageous because film thickness measurement errors do not influence the stress reading. However, the modulus of the film is still required and introduces an error. Major benefit of surface micromachined indicators is the possibility to measure the stress of a film which is deposited on the same sacrificial layer, patterned and attached to the substrate in the same way as the actual sensor structures. The as-deposited properties of the functional layer and their evolution change with the kind of implemented sacrificial layer, more precisely the surface properties of the sacrificial layer. Therefore, the results obtained with indicators are as close to the real sensor structure as possible. An example for this can be found below by comparing e.g. Fig. 2.9(b) and Fig. 2.14 which depict stress of poly-silicon on TEOS and low-stress nitride.²⁶ Finally, pointer structures allow for the analysis of the local distribution of stress and a separation of the stress gradient in contrast to the lateral and vertical

advantages
indicators

²⁵ The structures are not confined laterally and are independent of ν_F .

²⁶ Possible reasons for the change of material properties in dependance of the layer underneath include: different initial growth conditions of the functional layer, viscous deformation of the intermediate layer during anneal, and dopant diffusion with impact on the recrystallization during anneal.

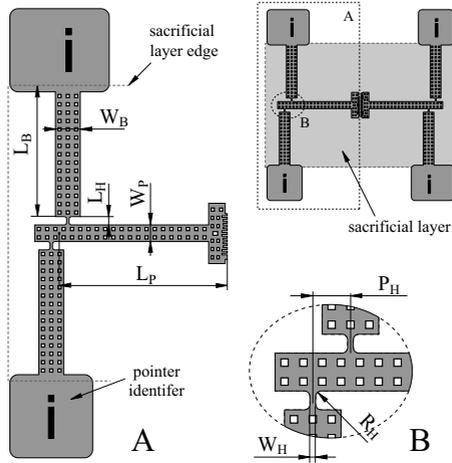


Fig. 2.7: Dimensional drawing of the pointer structure used for stress measurement of surface micromachined LPCVD layers.

average value obtained from wafer curvature. A structure for the measurement of the stress gradient is described in Appendix B.1.6.

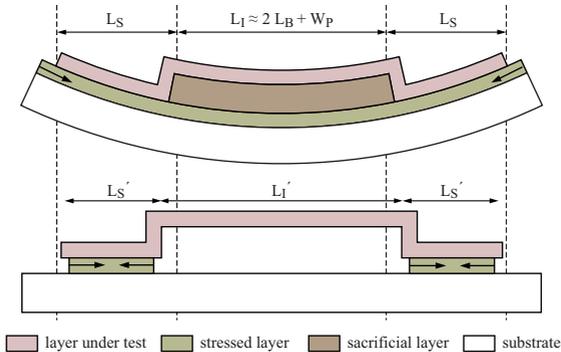


Fig. 2.8: Cross-sectional view of a surface micromachined beam illustrating the strain exerted by a partially removed second layers under tensile stress.

drawbacks
indicators

On the down side of indicator measurement there is to consider their worse performance in case of compressive stress and large stress gradients. For these cases the beams tend to bend upwards without movement of the indicator tip. Furthermore, indicators need to be structured and require a dry etch step for a reliable fabrication

of the indicator sprockets and hinges. Sticking must also be considered and takes place commonly during release of the pointers allowing to use them only once. Besides this, the most regrettable impact on the indicator performance have the hinges. Bending of these hinges consumes energy and lowers the indicated stress value up to 30 % (see correction factor C_H given in Tab. B.5). Therefore, the error due to hinge geometry deviation can be as high as 30 % too. Additionally, the strain of the indicator beams is influenced by any displacement of the indicator support itself as illustrated in Fig. 2.8. Solving (2.21) for the indicator displacement gives

$$N_s = S_i C_H \varepsilon^{(\text{beam})} \quad (2.23)$$

where $\varepsilon^{(\text{beam})}$ represents the strain of the indicator beams. This strain composes of intrinsic, and thermal stress of the layer under test, but also includes an additional external component ε_e .

$$\varepsilon^{(\text{beam})} = \frac{\sigma_t + \sigma_i}{E_F} + \varepsilon_e. \quad (2.24)$$

The external strain accounts for the displacement of the hinge support, which increases inversely proportional to the substrate's rigidity. For instance, a poly-silicon layer (PBOR560, $\sigma = 200$ MPa) is to be tested, which is deposited on top of an oxide sacrificial layer. In this case, a substrate protection layer is necessary to protect the fused silica bulk during the sacrificial etch. This protection may be implemented by means of a 100 nm low-stress nitride layer (Nit-Z20, $\sigma = 1.15$ GPa) on the wafer's top side. Suppose, the sacrificial etch is sufficiently long to remove the nitride layer completely, the initially stressed wafer relaxes, thus increasing the initial indicator beam length L_I to L_I' (see Fig. 2.8). The magnitude of this change can be calculated with (B.8). Additionally, the stressed nitride film remaining below the indicator support contracts, giving rise to a local displacement of the indicator support. According to numerical simulations, about 5 nm for the given example (approximately 2 nm on silicon) must be expected. The resulting error depends on the indicator geometry and ranges for the exemplary case between 3.4 %–7.2 % on fused silica. Results for the individual indicators on silica and silicon are provided in Tab. B.7.

2.2.5 Stress of CVD deposits on fused silica

The total stress of insulators and different types of poly-silicon on fused silica have been studied prior to and during anneal. The layers were deposited simultaneously on silicon and silica substrates to allow a direct comparison. Unless otherwise noted, stress data was measured by means of wafer curvature as discussed in Section 2.2.1.

The results for three kinds of silicon low-stress nitride as well as low temperature and high temperature CVD oxide are depicted in Fig. 2.9(a). Displayed is the magnitude of total stress before and after anneal for 12 h at 800 °C following the procedure given in Section B.1.2. Results for un-doped and in situ boron-doped poly-silicon are given in Fig. 2.9(b). As explained in Section 2.2.2, a general increase in total stress due to the low TEC of the silica substrate can be observed with predicted magnitude (see Fig. 2.3). A change in the stress difference ($\Delta\sigma = \sigma_{FS} - \sigma_{Si}$) prior and after

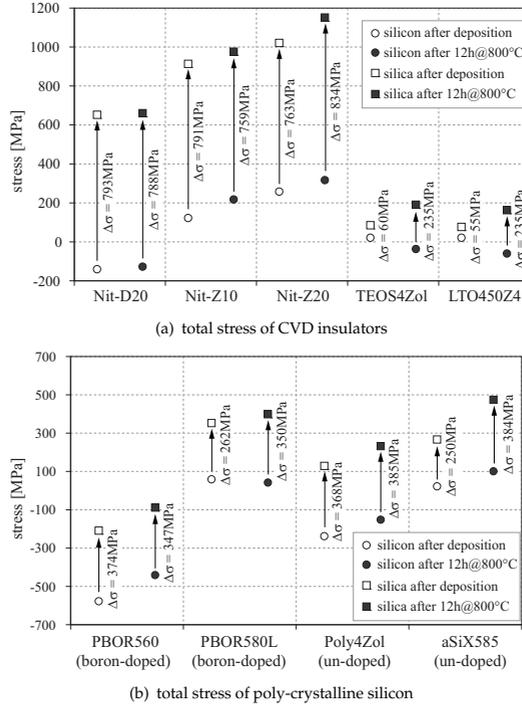
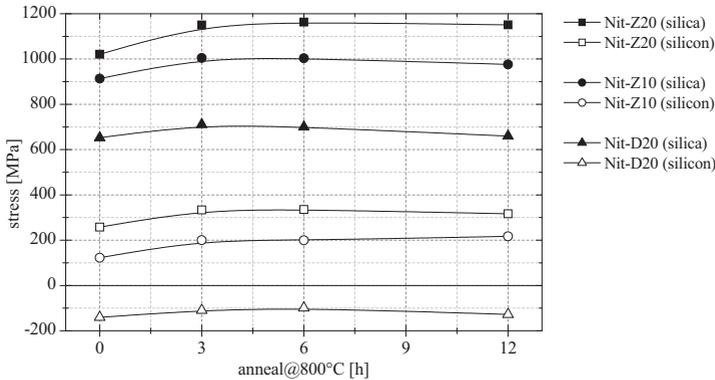


Fig. 2.9: Stress comparison of LPCVD insulators deposited on silicon and fused silica substrates (stress was evaluated after deposition and after anneal).

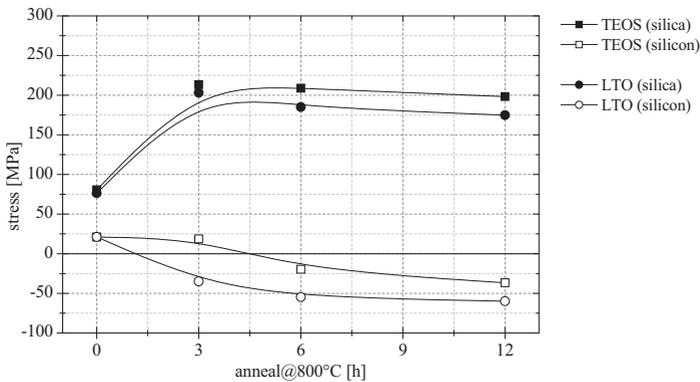
the anneal indicates a different evolution of the film's intrinsic stress on silica and on silicon during anneal. This might be due to viscous deformation of either film, base layer, or the substrate itself and will be discussed in more detail later for each deposit individually.

low-stress
silicon nitride

The stress evolution of low-stress silicon nitride is depicted in Fig. 2.10(a). The generally high stress levels even of low-stress nitrides on silica pose a strong thickness limit for the deposition of crack and fracture free films of approximately 180 nm. All layers show an increase in stress upon anneal on silicon and silica with similar magnitude. This increase is inversely proportional to deposition temperature T_d (see Tab. B.11). The lower T_d is the higher is the incorporated atomic fraction of hydrogen. This hydrogen is driven out during anneal and new Si-N bonds lead to a growing intrinsic stress of the layer. That is, the magnitude of stress increase is proportional to the incorporated H_2 in the as-deposited layer and stops immediately after all H_2 has left the deposit. Important for micromachining of low-stress nitride layers on silica is to note the thermal and morphological stability of these layers.



(a) low-stress CVD nitride



(b) low and high-temperature CVD oxide

Fig. 2.10: Stress of low-stress nitride and CVD oxide on silicon and fused silica after deposition and anneal in N_2 (the substrate type is indicated in parenthesis).

The viscosity of CVD-nitride is approximately two orders of magnitude larger than that of silicon oxide (see Fig. 2.4). Therefore, these layers can be regraded being stable in structure and stress during a moderate anneal because of their high viscous time constants τ (see Tab. 2.3). The maximum viscous relaxation of the fabricated silicon-rich nitride layers is estimated to be below 10 MPa during 8 h at 800 °C (see Tab. 2.4).

The stress evolution of high-temperature TEOS oxide (TEOS: tetra-ethyl-ortho-silicate, $SiO_4(C_2H_5)_4$) and LTO (LTO: low-temperature oxide)²⁷ is given in Fig. 2.10(b).

CVD oxide

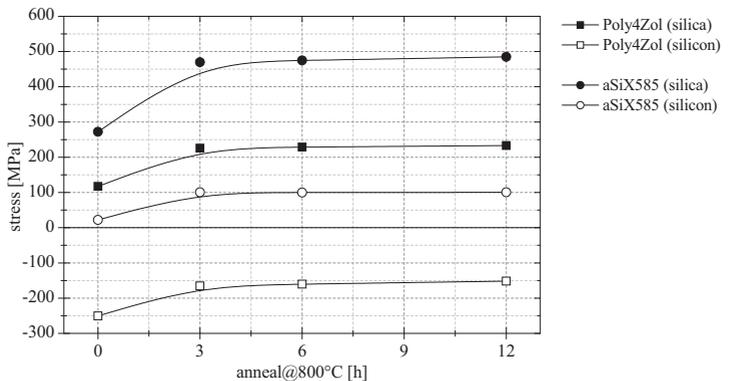
²⁷ LTO is deposited from a DES source (DES: di-ethyl-silane, $SiH_2(C_2H_5)_2$).

The sign of stress change depends on the choice of substrate and is indicative for viscous deformation of the film and implies TECs for both oxides between α_{FS} and α_{Si} . The intrinsic stress of as-deposited CVD oxide is approximately 300 MPa – 380 MPa [Car02] [Smo85] [Sta92]. This high intrinsic stress level is attributed to incorporated byproducts from the large precursor molecules and is almost balanced by a thermal stress of similar magnitude at room temperature. Equation 2.15 gives a 98.5 % relaxation of a CVD oxide layer after 12 h at $T_a = 800^\circ\text{C}$. That is, the total stress at ambient temperature after a complete relaxation during anneal is equal to the thermal stress component.²⁸ This allows the calculation of the mean TECs for both layers under test within the temperature range of $20^\circ\text{C} - 800^\circ\text{C}$ from the σ reading after anneal and (2.9). Consistent results are obtained with $\alpha_{TEOS} = 3.3 \times 10^{-6} \text{ K}^{-1}$ and $\alpha_{LTO} = 3.0 \times 10^{-6} \text{ K}^{-1}$. These coefficients are much larger than the usually reported $0.5 \times 10^{-6} \text{ K}^{-1}$ for SiO_2 at room-temperature. To explain this, a strong increase of the TECs at higher temperatures must be noted increasing the average TECs (see also Section 2.2.2 and [Sin78]). One feature of fused silica as substrate material is a tensile stress of layers which are usually compressive on silicon. This is e.g. the case for CVD oxide. As consequence, free standing *laterally supported* structures like membranes can be fabricated with SiO_2 as functional layer.

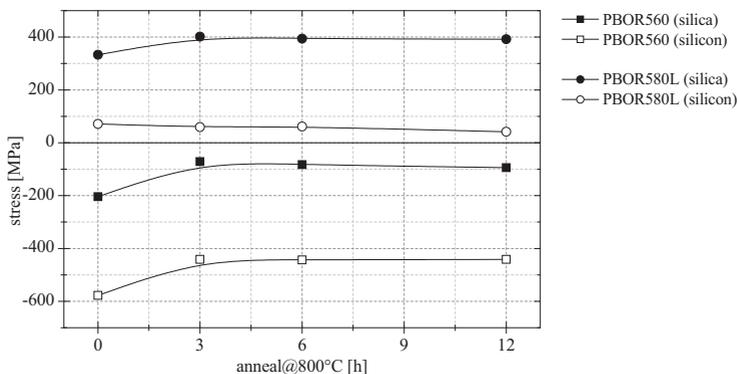
poly-crystalline
silicon

The interpretation of the stress measurement data of poly-silicon layers is more complicated because it requires knowledge about the as-deposited morphology and its evolution during anneal. For the time being it is sufficient to take the layers PBOR560 and Poly4Zol as fully crystalline and PBOR580L together with aSiX585 as partially crystalline (for a more detailed discussion of the internal structure of poly-silicon refer to Section 2.3). Crystalline as-deposited layers have a high intrinsic compressive stress component inversely proportional to the mean crystallite diameter. The smaller the grains are the more grain boundaries exist and the higher becomes the intrinsic compressive stress (see also Section 2.3.1). That is why the very fine grained PBOR560 is the most compressive layer in the as-deposited state. The size of the resulting crystallites during primary growth versus time can be represented by the root function (2.36) with a magnitude scaling exponentially with T_a . As result, asymptotic curves with decreasing intrinsic compressive stress can be observed for all poly-crystalline deposits no matter if un-doped (see Fig. 2.11(a)) or boron-doped (see Fig. 2.11(b)). This feature of poly-silicon must be noted because it enables an asymptotic stress adjustment to a level which corresponds to the chosen annealing temperature. However, this attribute of fully crystalline layers can not be utilized for surface micromachined clamped structures on silicon because of the compressive total stress of the layers on this substrate material at room temperature. In contrast, the increased thermal stress component of these layers on silica renders the total stress tensile (see Poly4Zol in Fig. 2.11(a)). Especially, the very fine grained PBOR560 can be annealed to a low tensile stress (if grown on oxide) as can be observed in Fig. 2.14. The same layer, if grown on silicon nitride (see Fig. 2.11(b)) remains compressive. This influence of the base layer on the growth of poly-silicon must be noted and can be attributed to the surface properties of silicon nitride and

²⁸ Thermal stress of wet oxide and CVD oxide after 16 h anneal at 1200°C is -330 MPa as measured by [Gia98]. This is exactly the thermal component of stress and shows the complete relaxation of the layer at annealing temperature.



(a) un-doped semi-crystalline and crystalline poly-silicon



(b) boron-doped semi-crystalline and crystalline poly-silicon

Fig. 2.11: Stress of un-doped and boron-doped poly-silicon after deposition and anneal in N_2 on silicon and silica substrates (the substrate type is indicated in parenthesis). Films aSiX585 and PBOR580L are semi-crystalline after formation. All layers have been deposited on a Nit-Z20 base layer.

its impact on the adsorption of silane. A more detailed discussion can be found further below in this section.

More vaguely becomes the discussion on stress of amorphous and partly amorphous silicon layers. The difficulty of viscous deformation of the amorphous or semi-crystalline deposit is highlighted by the graphs for aSiX585 and PBOR580L in Fig. 2.11. If these graphs are compared to the corresponding poly-crystalline as-deposited layers (Poly4Zol and PBOR560) depicted in the same figure, a different stress evaluation of the same layer on the two substrates must be noted in case of

semi-crystalline and
amorphous silicon

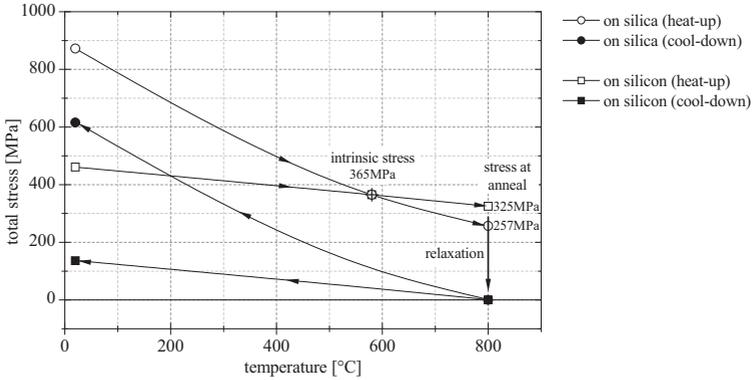


Fig. 2.12: Viscous relaxation of semi-crystalline silicon PBOR580L during anneal on silicon and fused silica substrates. The stress at annealing temperature $T_a = 800$ °C relaxes entirely. Room-temperature stress after cool-down is determined by the mismatch of thermal strain of deposit and substrate. The approximate intrinsic stress of the layer is marked at $T_d = 585$ °C.

the semi-crystalline films. On the other hand, the poly-crystalline layers change with similar magnitude and sign, no matter which substrate material was chosen. All layers in Fig. 2.11 have been deposited on top of a low-stress nitride layer which can be regarded as stable at the applied annealing conditions (the silica can be as well regarded being stable). With this in mind, it must be concluded that the partially crystalline layers under test relax during anneal to a certain extent, and that the resulting stress at room-temperature composes solely of the thermal stress component if a complete relaxation is assumed.²⁹ The final total stress of the semi-crystalline as-deposited layers depend on the deposit's and substrate's TECs. This conclusion is supported by a quite similar stress of aSiX585 and PBOR580L after anneal regardless the considerably different deposition conditions of these un-doped and boron-doped layers. Nevertheless, the observable deviations must be attributed to the composition depended layer TEC of the deposit and the individual state of relaxation after completion of the chosen annealing procedure.

The base layer, on which films are grown, have a twofold impact on the resulting layers stress. Firstly, the layer's morphology changes depending on the initial growth conditions. Secondly, a thermally instable base layer such as TEOS or LTO may itself deform during anneal and influence the measurement results if these are based on curvature readings. The problem is illustrated by Fig. 2.12. The graph shows the temperature dependent total stress σ_a of a PBOR580L layer deposited on a 500 nm TEOS base. The calculated magnitude of σ_a is given for a temperature ramp-up to 800 °C for deposits on silicon and on silica. The thermal stress decreases to zero at deposition temperature (T_d of PBOR580L: 580 °C). An intrinsic stress of approximately 365 MPa (on TEOS) remains at T_d . During further ramp-up, the

²⁹ Low viscosities for amorphous silicon have been reported by [Wit93] and [Vol93].

thermal stress becomes compressive, resulting in a substrate's TEC dependent stress at the final annealing temperature. The remaining stress relaxes due to viscous deformation proportional to the chosen annealing time. This stress relieve may either be caused by the deposit itself or may be due to deformation of the layer underneath. As stated above, a 98.5 % relaxation of TEOS during 12 h at 800 °C can be expected according to (2.15). In this way, a CVD oxide must be regarded as a floating base for thermally more stable deposits on top of it. That is, the resulting room-temperature stress after extended anneals on CVD oxide is solely equal to σ_t . It was necessary to take a mean TEC for the re-crystallized poly-silicon 17 % above the value of single crystal silicon to obtain consistent results for the example depicted in Fig. 2.12. This large TEC seems to be in disagreement with the low TECs given above for the poly-crystalline as-deposited layers, but some researches have also reported large poly-silicon TECs like [Sha01]. The results of the latter work suggest, that these large TECs result for *re-crystallized* layers, but that the TECs for poly-crystalline *as-deposited* layers are smaller than the TEC of single crystal silicon. The knowledge of the TEC is one step towards the interpretation of the overall annealing behavior and enables the approximate calculation of the intrinsic layer stress.

The morphology of deposits can be influenced by the chosen base layer. In the case of poly-silicon deposition, the initial growth zone extends approximately 200 nm into the deposit (see e.g. [Elb98]). Growth starts at localized islands on the base layer. The number and crystal quality of these islands depend on the mobility of adsorbed precursor atoms i.e. the number of free surface sites of the base layer. Oxide surfaces are known for their small free surface energy and cause fine-grained poly-silicon growth regimes. (Unchanged process conditions would result in a coarser grain structure if deposition would take place on silicon which has a higher free surface energy.) A film stress comparison of in situ boron-doped layers deposited on low-stress nitride and CVD oxide is given in Fig. 2.13. A consistent shifts towards a higher tensile total stress can be observed for all layers grown on oxide. This can be attributed to a finer grain structure of poly-silicon deposited on nitride in comparison to layers growth on silicon oxide (an extensive comparison of layer growth on SiO₂ and Si₃N₄ can be found in [Cla80a] [Cla80b] and [Cla80c], a structural comparison by means of TEM pictures is given by [Cau04]). The different stress evolutions during anneal, which are depicted in Fig. 2.13, can be explained by viscous flow of the CVD oxide (see preceding paragraph).

The latter discussion shows that the resulting layer stress of amorphous or semi-crystalline films is in direct relation to the stress at annealing temperature. These layers are most commonly utilized for surface micromachining on silicon substrates. By changing to fused silica substrates also σ at T_a is changed. It comes that all amorphous or partially amorphous silicon layers show a comparably large stress on silica. They are therefore not well suited for surface micromachining because commonly a low tensile stress is required. On the contrary, these partly amorphous silicon layers have due to the same reason a low tensile stress after anneal on silicon (see aSiX585 and PBOR580L on silicon in Fig. 2.11) and are accordingly often utilized as functional layer on this substrate material. As a conclusion, it is found that poly-crystalline as-deposited layers are well suited for micromachining on fused silica. The advantage of a silica substrate is a straight forward stress control of poly-

influence of
base layer
on the film's
morphology

improved
stress control
on fused silica

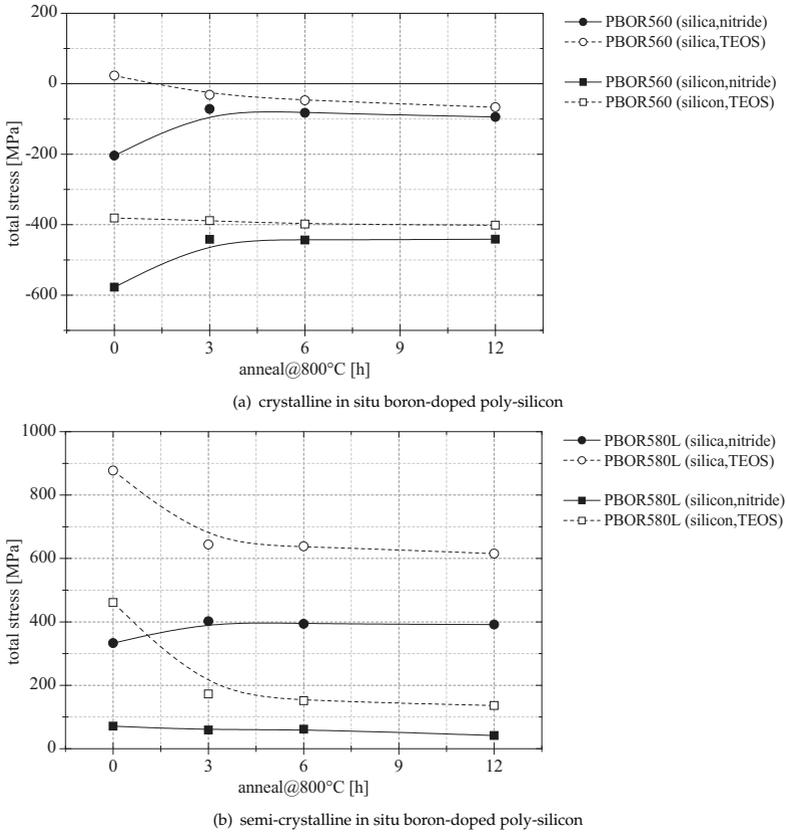


Fig. 2.13: Stress of in-situ boron-doped poly-silicon (crystalline and semi-crystalline) with grown on a nitride or a TEOS base layer (substrate type and respective base layer are indicated in parenthesis).

crystalline silicon by means of annealing temperature adjustment in order to obtain tensile layers. This convenient asymptotic stress adjustment is possible because of the exponential dependency of grain boundary mobility (2.37) on temperature and the grain growth dynamics (2.36).

A stress comparison of semi-crystalline and crystalline in situ boron-doped poly-silicon after various annealing procedures is presented in Fig. 2.14. All layers were deposited on 350 nm nitride covered³⁰ substrates and the readings were taken with surface micromachined indicators (which were attached to the nitride). TEOS is-

³⁰ The substrates were covered with a nitride stack of 100 nm Nit-D20, 100 nm Nit-Z10, and 150 nm Nit-Z20.

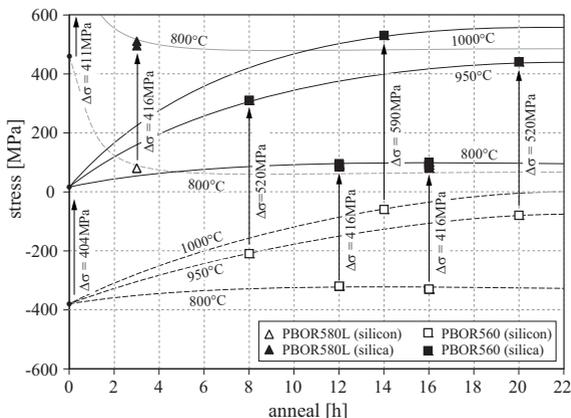


Fig. 2.14: Stress of 900 nm in-situ boron-doped semi-crystalline (PBOR580L) and polycrystalline (PBOR560) silicon on fused silica and silicon substrates after different annealing procedures. The layers were deposited on 350 nm nitride covered substrates. Stress readings were taken with surface micromachined indicators (attached to the nitride). A 500 nm TEOS film served as sacrificial layer.

lands with a thickness of 500 nm were used as sacrificial layer. Therefore, the presented results must be compared to the data of un-patterned deposits on TEOS presented in Fig. 2.13. A quite good agreement can be observed for the as-deposited layers and the ones annealed at 800 °C, but also a significant discrepancy for the others annealed at higher temperatures. It must be noted that the difference of stress $\Delta\sigma$ is constant for a certain annealing temperature and that the magnitude of $\Delta\sigma$ increases with T_a . Although this fact is very striking, the actual magnitude of stress reading can not be explained by any of the preceding film relaxation mechanisms of this section. It is supposed that viscous deformation of the substrate itself influenced the results. A substantial stress relieve within the fused silica substrate after several hours at 950 °C or 1000 °C can expect from the discussion in Section 2.2.2. It should result in a much higher stress than the actual observed level. This shows that real life is much more complicated and the stress exerted on the bulk silica must be considered to stem from a layer stack consisting of nitride ($\sigma_a > 0$) and poly-silicon ($\sigma_a < 0$). The resulting stress at annealing temperature is for this reason related to the stress of the whole layer stack and the advance of the viscous relaxation within the substrate bulk. As stated before, annealing procedures on silica should be limited to temperatures below 800 °C. Up to this temperature the substrate bulk can be considered stable for common annealing durations and complicated interactions of local layer stress and viscous bulk flow are prevented.

the mean
and sneaky
real life

Nitride stacks of this thickness show concentric cracks, which can only be observed after a sacrificial etch and do not interfere the results of local stress indicator readings.

2.2.6 Influence of temperature and humidity

Passivation layers are commonly used to protect micromachined structures against environmental influences such as humidity and chemicals. A measure for their protection capabilities is the change of layer stress during exposure to climate stress. In addition, stress changes within the passivation can also influence the characteristics of micromachined transducers if the layer exerts stress on the transducer. Therefore, LPCVD TEOS, PECVD lf-oxide, and PECVD hf-oxide films were simultaneously deposited on 10 cm silicon and fused silica substrates. The stress of these samples was monitored by means of wafer curvature during a sequence of successive humidity and temperature treatments.³¹

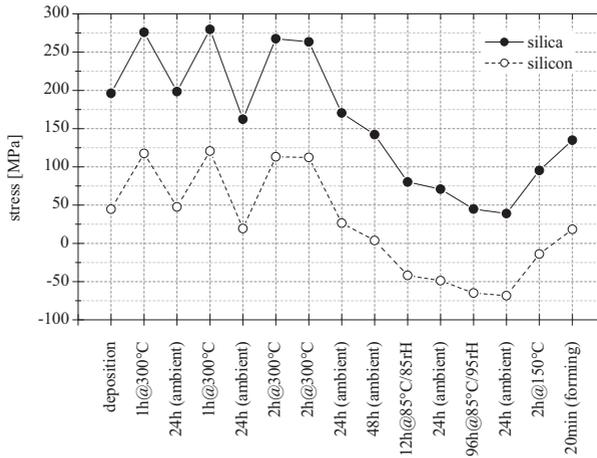


Fig. 2.15: Influence of humidity on the stress of TEOS. Stress was simultaneously measured on 10 cm silicon and fused silica substrates by means of wafer curvature after the indicated treatments (forming: N_2/H_2 ambient at 400 °C).

LPCVD TEOS

Measurement results for LPCVD TEOS are depicted in Fig. 2.15. It can be noted that LPCVD oxide is very susceptible to humidity uptake. Water diffuses readily in and out of the layer causing a stress change of up to 200 MPa at an ambient stress level³² of 200 MPa and 50 MPa for silica and silicon, respectively. It can be noted that humidity, which is driven into the layer at elevated temperatures, does not exit the layer within 24 h at ambient conditions but must be forced out at by means of a high temperature anneal. The TEOS deposition temperature is 700 °C and short time exposure to temperatures up to 400 °C (aluminum forming or reflow soldering) does not change the layer stress irreversibly.

³¹ The stability of an aluminum metallization was also test. The results are depicted in Fig. 2.34.

³² Clean room: 50 %RH at 22 °C

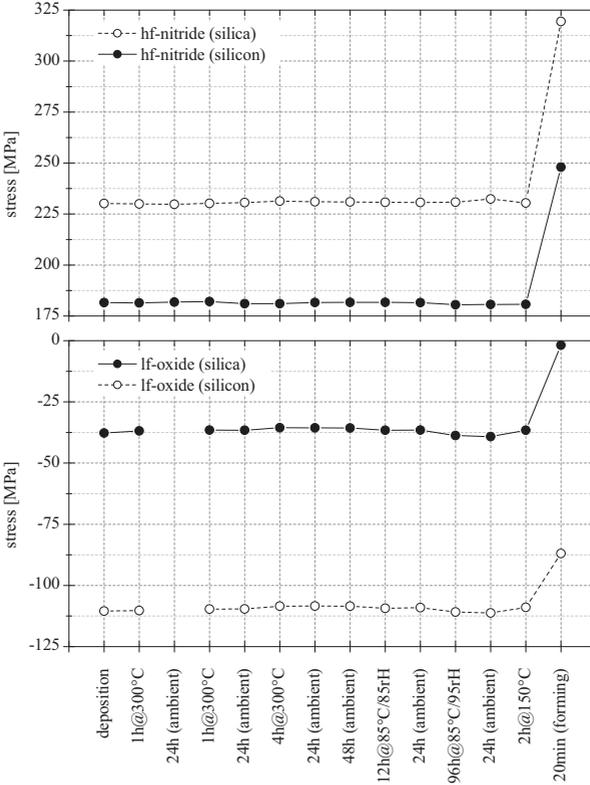


Fig. 2.16: Influence of humidity on the stress of PECVD lf-oxide and PECVD hf-nitride. Stress was simultaneously measured on 10 cm silicon and fused silica substrates by means of wafer curvature after the indicated treatments (forming: N₂/H₂ ambient at 400 °C).

The tested PECVD layers are less affected by humidity stress than the LPCVD TEOS as can be observed in Fig. 2.16. Only small stress changes can be observed for lf-oxide. The deviations of the hf-nitride readings can be attributed to the measurement uncertainty. Similar to the case of TEOS, humidity, which was driven in at 85 %RH at 85 °C, does not exit the layer at ambient conditions. The layer stress is not restored before an anneal at elevated temperature is conducted. Important to note is the impact of the short forming gas treatment at 400 °C which causes a pronounced increase of the layer stress.³³ The impact of temperature can already be

PECVD lf-oxide
PECVD hf-nitride

³³ Exposure to temperatures above 450 °C lead to cracking and delamination all tested PECVD layers (stress time was longer than 4 h).

observed after 6 h at 300 °C leading to a slight increase of the I_f -oxide stress.

The comparably good performance of the tested PECVD layers under humidity stress surprises. A possible explanation may be the commonly higher hydrogen content of these layers passivating dangling bonds. A higher number of un-passivated bonds can be assumed for the LPCVD deposit increasing the diffusion constant of humidity within the TEOS layer. The strong increase of the PECVD layer stress at elevated temperatures might be attributed to the same origin. Incorporated hydrogen exits the layer at temperatures above the deposition temperature and new bonds can form increasing the intrinsic stress component.

2.3 Surface micromachining

The presented sensor is almost entirely surface micromachined with all the related difficulties. Considering the progression of sensor development one must wonder why it took so long to finally fabricate a reasonably working prototype. Most of the encountered problems seem so simple and their solution do not look like achievements at all. Time was consumed by a large number of sometimes very small and silly mistakes. Any kind of helping information at hand would have been very appreciable during time of development. Therefore, it is the intention of this section to provide at least some food for thought with out the necessary depth in many cases but to be hopefully useful for required follow-up work. Many characteristics of the sensor are still not unambiguously attributed to a certain physical phenomena. However, the following sections summarize a number of promising candidates. *Middlehoek*, as one of the pioneers, supposed **microelectromagnetomechanoradio-optochemical systems (MEMMROCS)** as name for micromachined systems. This illustrates perfectly in one word that the required knowledge for a complete understanding approaches infinity, and that these small systems have the potential to irk the sometimes desperate engineer in thousand different ways.

2.3.1 Thin-film deposition

The class of surface micromachined transducers require, similar to bulk micromachined systems, sophisticated lithography and etching procedures, but in addition, physical, chemical, and electrical transducer material properties must be controlled accurately. Moreover, these layer properties must be homogeneous and reproducible. Thin-film deposition is the key issue during surface micromachining. It is origin for time consuming and costly development processes. The bulk material influences the results in some cases. Issues related to the silica bulk will be addressed through out the following sections.

Low-stress silicon nitride

Silicon nitride is an important layer because of its frequent application as diffusion barrier and protection layer as well as dielectric insulation. An extra issue poses the low TEC of fused silica if micromachining of nitride takes place on this special substrate. The large thermal mismatch of substrate and film does not allow

the deposition of stoichiometric nitride layers and one has to use silicon-rich nitride instead. Already these silicon-rich nitride deposits must be limited to a certain thickness unless cracks and fracture can be accepted. Any fissures must be in particular prevented if the nitride has to act as a wet-chemical protection layer at a later stage of the process.

For this work, low-stress nitride was chosen as protection during wet-chemical etching as well as dielectric insulation. Additionally, the pressure transducer plates are supported on the nitride layer and the mechanical stress of the latter influences the sensor's performance. It follows that a discussion of the deposition process with its impact on stress, dielectric properties and homogeneity (stress and thickness) is required and can be found in this section. The deposition of SiN_x by means of CVD is extensively discussed in literature and will only be briefly summarized.³⁴ More stress is put on the electrical insulation characteristics. These are rather poor and will influence the presented sensor adversely. Furthermore, dielectric properties will be discussed as they are commonly not considered in literature for the required application, i.e. an silicon-rich insulation layer at low field conduction fabricated by means of LPCVD under high tensile stress.

Deposition and layer stoichiometry

Already early publications analyzed the correlation of layer composition and state of mechanical stress with respect to the deposition parameters $\text{SiH}_2\text{Cl}_2/\text{NH}_3$ -ratio R_{CVD} and process temperature [Ire76] [Sek82]. In later works, additional information on homogeneity and influence of pressure were elaborated [Gar96] [TB98]. Throughout this work, silicon-rich nitride was deposited from di-chlor-silane (SiH_2Cl_2) and ammonia (NH_3) sources (see Tab. B.11 for the process details). Other silicon precursors are frequently used and described in literature like tetra-chlor-silane (SiCl_4) or silane (SiH_4). Although processes details may change in these cases, the general features of SiN_x formation remain:

$$\begin{aligned} R_{\text{CVD}} \uparrow &\longrightarrow \sigma \downarrow, r_d \downarrow, \Delta r_d \uparrow, n \uparrow, x \downarrow \\ T_d \uparrow &\longrightarrow \sigma \downarrow, r_d \uparrow, \Delta r_d \uparrow, n \uparrow, x \downarrow \\ p_d \uparrow &\longrightarrow \sigma \uparrow, r_d \uparrow, \Delta r_d \uparrow, n \downarrow, x \uparrow \end{aligned}$$

where T_d and p_d denotes deposition temperature and pressure, r_d and Δr_d deposition rate and its inhomogeneity over the boat. Layer stress σ always correlates with stoichiometric index $x = N_{\text{N}}/N_{\text{Si}}$ and index of refraction n .

It is found that a thermal compressive stress of approximately -350 MPa is exceeded by a very large intrinsic component resulting in an overall stress σ of approximately 1.2 GPa for the case of stoichiometric Si_3N_4 on silicon substrates. The high tensile intrinsic stress is attributed to highly strained bonds. Three factors raise this intrinsic stress and increase the etch rate of the deposit in hydrofluoric acid at the same time: an increase of the *Si-N bond density*, a reduction of *surface mobility*, and an increase of *H₂ incorporation*. That is, a higher silicon content lowers the stress

thermal & intrinsic
stress component

³⁴ A good introduction is given by [Fre97].

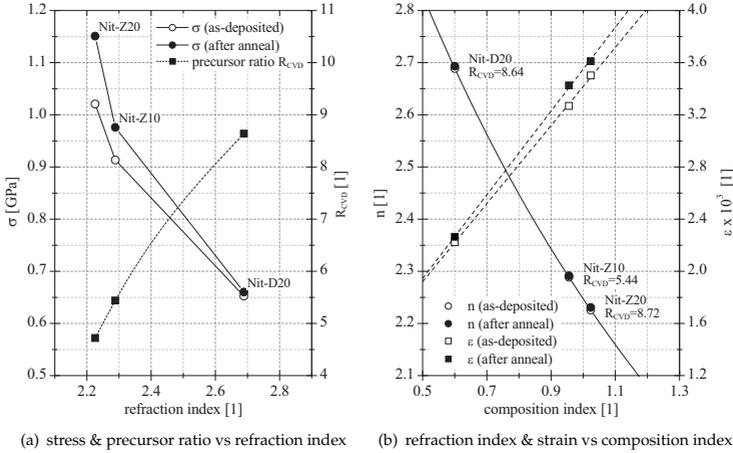


Fig. 2.17: Stress and strain of silicon-rich nitride on fused silica versus index of refraction and layer composition. The full line of Fig. 2.17(b) illustrates the result of (2.25) whereas the broken lines stress the linear relation of layer composition and strain (the graph for annealed layers was calculated with (2.28)).

and can be achieved by increasing R_{CVD} . All measures that increase the surface mobility also lower the stress, because adsorbed atoms have sufficient energy to travel far enough to form low energetic bonds. Finally, hydrogen incorporation plays an important role as discussed in [Nos88] [TB98]: firstly, impurities in general give rise to distorted bonds and to stress within a deposit, secondly, hydrogen continues to diffuse out of the deposit as the deposition proceeds and highly strained bonds form at these vacant sites.³⁵ That is, the stress reduces as the deposition rate decreases because of a net lower number of buried hydrogen atoms. The thermal budget of the deposit increases from the surface to the substrate. Hence, more H_2 is driven out of the layer part close to the substrate interface. Therefore, intrinsic stress increases in this region and results in a negative stress gradient observable for all nitride deposits.³⁶

The layer composition changes with the source gas ratio R_{CVD} . The net incorporation of silicon increases with R_{CVD} , whereas the density of the deposit drops slightly [Mak83]. Figure 2.17(a) shows that the refraction index n approaches the value of 1.98 for stoichiometric nitride.³⁷ According to [Mak83], a direct relation for

³⁵ Approximately 5 at%–8 at% of hydrogen is incorporated During LPCVD of silicon nitride [Ste83].

³⁶ A thin boundary layer forms very close to the substrate and an investigation with focus on this wafer-deposit interface can be found in [Sta92] stating a boundary layer of 5 nm thickness with compressive stress.

³⁷ Not depicted are deposits with R_{CVD} below unity. It is found that any further decrease of R_{CVD} below the value of 0.25 leads to no appreciable change in stoichiometry.

stress and
stress gradient
 H_2 incorporation

layer composition
and atomic ratio

n and atomic ratio $x = N_N/N_{Si}$ can be given

$$n = \frac{n_{Si} + \frac{3}{4}x(2n_{Si_3N_4} - n_{Si})}{1 + \frac{3}{4}x} \quad (2.25)$$

where $n_{Si} = 3.85$ and $n_{Si_3N_4} = 1.98$ denote the index of silicon and stoichiometric nitride, respectively. Basic algebraic manipulation yields

$$x = \frac{4}{3} \frac{n_{Si} - n}{n + n_{Si} - 2n_{Si_3N_4}} \quad (2.26)$$

and the actual ratios of $x = 1.04$ and 0.61 for Nit-Z20 ($n = 2.221$) and Nit-D20 ($n = 2.674$), respectively. The usefulness of refraction index measurement is further stressed by the fact that layer strain ε also relates linearly to the atomic ratio [Fre97]. Therefore, strain is also related to index by considering (2.26) and film stress measurement is possible by means of optical refraction index measurement.³⁸ The reported direct correlation of refraction index n , layer strain ε , and atomic ratio x of the deposit are illustrated in Fig. 2.17(b). For the deposits of this work the following approximate linear relations for x and strain after anneal at 800 °C on silicon and silica can be given

$$\varepsilon_{Si} = (2.995x - 2.198) \times 10^{-3} \quad (2.27)$$

$$\varepsilon_{FS} = (3.211x + 0.339) \times 10^{-3}. \quad (2.28)$$

Strain also seems to be the cause for density deviations of the deposits and the linear correlation of atomic density and composition index x [Toi03].

strain
on silica

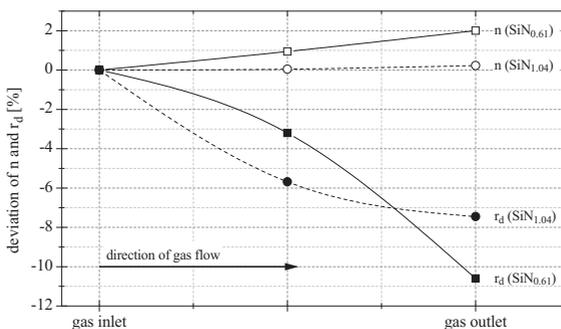


Fig. 2.18: Inhomogeneity of LPCVD SiN_x -processes. The deviation of deposition rate and refractive index is given normalized to their value at the gas inlet.

The deposition of silicon-rich nitride is challenging because it is an inherently in-

³⁸ The modulus of silicon nitride changes only slightly over a wide range of stoichiometry (see Fig. 2.6 or refer to [MS95]). For this reason x and n give also a fairly good measure for the film's mechanical stress.

inherent
inhomogeneity

homogeneous process due to the depletion of NH_3 along the wafer load. This is illustrated by the typical results given in Fig. 2.18. The more the deposition conditions along the wafer load differ from a stoichiometric composition the more the deposition rate decreases. Therefore, as NH_3 depletes, x drops (n increases), and accordingly, also r_d decreases. The deposition rate can be adjusted with the straight forward approach of a positive temperature ramp over the boat but, as stated above, σ and x decreases if T_d increases. That is, it is either possible to achieve a quite uniform layer composition (and stress) along the load or a uniform thickness. The situation gets worse the higher R_{CVD} is chosen, because ammonia depletes faster with increasing R_{CVD} . Some experiments with regard to homogeneity can be found in [Gar96] supporting the latter observations. The homogeneity can be improved by all measures that hinders depletion, i.e. deposition rate reduction by means of decreasing T_d and p_d . Uniformity of stress and thickness can be reasonably improved by means of a double deposition with mirrored wafer positions.³⁹

improved
homogeneity
on fused silica

The magnitude of the thermal stress component is raised for a nitride deposit on fused silica leading to an overall increased stress level. Advantageous is that the relative importance of the inherent inhomogeneity of σ_i , as described above, is lowered if σ_t increases. From the inhomogeneity of n depicted in Fig. 2.18 follows with (2.26) a corresponding deviation in x of $\pm 0.27\%$ ($\text{SiN}_{1.04}$) and $\pm 2.7\%$ ($\text{SiN}_{0.61}$) over the reactor load. According to Fig. 2.17(b), this deviation is in direct relation to an alteration of strain $\Delta\varepsilon$ and is also in approximate direct relation to a deviation of intrinsic stress $\Delta\sigma_i$ (which is equivalent to the deviation of total stress $\Delta\sigma$). An analysis of the ratio $\Delta\sigma/\sigma$ yields an inhomogeneity of $\pm 0.25\%$ of $\text{SiN}_{1.04}$ and $\pm 3\%$ of $\text{SiN}_{0.61}$ on fused silica about the reactor load. The same deposits would have an inhomogeneity of $\pm 1\%$ and $\pm 14\%$ on a silicon substrate.⁴⁰

Dielectric properties

SiN_x insulation
challenges

Four fundamental problems are related to nitride insulation layers: *high conductance, charge trapping, polarization and high surface charge densities* [Dea68] [Dea69]. The rather high conductance of silicon nitride in comparison to thermal silicon oxide is attributed to the bulk properties of SiN_x and results from the energy band structure, which is extensively discussed in [Rob91] and [Rob84]. It is agreed that conduction in stoichiometric films is due to a high hole mobility caused by tail states of the valence band. These states are dominated by $=\text{N}^-$ centers at higher N_2 content of the deposit, but are outnumbered by Si-Si centers as x drops below unity. The tail states of valence and conduction band extend further into the band gap the lower x drops, narrowing the gap almost symmetrically. Chains of bonded silicon break at x above unity into localized clusters and cause the gap to open steeply.

energy band
structure

Calculated energy gaps according to [Rob91] are given in Fig. 2.19 for the different kinds of nitrides used in this work. $\text{SiN}_{1.04}$ will be used as an insulation layer and

³⁹ Stacked depositions of nitride are feasible with no appreciable drawbacks, neither mechanical nor chemical. Reason for this is the very high thermal budget required for the oxidation of the deposit, which might take place during unloading and re-loading of the furnace.

⁴⁰ σ_t : ≈ 410 MPa (fused silica), ≈ -380 MPa (silicon); $\text{SiN}_{1.04}$: $\Delta\sigma = \pm 2.65$ MPa, $\sigma_i = 685$ MPa; $\text{SiN}_{0.61}$: $\Delta\sigma = \pm 19.5$ MPa, $\sigma_i = 256$ MPa

its band structure is for this reason depicted in more detail in Fig. 2.19(b) together with the sketched density of states of the band tails. Figure 2.19(b) also shows the energetic locations of the important $\equiv\text{Si}^0$ defect site. These trivalent bonded silicon atoms with one broken bond create highly localized sites and are considered to be charge traps with very long retention time [Fuj85]. The neutral $\equiv\text{Si}^0$ can catch holes as well as electrons and thus nitride layers can be charged with either polarity if stressed with a bias voltage above a certain field strength. Both of these special features of nitride, i.e. hole mobility and deep traps, have been widely utilized in non-volatile memories⁴¹, but are also a great concern for the stability of thin-film transistors with PECVD or PVD nitride insulation (see e.g. [Pow83]). The interaction of $\equiv\text{Si}^0$ and $=\text{N}^0$ determines the dielectric behavior of the nitride layer. Due to the energy level of the silicon dangling bond site $\equiv\text{Si}^0$, which lies above the dangling bond of nitrogen $=\text{N}^0$, these sites exchange charge and leave a net population of $\equiv\text{Si}^+$, $\equiv\text{Si}^0$, and $=\text{N}^-$ at equilibrium. The negatively charged nitrogen dangling bonds act as shallow hole traps and enable a hopping conduction at lower field strengths along an energy level right above the valence band. The same centers are also involved in high-field conduction by means of *Poole-Frenkel* emission (field assisted thermal excitation), which is the dominant transport process in silicon nitride at field strengths above about 400 MV/m ($\text{SiN}_{1.33}$, [Hab02]) and 50 MV/m ($\text{SiN}_{1.17}$, [Hab02]) if deposited on silicon substrates.

deep traps

conduction

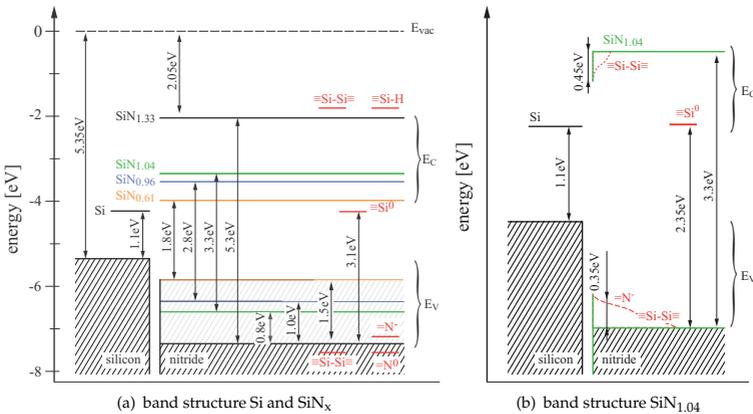


Fig. 2.19: Energy band structure and defect levels of SiN_x according to [Rob91]. Details for $\text{SiN}_{1.04}$ are depicted to the right also indicating schematically the density of tail states as well as the location of the $\equiv\text{Si}^0$ site within the band gap. Defect levels and tail states are colored in red.

Hydrogen can act as a passivation for silicon as well as nitrogen dangling bonds

⁴¹ Typical non-volatile memory structures are referred to as MNOS devices, i.e. metal nitride oxide semiconductor devices (see e.g. [Lun73]).

H₂ passivation
of bulk states

and roughly 5 at% – 8 at% H₂ remain in the layer after formation by means of LPCVD even at temperatures higher than 750 °C. This hydrogen can be driven out during successive anneal under H₂ free atmosphere. Some new bonds form at these vacant sites during such an annealing procedure (leading to an increased stress as discussed above). Although some new bonds form, a net increased number of dangling bonds remain within the layer. These dangling bonds are responsible for a degradation of the insulation performance of the nitride layer during anneal [Top76]. The weaker Si-H bonds break first at approximately 800 °C. Hydrogen, which is bond more tightly to the nitrogen, is driven out at temperatures above 900 °C [Ste83] [Rob91].

surface states

A high positive surface charge density of $(3 - 5) \times 10^{12} \text{ cm}^{-2}$ is reported to be common for LPCVD nitride deposited on a silicon surface [Hu66] [Dea68]. The reported magnitude is in good agreement with the charge density of $3.4 \times 10^{12} \text{ cm}^{-2}$ measured in this work (see Fig. 3.57).⁴² From this charge density can be estimated that every 200th surface atom acts as positive charge storage site.⁴³ The nature of these states is found to be very similar to the surface charges observed at CVD oxide interfaces to silicon, although their density is lower. The charge density is not dependent on crystallographic orientation of the substrate, and it is agreed that no incorporation of substrate (or base layer) material into the silicon nitride deposit takes place. Especially, the combination of rough surfaces with silicon nitride leads to high charge densities. Surface charges at oxide-silicon interfaces are commonly annealed effectively with hydrogen at low temperatures [Dea69]. Unfortunately, nitride acts as a diffusion barrier and either reduces or impedes the penetration of hydrogen at lower temperatures whereas the desired hydrogen passivated interface bonds break at higher temperatures. However, the experiments described in [Dea69] show that in saturated H₂-atmospheres at higher temperatures (700 °C – 1000 °C) hydrogen can penetrate the nitride and, due to their high concentration, result in a net increased incorporation into the interface. This measure is reducing the number of fast states by more than one order of magnitude. Fast surface states do also influence the sensor described in this work. The transient behavior of these states give rise to an interface capacitance if an ac voltage is applied across the interface. Charging and discharging of the surface states cause an energetic loss under applied ac voltage. This is resulting in an overall frequency and voltage dependence of the capacitance equivalent circuit of the nitride insulation on a silicon conductor (frequency and voltage dependent ac resistance, see Section 3.4.1).

H₂ passivation
of surface states

polarization

A bulk related polarization phenomenon of silicon nitride is reported [Dea68]. The polarization increases in rate with increasing temperature and its magnitude is proportional to the applied electric field. It is speculated that the cause for polarization are dipoles within the bulk material similar to those reported in doped glasses. However, also the $\equiv\text{Si}^0$ might be responsible because of its reported paramagnetic character [Rob91].

According to the preceding summary of silicon-rich nitride properties, one is not tempted to use silicon nitride as dielectric insulation. However, there are also some

⁴² Surface charge densities for low-temperature hydrogen annealed thermal oxide interfaces can be below the CV measurement detection limit of $5 \times 10^{10} \text{ cm}^{-2}$ [Dea69].

⁴³ <111> orientation: $7.85 \times 10^{14} \text{ atoms/cm}^2$; <110> orientation: $9.6 \times 10^{14} \text{ atoms/cm}^2$; <100> orientation: $6.8 \times 10^{14} \text{ atoms/cm}^2$ [Sze81]

positive aspects to mention. These must be considered especially for designs on fused silica. As described above, the insulation properties degrade as x drops, but the dielectric properties are in addition related to the mechanical stress. The higher the mechanical stress is the better gets the insulation. Nitride stress levels on silica are much higher than on silicon. Therefore, under favorable circumstances, an insulation made out of silicon-rich nitride on fused silica can be expected to perform as good a stoichiometric nitride insulation on silicon. The following paragraphs describe the impact of mechanical stress on electric conduction in silicon nitride.

positive impact of silica substrates

Charge transport in silicon nitride is reported to be primarily bulk limited and the current density J composes of three distinct contributions [Sze67]

charge transport in silicon nitride

$$J = J_1 + J_2 + J_3 \quad (2.29)$$

$$J_1 = C_1 E \exp \left[- \frac{q(\Phi_1 - \sqrt{qE/\pi\epsilon})}{kT} \right] \quad (2.30)$$

$$J_2 = C_2 E^2 \exp \left[- \frac{E_2}{E} \right] \quad (2.31)$$

$$J_3 = C_3 E \exp \left[- \frac{q\Phi_3}{kT} \right] \quad (2.32)$$

where J_1 accounts for field-enhanced thermal excitation (*Poole-Frenkel* emission), J_2 for field ionization and J_3 for hopping of thermally excited carriers between insulated states. Φ_1 and Φ_3 denote heights of potential barriers, q the unit charge, k the Boltzmann constant, ϵ the dynamic permittivity of the nitride, and C_1 to C_3 proportionality constants.

Poole-Frenkel emission dominates at higher temperatures ($T > 60^\circ\text{C} - 80^\circ\text{C}$) and high field E . Whether J_3 or J_2 prevails at room temperature is supposed to depend on the layer composition. J_2 is the major contribution for the case of a stoichiometric layer deposited at high temperatures (deposition at 1000°C from NH_3 and SiCl_4 precursors) [Sze67], but the data given in [Hab02] indicates a dominant J_3 .⁴⁴ In the latter report, nitride was deposited from a SiH_2Cl_2 source within a temperature range of $800^\circ\text{C} - 850^\circ\text{C}$. These process conditions are very similar to the conditions of this work. For this reason, the results are believed to be applicable for this work too. The results of [Sze67] and [Hab02] are summarized in Fig. 2.20(b) and the corresponding data can be found in Tab. 2.5. Current density J_3 gives a straight horizontal line in the J/E -plot whereas the lines with constant slope at higher field strength correspond to *Poole-Frenkel* emission. A good agreement of the measurement data can be observed at high field strength for $\text{SiN}_{1.33}$ but, as stated above, the film quality in [Sze67] (lower H_2 incorporation at higher temperatures) improved the insulation properties rendering J_2 dominant.

Almost no literature discussion on low-field charge transport in silicon-rich nitride can be found. The relevant magnitude for this work is $10 \text{ MV/m} - 50 \text{ MV/m}$ but most research on conduction focuses primarily on high-field strength conduction beyond approximately 400 MV/m . Common structures are referred to as MNOS de-

literature data on low field conduction

⁴⁴ PECVD nitride shows a very similar behavior and [Mel05] reported the major current contribution to be of *Poole-Frenkel* type with a surprisingly high barrier potential of about 1 V.

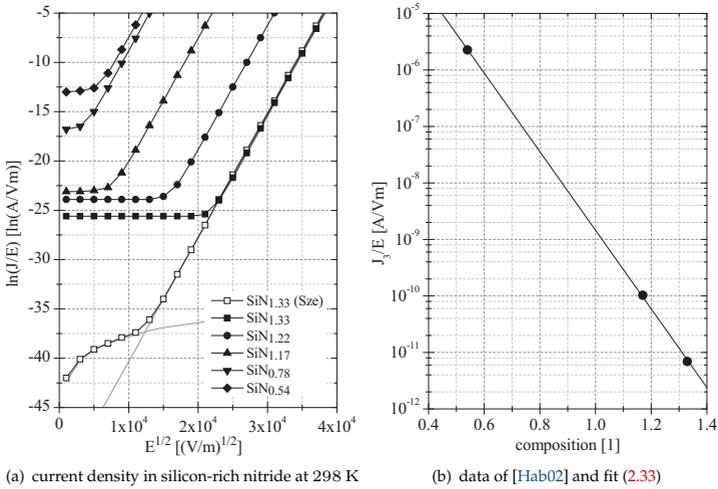


Fig. 2.20: Literature data on the conduction in silicon-rich nitride. Measurement data was taken from [Hab02] and [Sze67]. The low field tails of the silicon-rich nitride were calculated with fit (2.33), which is in very good agreement with the reported data. The full gray lines illustrate the contributions of Poole-Frenkel emission (straight line) and field ionization.

Table 2.5: Summary of parameters required for the calculation of the current density in silicon-rich nitride with (2.30) (dynamic permittivity $\epsilon_r = 5.5$) and (2.32). The values for J_3/E were calculated with (2.33) and the data given for deposits on fused silica at ambient temperature $T = 298$ K assume the validity of the fits (2.33) and (2.34).

composition	C_1 [A/Vm]	Φ_1 [V]	J_3/E [A/Vm]	strain $\epsilon \times 10^3$ [1]	stress σ [GPa]	comment
SiN _{1.33}	0.1	1.30	$< 2 \times 10^{-19}$	6.00	1.20	[Sze67]
SiN _{1.33}	1.44×10^{-5}	1.08	7.33×10^{-12}	6.00	1.20	[Hab02]
SiN _{1.22}	1.81×10^{-4}	0.91	4.27×10^{-11}	2.00	0.40	[Hab02]
SiN _{1.17}	2.75×10^{-3}	0.69	9.51×10^{-11}	0.08	0.02	[Hab02]
SiN _{0.78}	1.38×10^{-2}	0.44	4.91×10^{-8}	-2.00	-0.40	[Hab02]
SiN _{0.54}	3.86	0.55	2.30×10^{-6}	-2.60	-0.52	[Hab02]
silicon-rich nitride on fused silica						
SiN _{1.04}	1.36×10^{-5}	1.11	7.65×10^{-10}	5.76	1, 15	Nit-Z20
SiN _{0.96}	3.87×10^{-5}	1.02	2.76×10^{-9}	4.57	0.91	Nit-Z10
SiN _{0.61}	1.22×10^{-4}	0.92	7.49×10^{-7}	3.26	0.65	Nit-D20

vices (MNOS: metal nitride oxide semiconductor) and are used as nonvolatile memory cells together with floating gate devices. Both device types rely on the semi-insulating properties of a dielectric like e.g. silicon nitride at high-field strength. Whereas also focusing on high-field *Poole-Frenkel* emission, the work of [Hab02] must be noted for three reasons:

1. Also low-field tails of the measured data are given for silicon-rich nitrides. These tails indicate the magnitude of current conduction in the field strength regime relevant for this work. Furthermore, it will be shown with the data of [Hab02], that the regime of low-field conduction is extended up to 500 MV/m on silica because of the stress sensitivity of *Poole-Frenkel* emission. Additionally, a correlation of stoichiometry and low-field conductivity will be worked out further below.
2. The *Poole-Frenkel* emission barrier height Φ_1 is correlated with the residual Si-N bond strain and therefore corresponds also to the layer composition.⁴⁵ This finding is of particular interest for a layer deposition on fused silica substrates because a low-stress nitride like Nit-Z20 has a total stress of about 1.1 GPa at room temperature, a level which is comparable to the stress of stoichiometric nitride SiN_{1.33} deposited on silicon. Consequently, J_1 for Nit-Z20 on silica will be as low as for stoichiometric nitride deposited on silicon. However, this benefit can turn into a serious problem if the nitride insulation is operated under conditions, where *Poole-Frenkel* emission is dominant and the target application is sensitive to parasitic conductance changes. Any temperature change will lead to an alteration of strain within the nitride insulation and will therefore cause also a severe conductance shift. The change of conductance due to stress can be utilized as sensing means. Such a piezoconductive strain sensor is described in [Hab04]. The thermal stress of Nit-Z20, which is used as insulation layer in this work, is about 400 MPa at room-temperature, i.e. the stress in the insulation changes approximately with a rate of 0.5 MPa/K. This may have considerable impact on the sensor performance and must be noted.
3. The study covers a composition range of SiN_{1.33} to SiN_{0.54}, which includes the nitride composition of this work (SiN_{1.04} to SiN_{0.61}).

Although not stated in [Hab02], the magnitude of the low-field hopping conduction scales with the layer composition and can be fitted with an exponential function as depicted in Fig. 2.20(b). This is reasonable as it means that barrier height Φ_3 scales with the atomic fraction $x = N_N/N_{Si}$ of the layer. This correlation becomes also plausible if Fig. 2.19 is considered. A fit of the experimental data of [Hab02] to the function

$$J_3 = C_3 E \exp \left[- \frac{q\Phi_3 x/x_s}{kT} \right] \quad (2.33)$$

yields a potential barrier of $\Phi_3 = 0.55$ V and $C_3 = 1.31 \times 10^{-2}$ A/Vm.⁴⁶ Where x_s

⁴⁵ Mechanical stress was already supposed as influencing parameter on the charge trapping characteristics in earlier literature [Fuj85].

⁴⁶ Unfortunately no current density data at different temperatures and a low applied field strength was available to verify the general validity of the fit.

denotes the ratio of 1.33 for stoichiometric nitride. The latter fit was also used to represent the experimental data in Fig. 2.20(a).

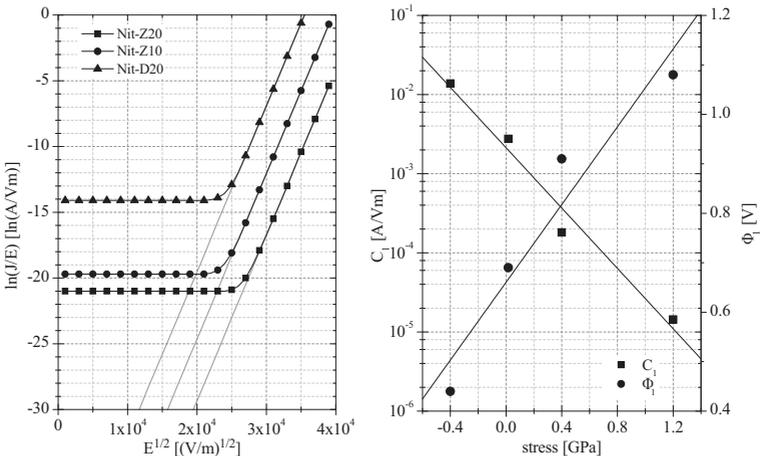
The potential barrier for *Poole-Frenkel* emission scales linearly with the Si-N bond strain [Hab02]. It is possible to give an approximate expression for *Poole-Frenkel* barrier Φ_1 as function of layer stress if the almost composition invariant modulus of silicon-rich nitride (see Fig. 2.6) and an stress of 1.2 GPa of SiN_{1.33} on silicon is taken into account

$$\Phi_1 = 0.39 \text{ V/GPa } \sigma + 0.66 \text{ V}. \quad (2.34)$$

It is straight forward to do a similar fit for the pre-exponential factor which gives

$$C_1 = 2.13 \times 10^{-3} \text{ A/Vm} \exp \left[- \frac{\sigma}{227.86 \text{ MPa}} \right]. \quad (2.35)$$

Experimental data and fits for Φ_1 and C_1 can be compared in Fig. 2.21(b). Actual values for the expected current densities of the deposits fabricated in this work are shown in Fig. 2.21(a) considering the latter fittings and the magnitude of the individual stress on fused silica.



(a) expected current densities on silica at 298 K

(b) data of [Hab02] and fits to (2.34) and (2.35)

Fig. 2.21: Estimated current densities in silicon-rich nitride deposited on fused silica. The calculations are based on (2.30) and (2.32) assuming the validity of the fits (2.34) and (2.35). The agreement of the latter fits to measurement data is shown to the right.

onset shift of
Poole-Frenkel
emission on
fused silica

It can be noted in Fig. 2.21(a) that the onset of *Poole-Frenkel* emission is retarded on fused silica due to the increased thermal stress in the layer. Actual values can be calculated with (2.30) and the fits (2.34) and (2.35) for the individual magnitude of stress. The hopping condition J_3 prevails up to a field strength of 500 MV/m and can

be directly related to the layer composition. The expected maximum field strength during operation of the presented sensor is about 170 MV/m , therefore, the bulk conductivity of the nitride insulation is expected to be well described with (2.33). The actual fit of the measurement data in Section 3.4.1 indicates a dc resistivity greater than $1000 \text{ G}\Omega\text{cm}$ which is above the value calculated in this section.⁴⁷

It can be concluded from the discussion in this section, that silicon-rich low-stress LPCVD nitride offers reasonable dielectric insulation properties on fused silica, which are improved by the high thermal stress level on this substrate material. Additionally, these silicon-rich layers show an increasing resistance to hydrofluoric solutions the higher the silicon content of the layer gets. Such a resistance comes in handy when the silica bulk material needs to be protected during wet-chemical removal of an oxide sacrificial layer. Because of these reasons silicon-rich nitride serves as dielectric insulation as well as wet-chemical protect in the presented pressure sensor process.

importance of low-stress nitride for this work

LPCVD silicon dioxides

LPCVD oxide deposition processes are not influenced by the fused silica substrate solely the as-deposited stress and its evolution during anneal changes (see Fig. 2.9(a) and Fig. 2.10(b)). Important with respect to interpretation of the stress readings, is the high intrinsic stress of these layers (TEOS approximately $300 \text{ MPa} - 380 \text{ MPa}$ [Car02] [Smo85] [Sta92]) and the low density of the as-deposited layers. The latter is attributed to incorporated byproducts from the large precursor molecules⁴⁸ [Sta92] and gives rise to volume shrinkage of $5\% - 9\%$ during preceding thermal anneals (see Fig. 2.22, additional results of two step anneals are summarized in Fig. B.4). The low density renders the layers susceptible to plastic deformation, which can be beneficial, if the layers should act as stress compensation between the fused silica bulk and another highly stress layer such as silicon nitride or re-crystallized amorphous silicon. (The impact of CVD oxide as a floating base layer is highlighted by Fig. 2.12.)

intrinsic stress

density and shrinkage

The densification of CVD oxides need to be considered if these films are used as sacrificial layers. The volume shrinkage is accompanied by the out diffusion of incorporated hydrogen, which is agreed to increase the wet chemical etch rate [Büh97]. That is, annealed sacrificial layers require an up to five times longer processing time depending on the etch solution (refer to Tab. B.17).

usage as sacrificial layer

CVD oxides are, as for the presented sensor the case, commonly used as cavity sealants. Three considerations are important: penetration of the oxide into the cavities during deposition, gas leakage into the sealed cavity due to the low density of the sealant material, and a high number of surface states (i.e. a high charge density) at the sealant-wall interface in case of a silicon cavity.⁴⁹ The very good conformity of LPCVD processes is consequence of the high re-emission rate of adsorbed molecules

cavity sealing

⁴⁷ It must be noted that the calculations of this section are based on the measurement data of [Hab02] and the actual LPCVD processes similar but still not identical. The process conditions affect to a great extend the low field tails and are most likely the reason for the observed deviation.

⁴⁸ TEOS: $\text{SiO}_4(\text{C}_2\text{H}_5)_4$; LTO: $\text{SiH}_2(\text{C}_2\text{H}_5)_2$

⁴⁹ A three times higher surface state density at the oxide-silicon interface for low-temperature SiH_4 -oxide in comparison to thermal oxide has been reported by [Dea68].

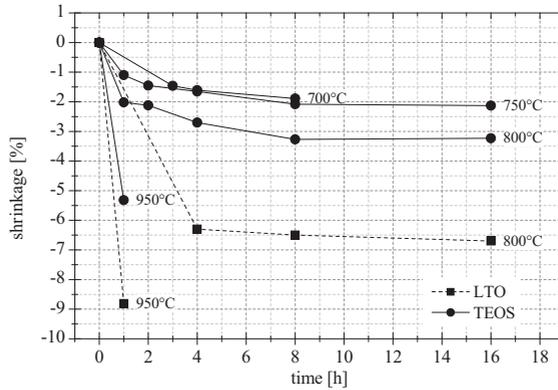


Fig. 2.22: Shrinkage of CVD low- and high-temperature oxide during anneal in N_2 ambient.

prior to their chemisorption on the surface and is discussed in Section 2.3.1.

Un-doped poly-crystalline silicon

Un-doped poly-silicon is not part of the fabrication process of the sensor presented in this work. However, understanding the process of un-doped poly-silicon formation is fundamental to interpret the distinct growth phenomena of in situ boron-doped poly-silicon the sensor transducer material. For this reason, a discussion about un-doped poly precedes the discussion about the doped films. This section intends to highlight the fundamentals of thermal silane decomposition. This process determines the crystallographic structure and the mechanical properties of the deposit. It will become obvious that the presence of additional dopants, like e.g. boron, only accelerate or hinder certain reactions. Therefore, conclusive consequences for the material characteristics can be deduced from basic aspects of the deposition process.

growth regimes

A comprehensive study on the growth of un-doped poly-silicon was elaborated by [Bis86]. It results in two figures necessary for a qualitative description of the deposition by means of SiH_4 pyrolysis (see Fig. 2.23): a pressure-temperature phase diagram and an Arrhenius-plot of deposition rate r_{d-Si} , nucleation rate r_n , and crystallization rate r_c . Layer formation can take place in two regimes dependent on the chosen process temperature T_d :

1. silicon deposition rate is higher than crystal growth rate (right of point A in Fig. 2.23(b))
2. crystal growth rate is higher than deposition rate (left of point A in Fig. 2.23(b))

nucleation

In both cases nucleation takes place at the gas-wafer interface with rate r_n but in the first case the nuclei can not grow fast enough and are buried in the deposit as the layer formation proceeds. The resulting layer is amorphous or semi-crystalline. As

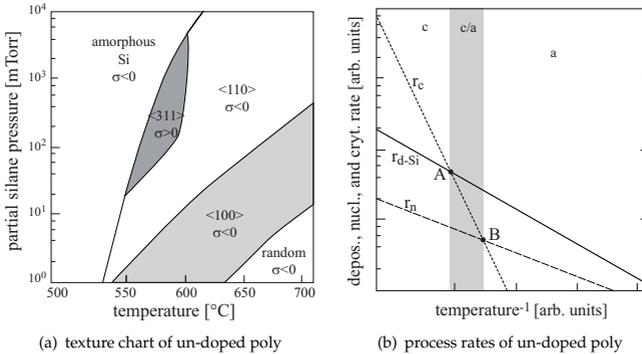


Fig. 2.23: Pressure-temperature phase diagram and deposition and crystallization rate of un-doped poly-silicon. Data for the phase diagram is taken from [Jou89] and [Bis86]. All rates are given in arbitrary units and are not to scale (r_c : crystallization rate; r_n : nucleation rate; r_{d-Si} : silicon deposition rate). The sign of the resulting film stress σ on silicon substrates is also indicated (left picture), along with the crystallization state (right picture, c: fully crystalline; c/a: semi-crystalline; a: amorphous). Point A corresponds to transition temperature T_t .

deposition temperature T_d rises or pressure p decreases, the number of adsorption sites increases, i.e. the number of desorbed hydrogen atoms increases. This in turn increases the surface mobility of adsorbed silicon atoms and promotes the crystal growth.

$$T_d \uparrow, p \downarrow \longrightarrow \text{surface mobility} \uparrow \longrightarrow r_c \uparrow$$

In the regime to the left of point A of Fig. 2.23(b), the mobility is sufficiently high that all silicon atoms are incorporated into the crystal surface and the layer is fully crystalline as-deposited. The temperature at which the growth changes from amorphous to crystalline is referred to as the transition temperature T_t . It is characteristic for a chosen set of process parameters and with impact on the resulting film stress σ as indicated in Fig. 2.23(a). Un-doped poly-silicon is crystalline beyond 600 °C for all applicable process conditions.

Amorphous or partly crystalline deposits can be re-crystallized by means of a subsequent annealing step. Such layers show a characteristic <311> texture in contrast to the prevailing <100> and <110> textures for crystalline as-deposited layers. The change in crystal structure results from two different growth mechanisms associated with the two growth regimes: solid phase recrystallization and crystal growth at the gas-interface. An explanation for the differing textures is found if the directional growth rates for crystalline silicon are considered. Growth in direction <100> is fastest followed by <311>, <110>, and <111>.⁵⁰ The relative difference is related to the number of atoms which are required to complete the crystal lattice on the individual crystal planes, i.e. to create a sixfold ring for silicon (see Fig. B.5 in

⁵⁰ The crystal growth rate ratios are $r_{<100>} = 1.5 \times r_{<311>} = 3 \times r_{<110>} = 25 \times r_{<111>}$ (see [Bis86]).

amorphous
deposition

transition
temperature

texture

the appendix). One atom is necessary on (100) planes, two on (311) planes, again two on (110) planes which must also bond to each other, and three on (111) planes. (311) planes are rather stacked and incomplete (100) planes. Thus, it is illustrative to imagine a $\langle 311 \rangle$ texture as a result of solid phase recrystallization when all buried nuclei grow simultaneously, with highest speed in $\langle 100 \rangle$ direction, finally intercepting each other. As consequence, the texture chart as depicted in Fig. 2.23(a) follows with a $\langle 110 \rangle$ texture, which can only prevail in the diagonal of the chart. Here, process pressure and temperature are in the right ratio to provide a sufficiently high number of silicon atoms at the surface with high mobility. This is necessary to favor $\langle 110 \rangle$ growth during which always to atoms must be add to the existing crystal plane. As pressure decreases the number of sticking silicon atoms decreases and a $\langle 100 \rangle$ texture results. $\langle 100 \rangle$ texture occurs because only one atom is necessary to add another crystal plane. Crystal growth slows down but the adsorbed atoms can travel on the surface due to the higher surface mobility until they meet to complete the (100) face. If pressure is kept unchanged but temperature is decreased, the mobility of the adsorbed atoms decreases. In this case, crystallization rate decreases faster than deposition rate (see Fig. 2.23(b)) and existing nuclei can not grow before they are buried. Either an amorphous or a partially amorphous layer forms. Crystal grain diameters d_c of crystalline as-deposited un-doped poly range typically between 40 nm – 120 nm, increasing with deposition temperature and with decreasing pressure.

$$T_d \uparrow, p \downarrow \longrightarrow d_c \uparrow$$

Amorphous or partially crystalline layers can be re-crystallized. The growth of the buried nuclei differs from the growth during deposition because they must grow within the bulk of the layer. In this case the expansion of the grain is limited by the growth rate of the slowest plane because a minimum surface energy must be maintained. Hence, the recrystallization rate is determined by growth speed in $\langle 111 \rangle$ direction and the density of nuclei. It is concluded in [Bis86] that dangling bonds rather than vacancies are involved in this recrystallization process because of their high number in amorphous silicon. Dangling bonds increase the grain boundary mobility. That is, the higher the concentration of incorporated hydrogen c_H is, the higher will be the number of dangling bonds, and the higher will be the recrystallization rate r_{re-c} . This has important implications for the adjustment of the film stress as will be discussed later.

$$c_H \uparrow \longrightarrow r_{re-c} \uparrow$$

Solid phase recrystallization requires energy and time. A crystalline layer in partly amorphous films can be found at the wafer-layer interface. This part of the deposit was longer exposed to the deposition temperature than the region close to the layer-gas interface and recrystallization already started. The grain size of re-crystallized layers is influenced by the density of nuclei in the deposit, which is proportional to the nucleation rate r_n during deposition. The solid phase crystal growth mechanism changes and slows down at grain impingement when all amorphous silicon is consumed. That is, the higher the nucleation rate r_n during deposition is the smaller

will be the average crystal diameter d_c of the re-crystallized layer and the smoother will be the film's surface.

$$r_n \uparrow \longrightarrow d_c \downarrow$$

Until grain impingement, the recrystallization rate is controlled by the dangling bonds of desorbed hydrogen. A crystal growth beyond this point is referred to as primary grain growth and its rate is again limited by the mobility of the grain boundaries. Differing from the case of recrystallization, the number of dangling bonds becomes negligible and the grain boundary mobility is related to the vacancy density within the grains. Diffusion takes place due to individual atoms crossing the grain boundaries with a probability proportional to the vacancy density of the neighbor grain. Vacancies result from atoms which have left their lattice site due to thermal excitation. Dopants on substitutional sites increase the probability of the occurrence of such an abandonment. The process is very similar to the thermal excitation of charge carriers. For this reason, the density of vacancies is modeled to depend in a similar way on fermi level and temperature as the carrier density does [Sze85]. That is, an intrinsic density of vacancies can be increased due to an increase of temperature as well as by addition of *both* types of dopants. This has important implications for the modeling of grain growth of doped poly-silicon layers. The growth kinetics can be described with equation [Kim88]

$$d_c = \sqrt{C_f E_{gb} M t + d_{c_0}^2} \quad (2.36)$$

where M denotes the vacancy dependent grain boundary mobility and d_{c_0} the initial grain diameter. Equation (2.36) was originally derived to describe secondary grain growth (see below) in poly-silicon, but can also serve to provide qualitative information for primary grain growth. It can be seen that grain sizes obey a \sqrt{t} -law which is influenced by the average grain boundary energy E_{gb} and C_f representing a constant relating E_{gb} to the driving force of grain growth.⁵¹ The grain boundary mobility can be expressed as

$$M = M_0 \exp(-E_A/kT) \quad (2.37)$$

where M_0 is an pre-exponential coefficient and E_A the apparent activation energy which is a function of the vacancy density mentioned above. It follows that primary crystal growth can be effectively influenced by doping and will be discussed in the preceding section. Primary crystal growth requires more energy than solid phase recrystallization and, as consequence of (2.37), the resulting grain size can be effectively controlled by the chosen annealing temperature. The shape of the crystals tend towards the minimum of total surface energy which is assumed to be achieved if the crystal lattice is perfect and the faces are complete. Therefore, the larger the grains become the higher will be the required energy to add an additional complete layer to the grain. Hence, the final grain diameter, which is achievable during an asymptotic anneal is proportional to T_a . A stable equilibrium grain outline is

⁵¹ Details on the origin of surface energy and illustrative explanations can be found in [Spa00] and [Nix01].

primary grain
growth

grain growth
dynamics

grain boundary
mobility

reached if the total surface energy of the grain is minimal (grain shape) at a level corresponding to the provided thermal energy (grain size) (see e.g. [Bis86]). Important to note is also the possibility of slow, asymptotic anneals due to the square root in (2.36).

$$T_a \uparrow \longrightarrow d_c \uparrow$$

impact of the base layer

A further implication of the described concept is that grain growth on surfaces with differing surface energies leads to crystal structure variations. A crystalline growth on silicon oxide surfaces e.g. results in a columnar structure which does not occur in case of growth on silicon. This is caused by the lower surface energy of the silicon oxide which results in the formation of islands at the very beginning of the growth process [Bis86]. The islands with the fastest growing crystal planes oriented normally to the wafer surface overtake their slower neighbors and cause a columnar structure with a $\langle 100 \rangle$ or $\langle 220 \rangle$ texture. It is important to note the impact of the underlying surface on the crystalline structure of the deposit and its impact on layer stress and stress measurement (see also Section 2.2).

secondary grain growth

A lateral growth is started, called secondary grain growth, if films with a texture of fast growing crystal directions are further annealed. Similar to primary grain growth, fast faces have the advantage over the slower, but growth direction is now parallel to the wafer surface changing the film's texture finally to $\langle 111 \rangle$, because the fast $\langle 100 \rangle$ faces are now oriented in parallel to the wafer surface (see e.g. [Elb98]).

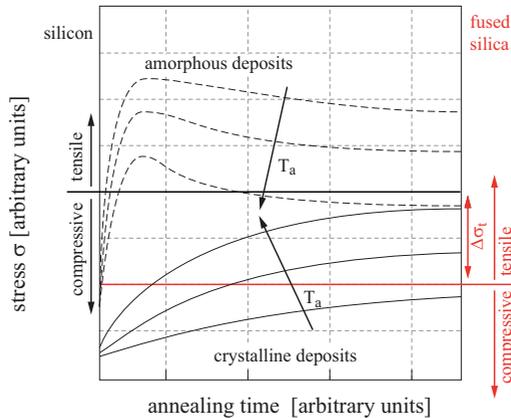


Fig. 2.24: Total stress σ of un-doped poly-crystalline silicon after deposition and anneal. The general annealing characteristics were reported by [Guc88] and are in good agreement with the results of this work. The magnitude of stress on fused silica is shifted towards higher tensile stress levels due to the increase of the thermal component.

film stress

The as-deposited film stress σ is found to be compressive for fully amorphous layers as well as fully crystalline deposits. A $\langle 311 \rangle$ texture and either tensile or

low compressive stress may result after layer formation in the transition regime. Amorphous deposits get tensile during anneal and crystalline films remain compressive at decreased magnitude. Fig. 2.24 illustrates the general annealing characteristics of poly-silicon as reported by [Guc88]. These are found to be in very good agreement with the results of this work (see also Fig. 2.9(b), Fig. 2.14, Fig. 2.11, and Fig. 2.13). The TEC of amorphous poly-silicon is smaller than the TEC of silicon. This explains the compressive total stress of amorphous as-deposited layers at room temperature which is dominated by the thermal stress component. The TEC of crystalline poly is close to that of bulk silicon and does not contribute much to the total layer stress. During formation of crystalline as-deposited layers atoms diffuse along defects which are found in large numbers at the grain boundaries. These atoms, which force themselves between the boundaries of two crystallites, remain there and are responsible for a resulting compressive intrinsic stress of crystalline poly-silicon. Thus, the magnitude of compressive stress of crystalline layers correlates with the density of grain boundaries. That is, the larger the grains become the lower will be the magnitude of compressive stress in the deposit. The low TEC of fused silica increases the thermal stress component and poly-crystalline as-deposited films can become tensile as indicated by the red line in Fig. 2.24. If amorphous layers are annealed, excess hydrogen is driven out of the deposit and dangling bonds link to each others. The layer shrinks resulting in stretched bonds which render the total stress tensile. The higher the annealing temperature is chosen the lower will be the resulting tensile stress until it becomes compressive when primary grain growth is completed. In both cases, annealing temperature T_a and crystal diameter d_c are inversely proportional to the magnitude of intrinsic stress.

$$T_a \uparrow, d_c \uparrow \longrightarrow |\sigma_i| \downarrow$$

Besides the stress, also the mechanical strength of the deposit can be related to its morphology. According to [Cha69], the applied mechanical stress, which is required for plastic deformation increases with decreasing grain diameter. Furthermore, it can be shown that a stress level below a certain limit (for a certain grain size) does not cause any plastic deformation within a grain. *Chaudharis* concluded that the plastic deformation of grain boundaries obeys a similar law and are therefore also not likely to occur if stress levels remain under a certain limit. Sliding of grain boundaries may take place but is suspected to be slower than diffusion creep. All of these effects scale inversely with the average grain size rendering fine grained films the most robust. However, it is necessary to calculate the local stress within layer and substrate to assess the actual probability of plastic deformation. An estimate for the stress distribution over the layer depth can be found in Appendix B.1.4. Actual measurement data for the yield stress of poly-silicon is given e.g. by [Kam04]. They found in agreement with [Cha69] the highest strength of 2.35 GPa for fine-grained samples (i.e. amorphous silicon deposited at 560 °C which was annealed at 850 °C).⁵²

yield strength

The oxidation of poly-silicon or oxygen penetration into it can become a concern

⁵² A similar yield stress magnitude is expected for the transducer layer of this work (PBOR560BT, in situ boron-doped poly). The high yield strength in this special case is related to the fine-grained *as-deposited* morphology of in situ boron-doped layers.

Table 2.6: Oxygen penetration depth into bulk silicon and poly-silicon. Bulk diffusion depth was calculated with (2.38) and $d = \sqrt{Dt}$. The poly depth was estimated to be 4/3 of the bulk value based on oxidation data given by [Bou96].

temperature [°C]	time [h]	diffusivity [cm ² /s]	depth (bulk) [nm]	depth (poly) [nm]	equivalent thermal budget
450	6.9	3.35×10^{-19}	0.1	≈ 1.2	1.2 μm LTO
705	2.5	1.39×10^{-14}	112	≈ 149	1.2 μm TEOS
800	6.0	2.00×10^{-13}	656	≈ 876	≈ 15 nm dry oxide
900	1.0	2.08×10^{-12}	865	≈ 1153	≈ 15 nm dry oxide

oxidation of and
diffusion into
poly-silicon

during MEMS fabrication. Insulation layers of thermal oxide may need to be grown on a poly-silicon structure or high temperature CVD oxides have to be deposited or annealed in oxygen ambient. Oxygen can diffuse into single crystal silicon not necessarily reacting chemically with it. This diffusion process is accelerated if grain boundaries are present. For example, asymptotically annealed tensile poly-silicon pressure sensor plates (200 MPa, PBOR560) covered with a thin TEOS layer and annealed in nitrogen atmosphere, became compressive and remained in this state even after wet-chemical TEOS removal. Other researchers have observed similar phenomena, like e.g. [Mas90] who reported the initially tensile stress of a heavily boron-doped single crystal silicon membrane to change to compressive upon oxidation and moreover to develop a negative stress gradient. *Maseeh* et al. attributed this to a possible plastic deformation of the silicon at the oxide interface based on calculations made in [Jac66]. Their calculations indicate that thermal oxide could exert sufficient stress to cause dislocations and hence plastic deformation of the silicon if grown on thin plates. Although possible, this explanation is not able to explain the reversibility of the observed stress and stress gradient change as documented by [Für99]. *Fürtsch* et al. compared the effects of nitrogen and oxygen ambient during anneal on thick poly-silicon. Whereas annealing in nitrogen lead to the expected decrease of the compressive stress (see Fig. 2.24) whereas oxygen showed the opposite effect. Additionally, the changes of stress were reversible canceling out a possible plastic deformation caused by thermal mismatch. Reversible diffusion of oxygen into the silicon and out of it is given as explanation. The reported diffusion constant for oxygen in silicon within the temperature range of 330 °C–1240 °C was determined to be [Sta83]

$$D = 0.17 \text{ cm}^2/\text{s} \exp \left[\frac{-2.54 \text{ eV}}{kT} \right]. \quad (2.38)$$

This results in a considerable penetration depth of approximately $\sqrt{Dt} = 112$ nm during 2.5 h in oxygen ambient at 705 °C, a thermal budget which corresponds to the formation of 1.2 μm TEOS oxide.⁵³ The estimated oxygen penetration for the

⁵³ Extensive data on oxygen diffusion is also summarized in [Gös82].

relevant cases of this work is summarized in Tab. 2.6. As pointed out before, the diffusion constant increases with the number of grain boundaries promoting diffusion along their defects. That is, oxygen penetration may have a significant impact on the transducer stress. This is especially the case for the often implemented fine grained poly-silicon transducer films (additional information for the case of in situ boron-doped poly is provided in the next section).

In situ boron-doped poly-crystalline silicon

In situ boron-doped poly-silicon was chosen as functional layer for this work. This section is intended to collect useful information to develop an illustrative understanding of the deposition process and the resulting material properties. It's extent is due to three reasons: no comprehensive literature is available on in situ boron doping, the process involves complex physicochemical phenomena, and an improved understanding leads to time saving in conjunction with an increased fabrication yield. Table B.12 in the appendix presents an overview of literature sources related to in situ boron-doped poly-silicon which are considered to be a good starting point for further reading. Although processing condition vary greatly in the cited publications, even precursor types are not identical, the characteristic aspects of in situ boron-doped poly-silicon films remain. The acquired data in course of this work agrees well with literature and reported findings are believed to apply even if process condition differ. Nevertheless, much more experimental work must be carried out to verify the sometimes hypothetical interpretations.

In situ boron-doped poly-silicon offers a number of advantages in comparison to standard implantation or diffusion doped poly-silicon films:

advantages
of in situ
boron-doping

- The doping profile is homogenous at a very high dopant concentration level close to the solid solubility.
- A homogenous crystal structure results and in consequence a low stress gradient is caused by in situ doping with boron.
- Deposited layers are under a very high compressive stress on silicon due to their fine grained structure. Therefore, the stress can be adjusted to be low and tensile on silica.
- Boron-doped films can make good electrical contacts to aluminium (which is also a p-type dopant) without forming *Schottky* barriers.
- Poly-silicon with a high concentration of boron exhibit an improved corrosion-resistance to alkaline ambient [Sta03].⁵⁴
- A high surface quality with a very small roughness is caused by the fine crystalline structure at high doping levels.
- The typical fine-grained morphology of poly-crystalline as-deposited layers leads to a high yield strength (see Section 2.3.1).

⁵⁴ Stark et al. observed that poly-silicon corrodes at ambient temperature if exposed to phosphate buffered saline (an alkaline solution to model body fluids like sweat or blood) [Sta03]. The rate of poly-silicon dissolution decreased orders of magnitude after boron implantation comparable to the rate reduction at boron etch-stops during anisotropic etching of silicon.

- A very good, near perfect step coverage and dopant homogeneity even if very high aspect ratio features like deep trenches and vias are filled [Gri02]
- The crystalline structure of in situ boron-doped poly-silicon is thermally more stable than n-type or un-doped poly-silicon [Cau04].

disadvantages
of in situ
boron-doping

Besides these motivating aspects serious difficulties exist, which are related to the special kind of LPCVD process. In this work, in situ boron-doped poly was deposited by means of pyrolysis of silane (SiH_4) and diborane (B_2H_6). Process control is challenging for the following reasons:

- Multiple precursor LPCVD processes are in general more difficult to control because of their interaction and depletion within the reactor.
- The crystallinity of the deposit increases the complexity of the process model in comparison to amorphous layers like silicon nitride.
- Parameters of the deposited layer strongly depend on the decomposition of the boron precursor which influences the involved reactions in a sensitive way. Therefore boron concentration fluctuation leads to an inherent process inhomogeneity.⁵⁵
- Diborane with its strong influence on the deposition dynamics is not stable at room temperature [Air06]. It decomposes to higher boranes rendering long-term process control difficult.

diborane
diluted in
silane

Usually process control requires the supply of diluted diborane. During this work, a mixture of $\text{B}_2\text{H}_6/\text{SiH}_4 = 1/10$ was used and is believed to introduce additional process variations. The diborane itself is meta-stable and decomposed to higher boranes.⁵⁶ In silane, a decomposition of up to 30 % during the first year and 50 % during the first two years after mixing must be expected [Air06] (see also Fig. B.6 in the appendix). A possible solution to overcome these problem could be the dilution of B_2H_6 in H_2 which stabilizes the diborane.⁵⁷

The precursor decay must be expected to have an impact on the LPCVD process. Observed long-term deposition rate changes, as depicted in Fig. 2.25, show a markedly increase of the deposition rate during the first year. The rate drops again significantly when the precursor gas is supplied from a freshly filled bottle. In addition, long-term changes of the layer characteristics suggest an increasing boron incorporation within the deposit over time.⁵⁸ A proven explanation can not be given, but influences of other reactor components can be ruled out, i.e. changes of the reactor tube or mass flow controllers (see Fig. 2.25) leaving the precursor gas as origin for the observed changes.⁵⁹ Three mechanisms may exist which could explain the

⁵⁵ The distinct inhomogeneity can be lowered by means of gas injector tubes as already stated in early literature (see e.g. [Mar88]), but a rigorous explanation of the origin of this problem is not available.

⁵⁶ Borane hydrogen compounds are called boron hydrides. They appear in the following forms: closo- B_nH_n^2 , nido- B_nH_{n+4} , archo- B_nH_{n+6} , hypo- B_nH_{n+8}

⁵⁷ Literature sources using this special precursor mixture do not report about stability issues [Jou89] [Haj89].

⁵⁸ Long-term observations over three years are: increasing deposition rate, increasing compressive stress, and a decreasing resistivity.

⁵⁹ Replacement of quartz tubes and the thickness of the deposit on the reactor walls have a minor impact on the process. Mass flow controllers either work well or brake down completely.

observations: separation of the individual boranes in the gas lines from the source bottle to the reactor,⁶⁰ sedimentation of the boranes within the gas bottle, or an increased thermal decomposition rate of the higher boranes in the reactor. The molar mass of boranes increases with their molecular size. Diborane has a lower molar mass of 27.67 g/mol than silane with a mass of 32.21 g/mol. This ratio inverts for higher boranes. Therefore, the hypothesis of an increasing boron/silane ratio of the gas supply caused by sedimentation seems unlikely. Gas injector tubes are required for homogeneity improvement. In this work, the diborane mixture was supplied at the reactor door and injected in the middle reactor load. Therefore the precursor needed to travel approximately 1.5 m through the small injector tube being in direct contact to the hot reactor wall. Dependent on the chosen gas flow, it took 3 sec – 8 sec for the gas to travel the injector possibly heating-up and partly decomposing during this time. This may allow higher boranes to get in higher concentrations into the reactor since they are thermally *more* stable.⁶¹

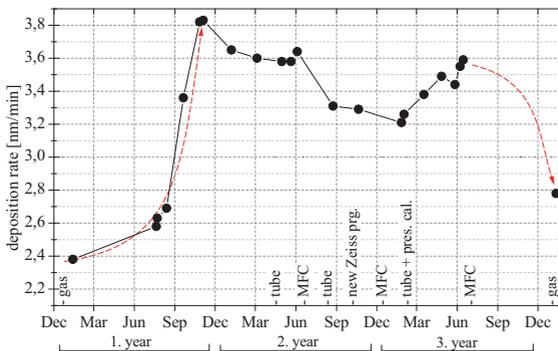


Fig. 2.25: Long-term evolution of the in situ boron-doped poly deposition rate (diborane/silane precursor mixture). Important events are marked at the bottom axis (gas: new diborane/silane bottle connected, MFC: mass flow controller changed, tube: furnace tube changed, pres. cal.: vacuum pressure gauge calibrated, new Zeiss prg.: optical parameters changed for interferometric thickness measurement).

The following observations can be found in publications independent of the process conditions and adopted gas mixtures:

**prominent features
in situ boron-doping**

1. an increase of the poly-silicon deposition rate when boron is introduced into the process which saturates at a certain level
2. a low uniformity over the reactor load, i.e. a significant drop of the deposition rate along the reactor and a bad uniformity over the wafer
3. a decrease of the amorphous/crystalline transition temperature T_t

⁶⁰ Long gas lines may act as a gas chromatographic column and a separation of molecule groups with differing masses could occur.

⁶¹ As a general rule, higher boranes show an increasing stability but there are also exceptions to the rule and some decompose readily [Wik07].

4. a very high crystallinity of the deposit, i.e. very small crystals even if deposited at higher temperatures
5. a crystal growth at the deposit-gas interface
6. a high thermal stability of the layer, i.e. significant morphological changes of crystalline deposits can only be achieved at high annealing temperatures

The observations have been confirmed in course of this work and will be discussed throughout the proceeding paragraphs.

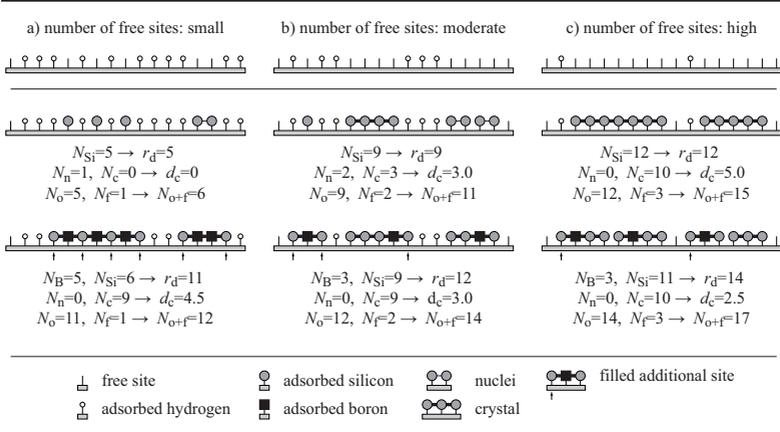


Fig. 2.26: Comparison of boron and silicon adsorption at different densities of adsorption sites for the cases of un-doped and boron-doped poly-silicon deposition. (N_{Si} : number of adsorbed silicon atoms; N_B : number of adsorbed boron atoms; r_d : deposition rate; N_n : number of nucleation bonds; N_c : number of crystal bonds; d_c : average grain diameter; N_o : number of occupied sites; N_f : number of free sites; N_{o+f} : total number sites)

It is important to note that the presence of boron during the crystal growth of poly-silicon does not change the general aspects of poly-silicon deposition as described above. All the sometimes puzzling observations boil down to the understanding of the interplay of boron and silicon during adsorption and its dependence on the individual processing parameters.⁶² Fig. 2.26 visualizes the influence of adsorption site density on the deposition of un-doped and in situ boron-doped poly-silicon and highlights the impact of boron on the deposition. Three illustrative cases can be distinguished where the number of free sites is a function of process pressure and temperature and :

- a) number of free sites: small

un-doped: The few adsorption sites are almost all occupied. The surface mobility is low due to the small number of free sites. Nucleation and crystal

⁶² Gas phase reactions of the boron precursor with silylene (SiH_2) are not believed to be relevant [Fre95].

growth rate are proportional to the surface mobility because side by side sites are required for mating. Hence, no crystal growth is possible and few nuclei can form.

boron-doped: If boron is added it adsorbs primarily, the small islands of desorbed hydrogen are enlarged and bridged by the boron which weakens the strength of surrounding hydrogen bonds [Fre95] [Gri02]. The weakened bonds in the vicinity of adsorbed boron atoms increase the overall number of surface sites, thus promoting nucleation, crystal growth and result additionally in an increase of adsorbed silicon atoms. The crystal size is large due to the high concentration of boron and the resulting high surface mobility.

b) number of free sites: moderate

un-doped: Small islands of desorbed hydrogen occur. Surface mobility and deposition rate increase due to a larger number of un-occupied sites. Crystal growth starts and nucleation is promoted.

boron-doped: The number of thermally generated surface sites and adsorbed boron atoms is inversely proportional. Therefore, as desorption of hydrogen increases also desorption of boron increases and the number of sticking boron atoms decreases. Additionally, boron can create only extra free sites if an atom is adsorbed at the edge of an island or on an isolated site. Hence, the number of additional adsorption sites decreases. Accordingly, the deposition rate enhancement also drops. The surface mobility, which is proportional to the boron concentration, is lowered. The number of individual crystallites, which can not mate, increases and the average crystal sizes decreases.

c) number of free sites: high

un-doped: Many free sites exist and the surface mobility is very high. All adsorbed silicon atoms can form crystal bonds on their way over the surface and no new nuclei develop.

boron-doped: The boron concentration in the layer stabilizes because the increase of thermally generated sites compensates the increase of the boron desorption rate, i.e. the boron incorporation rate may increase again proportional to T_d . The number of additionally generated sites becomes negligible because thermally generated adsorption centers dominate. Surface mobility is very high and all atoms can travel over the surface to their preferred bonding site. That is, boron spreads out homogeneously because of the limited solid solubility and act as nuclei during the simultaneous grain growth of a high number of crystallites. Impinging crystallites do not mate during the deposition after they have gained a certain size, because of the limited thermal energy and the inhibiting action of boron on the grain boundary mobility. The resulting deposit is very fine grained at low level of incorporated dopant.

This illustrative model explains: rate enhancement, fine grained structure, decreasing grain size with increasing process temperature (in situ boron-doped), increasing grain size with increasing process temperature (un-doped), transition of boron incorporation rate, resistivity and the general issue of inhomogeneity which is influenced by hydrogen and HCl within the reactor.

Nucleation during in situ boron-doped poly deposition takes place at the poly-gas interface as reported by [BD91]. The addition of boron leads to a significant

increase of the nucleation and deposition rate. A roughly doubled deposition rate is reported in [Mar88] after raising the the B_2H_6/SiH_4 precursor ratio from 0 to 30×10^{-3} . Deposition rate saturation was observed at three times the un-doped rate and a BCl_3/SiH_4 ratio of 2.5×10^{-3} [Fre95]. The reported rate changes are explained by assuming the adsorbed boron atoms, having a low electronegativity [Gri02], to lower the chemical strength of the surrounding Si-H surface bonds [Fre95]. Therefore adsorbed boron increases the probability of silane chemisorption in their vicinity and enhances the silicon deposition rate r_{d-Si} . As in un-doped depositions, nucleation rate r_n increases if the surface mobility of adsorbed atoms increases. The latter is proportional to the number of free surface sites. As conclusion, boron enhances the deposition rate and nucleation rate at the same time by weakening the Si-H bonds. Figure 2.26 illustrates that the rate enhancement for the case of scarce adsorption sites is more pronounced, i.e. for lower deposition temperatures and higher partial pressures of hydrogen and silane. The hypothetical model of weakened hydrogen bonds by adsorbed boron is in good agreement with further observations:

- The rate change is independent on the type of boron precursor (B_2H_6 , BCl_3).
- Resistivity and deposition rate drop along the reactor load if no injectors are used.
- Deposition rate and boron concentration within the deposit saturate simultaneously when the boron/silane ratio is increased.
- n-type dopants have an opposite action on the deposition rate.⁶³

General feature of in situ boron-doped poly-silicon growth is a lowered apparent activation energy in comparison to the un-doped process resulting in a rate enhancement and a weaker temperature dependency of the deposition. This can be observed in Fig. 2.27 showing a comparison of *Arrhenius*-plots of un-doped and in situ boron-doped processes. The measured activation energy of $E_A = 1.39$ eV (in situ boron-doped, B_2H_6/SiH_4 ratio of 6.29×10^{-3}) and $E_A = 1.67$ eV (un-doped) agree with the trend described in literature⁶⁴ and is close to the lower limit of the commonly given range for un-doped poly of 1.4 eV to 1.7 eV [Mar88].



Prominent feature of in situ boron-doped poly is a lowered transition temperature T_t , i.e. a lowered onset of crystal growth. Crystalline depositions down to 520 °C are feasible and are reported by all authors summarizes in Tab. B.12. As stated before, the deposition and nucleation rate is promoted by adsorbed boron at the wafer-gas interface. That makes the transition temperature inversely proportional to the boron

activation energy

transition temperature & morphology

⁶³ A rate reduction by a factor of two for phosphorous and a factor of five for arsenic in situ doping of poly-silicon is reported in [Eve73].

⁶⁴ An E_A of 1.25 eV for a B_2H_6/SiH_4 ratio of 5×10^{-3} is reported in [Haj89] (see Fig. B.7(a)). Activation energies of 1.0 eV and 0.2 eV for crystalline and amorphous depositions were measured in [Mar88].

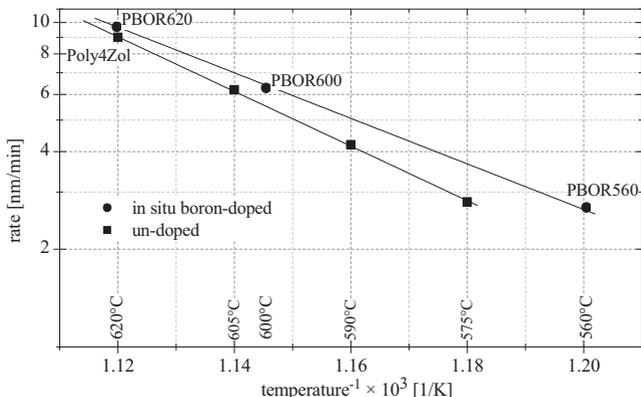


Fig. 2.27: Deposition rate versus deposition temperature of un-doped and in situ boron-doped poly-crystalline silicon. Full lines represent *Arrhenius* fits (un-doped: $r_0 = 2.41 \times 10^{10}$ nm/min and $E_A = 1.67$ eV; boron-doped: $r_0 = 7.049 \times 10^8$ nm/min and $E_A = 1.393$ eV). The diborane/silane ratio was fixed to 6.29×10^{-3} . Data of un-doped poly deposited below 620 °C is taken from [Elb98] whereas data at 620 °C corresponds to parameter set Poly4Zol.

concentration within the deposit c_B .

$$c_B \uparrow \longrightarrow T_t \downarrow$$

A change of activation energy is expected at T_t as observed by [Mar88]. The constant E_A measured between 620 °C and 560 °C (see Fig.2.27) indicates a crystalline deposition within the tested temperature range.⁶⁵ The change of apparent activation energy at T_t was not observed by groups working with H_2 diluted precursors (see [Haj89] and Fig. B.7(a)). An explanation would be that the hydrogen in the source gas ([Haj89]: $B_2H_6/SiH_4/H_2$) lowered the impact of film morphology changes on E_A . That is, the hydrogen partial pressure is not changed significantly by the excess H_2 from the chemical decomposition within the reactor if hydrogen is used as carrier gas. This implication is important because the H_2 partial pressure also influences the density of free surface sites. Therefore, fluctuations of hydrogen partial pressure over the reactor load can be correlated with the inherent process inhomogeneity associated with the gas mixture B_2H_6/SiH_4 (see further below in this section). This is supported by the strong deposition rate decrease caused by hydrogen introduction into the reactor which was observed during this work.

influence of hydrogen

The crystallographic structure of in situ boron-doped poly-silicon was analyzed with respect to deposition temperature and silane partial pressure by [Jou89]. Texture charts for un-doped and boron-doped films based on these results are shown

texture

⁶⁵ The transducer plate material (short name: PBOR560) of the presented sensor was crystalline deposited with a diborane/silane ratio of 6.29×10^{-3} at 560 °C.

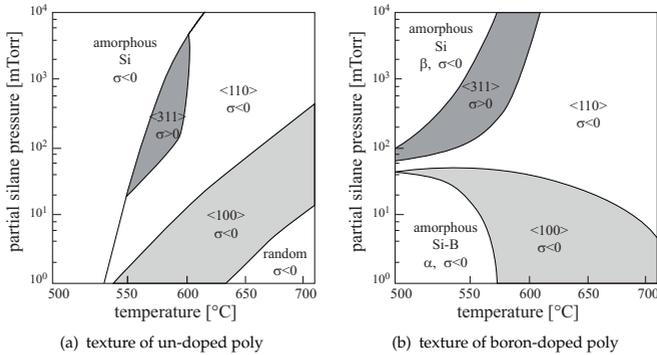


Fig. 2.28: Texture versus temperature charts of un-doped and boron-doped poly silicon in accordance to [Jou89] (misleading data due to transport limited depositions have been omitted). The boron/silane ratio of the $B_2H_6/SiH_4/H_2$ gas system was fixed to 5×10^{-3} . α and β indicate amorphous silicon with either high (Si-B compound) or low boron concentration, respectively.

in Fig. 2.28 (interpreted with additional information provided by [Haj89]). Some characteristic features can be identified:

- existence of an as-deposited crystalline regime down to 500 °C
- occurrence of an amorphous Si-B compound at low T_d and low p_{d-Si}
- broadening of the <110> texture regime in comparison to the un-doped case.

The promotion of crystal growth by adsorbed boron can be noted leading to very low transition temperatures. <100> texture is characteristic to occur at low crystal growth rate to silicon adsorption rate ratios. As the silicon adsorption rate increases, e.g. by increase of silane partial pressure, the texture changes to <110>. In the case of in situ boron-doped silicon, the silicon adsorption rate is strongly influenced by the boron incorporation rate which *decreases* with increasing temperature. As consequence, texture transition does not take place along the diagonal of the texture chart, but turns clockwise in dependence on the diborane flow (more precisely following the boron incorporation rate).⁶⁶ Deposits of this work processed with parameter-sets PBOR560 and PBO560BT had a <311>/<110> texture which occurs for crystalline deposits close to the transition regime (see Fig. 2.28(b)).⁶⁷ The <311> texture is characteristic for solid phase recrystallization [Bis86] which took place during layer formation in course of this work.

In situ boron-doped poly-silicon films have a very smooth surface in comparison to un-doped crystalline deposited layers. This can be explained by the small size

⁶⁶ Refer to the boron incorporation rate given in Fig. B.7(c), which corresponds to the textures given in Fig. 2.28(b).

⁶⁷ The texture was deduced from the layer characteristics: PBOR560 and PBO560BT layers are highly compressive, are stable up to high annealing temperatures, and their resistivity depends strongly on deposition temperature (compare to Fig. B.7(d) and Fig. 2.32).

of the crystalline grains which nucleate proportional to the number of incorporated boron atoms. This is, the higher the diborane/silane ratio is set the higher will be the number of crystallites and the lower will be their average size. Reported grain sizes vary between 80 nm and 40 nm within the relevant temperature range (see [Bou96], [BD91], [Jou89]). Authors agree by stating a grain size decrease with increasing deposition temperature (grain sizes were deduced from TEM photographs) and no observed grain growth during deposition. This is in agreement with the model illustrated in Fig. 2.26 (transition from a small to a moderate number of free surface sites). Some researchers reported an enlargement of crystallite sizes from the wafer-interface to the top of the layer [BD91]. The observed very small crystals of 5 nm–10 nm at the beginning of growth are in agreement with a peak in c_B in the same layer region [Haj89]. This is also in accordance with the observed positive stress gradient of the crystalline as-deposited layers of this work. No explanation is given for the preferential adsorption of boron during the initial phase of growth.

A general trend of decreasing boron incorporation at increasing deposition temperature is observed (see Fig. 2.32) in agreement with literature. It is attributed to a rising boron desorption with deposition temperature. Additional insight is gained if the incorporation rate $r_d \times c_B$ is considered measuring the atoms per unit area and unit time. It gives information on the stiction of a reactant species. The difficult process control of in situ boron-doping is stressed by the reported trend changes of boron incorporation rate with consequences for the silicon deposition rate and crystal growth. The boron incorporation rate $r_d \times c_B$ changes its trend at a certain critical process temperature T_c (see Fig. B.7(c)). This alteration is either due to an approached solid solubility (at low deposition pressure) or due to change of the free surface site density (at high deposition pressure). As illustrated above, the boron adsorption decreases with increasing temperature, i.e. boron desorption increases, but also hydrogen desorption increases simultaneously with a higher rate. That is, the net higher number of free surface sites leads at T_c again to an increase of the boron incorporation rate (although this does not change the general decline of c_B in the layer). This model is in agreement with the observable increase of T_c if process pressure is increased (see Fig. B.7(c)).

Boron can be incorporated at levels well above the single crystal solid solubility corresponding to the individual process temperature (see Fig. B.8 and Tab. B.13 for the solid solubility of boron). A possible explanation is the formation of an amorphous Si-B compound as proposed by some researchers [Haj89]. It occurs primarily at low deposition temperature and pressure, but it may also be found in lower volume fractions at other deposition conditions. Actual values for the boron concentration of films fabricated in course of this work have not been measured. Literature values for in situ boron-doped layers are: $2.5 \times 10^{21} \text{ cm}^{-3}$ @555 °C [Fre95], $2 \times 10^{20} \text{ cm}^{-3}$ @520 °C–605 °C [Bou96], and $5 \times 10^{17} \text{ cm}^{-3}$ @625 °C [Haj89].

In situ boron-doped processes show a distinct inhomogeneity of the deposition rate, resistivity, and film stress along the reactor load. Therefore, reactor are commonly equipped with injector tubes. Depletion of boron along the reactor load as the only reason can be ruled out. The inhomogeneity can be reduced, but remains even for high boron supply rates [Fre95]. The cause for this process feature is most likely the combined action of silicon deposition rate enhancement in the presence of

incorporation rate &
boron incorporation

boron concentration

inhomogeneity

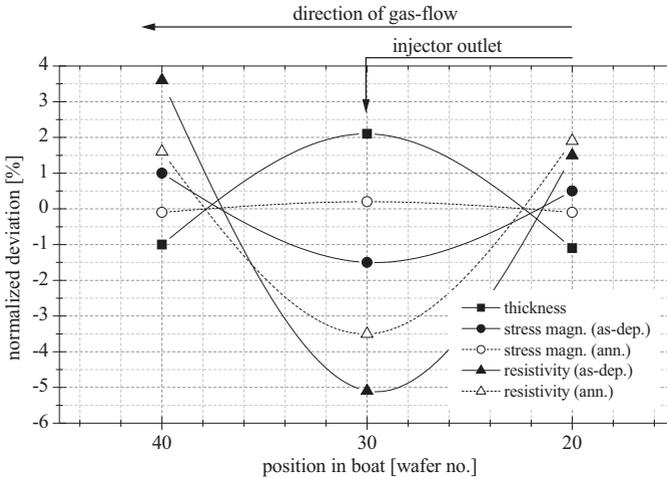


Fig. 2.29: Representative inhomogeneity of thickness, stress, and resistivity of in situ boron-doped poly-silicon (747 nm, -534 MPa, 7.0 m Ω cm, PBO560BT). Values are normalized to the average of the whole furnace load. Annealing took place in nitrogen ambient for 12 h at 775 °C (-401 MPa, 10.3 m Ω cm). Outlet of the gas injector is located at boat position 30. No noticeable thickness change during anneal can be observed for the depicted as-deposited crystalline layer.

boron and the competition of boron with other reaction byproducts adsorbed on the wafer surface. A markedly decrease of the deposition rate in presence of H_2 or HCl is reported and concluded to lower the boron adsorption rate [Fre95]. A representative example of this work is given in Fig. 2.29. It shows a pronounced decrease in resistivity as well as an increased deposition rate at the injector tube outlet. The stress distribution over the reactor is also related to the position of the injector, but is within the expected error of measurement caused by erroneous thickness readings.

Figure 2.30 illustrate and summarizes the fundamental processes involved during in situ boron-doped poly formation as discussed so far. The *Arrhenius*-plots are not to scale, but show general trends including: silicon deposition rate r_{d-Si} enhancement, shift of transition temperature T_t (point A), shift of in situ recrystallization temperature (point B), temperature dependency of boron concentration c_B , and shifts of nucleation rate r_n and crystallization rate r_c . The distinct influence of boron is highlighted by a comparison to un-doped poly-silicon.

An interpretation of the layer conductivity must include the influence of boron concentration and the layer morphology. The general rule

$$c_B \uparrow \leftarrow \sigma_{pSi} \uparrow$$

as observed e.g. by [Mar88], [Haj89] and this work (see Fig. 2.32) holds for many cases, but a model is required for a better understanding of the distinct electrical

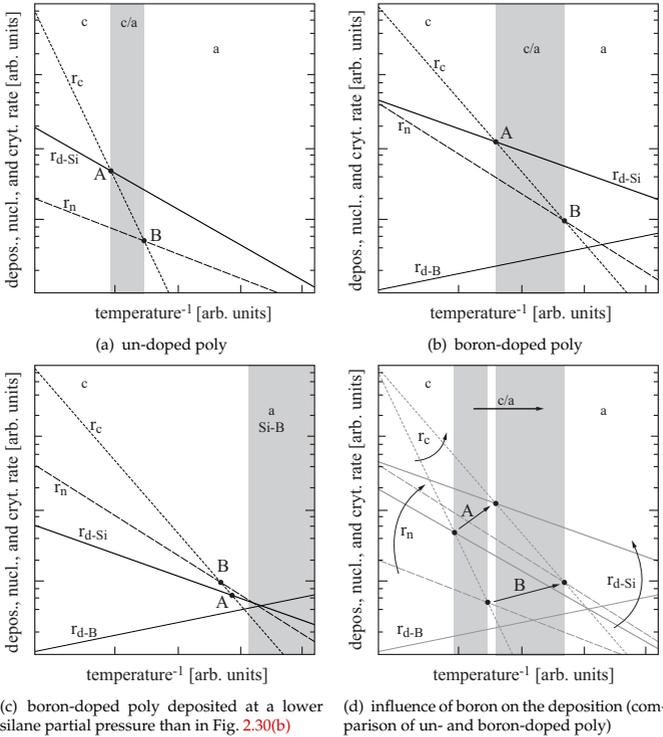


Fig. 2.30: Deposition-, nucleation-, and crystallization rate comparison of un-doped and boron-doped poly-silicon (r_{d-Si} : silicon deposition rate; r_{d-B} : boron deposition rate; r_n : nucleation rate; r_c : crystallization rate; c: crystalline regime; c/a: partially crystalline regime; a: amorphous regime; Si-B: silicon boron compound; A: transition to crystalline deposition; B: start of crystallization.)

behavior of doped poly. A one-dimensional model as suggested in [Set75] and is presented here (see Appendix B.2.5 for the full set of equations). It is based on the experimental findings of: an initially decreasing carrier mobility with increasing dopant concentration followed by a sharp collapse after which the mobility starts to increase again with increasing dopant concentration [Set75].⁶⁸ This can be understood if the conductivity σ_{pSi} is considered in analogy to conduction in crystalline silicon but with the difference that average carrier concentration \bar{p} and the effective

⁶⁸ The results and model are in agreement with the observed resistivity changes during thermal treatment reported by [Bou96] if the annealing kinetics of poly-silicon are considered.

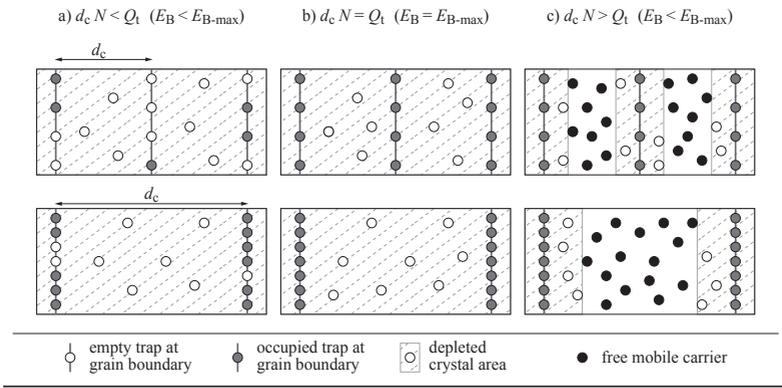


Fig. 2.31: Mobile carrier concentration in doped poly-silicon films. The number of free carriers depend on grain diameter d_c , dopant density N , and trap density Q_t . The height of the energy barrier E_B at each grain boundary rises with the number of trapped carriers and width of the depletion zone.

mobility μ_{eff} are functions of dopant density and layer morphology

$$\sigma_{\text{pSi}} = q \bar{p} \mu_{\text{eff}} \quad (2.39)$$

$$\mu_{\text{eff}} = d_c q \sqrt{\frac{1}{2\pi m^* kT}} \exp\left(-\frac{E_B}{kT}\right) \quad (2.40)$$

where q , d_c , and m^* denote unity charge, grain diameter, and effective mass, respectively. E_B represents the impact of an energy barrier originating from the grain boundaries. A high density of defects Q_t per unit area can be found at the grain boundaries of poly-silicon. These defects act as trapping centers which reduce the number free carriers. Furthermore, trapped carriers at the grain boundaries built-up potential barriers increasing the barrier height E_B which reduce the effective mobility of the remaining free carriers. The density of traps Q_t/d_c per unit volume will be very high and will exceed the density of dopants N per unit volume if the film structure is very fine-grained and the average crystal diameter is small. Consequently, all carriers will be captured after activation at the grain boundaries leaving the grain bulk fully depleted. For such a layer morphology, the barrier height will increase with increasing dopant concentration. The minimum of μ_{eff} is reached when the trap density is equal to the dopant density N , because the whole layer is depleted and the potential barriers are at their maximum height. If dopant concentration or grain size is further increased N gets larger than the trap density and the mobility starts to increase. The depleted grain regions shrink and the energy barriers decrease with $1/N$. These cases are illustrated in Fig. 2.31. The existence of the described two regimes lead to differing temperature dependencies which can be utilized to deter-

mine the dominating resistivity component of the actual deposit under test:

$$\bar{E}_B = \frac{q^2 d_c^2 N}{8\epsilon_{pSi}}, \quad \sigma_{pSi} \propto \exp\left(-\frac{\frac{1}{2}E_g - E_f}{kT}\right) \quad Q_t > d_c N \quad (2.41)$$

$$\bar{E}_B = \frac{q^2 Q_t^2}{8\epsilon_{pSi} N}, \quad \sigma_{pSi} \propto \frac{1}{\sqrt{T}} \exp\left(-\frac{E_B}{kT}\right) \quad Q_t < d_c N \quad (2.42)$$

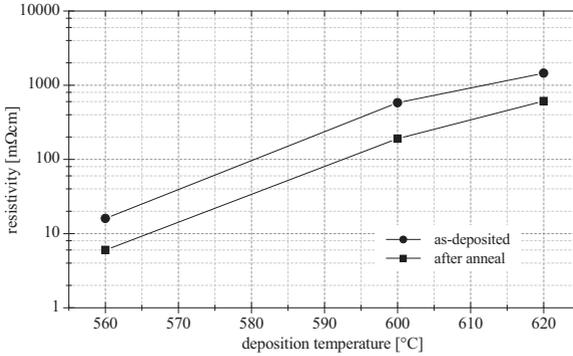


Fig. 2.32: Resistivity of in situ boron-doped poly-crystalline silicon versus deposition temperature. Data is given for as-deposited and annealed films. Annealing was conducted for min 30@950 °C in nitrogen atmosphere (layer thickness \approx 500 nm; deposition parameters: PBOR560, PBOR600, and PBOR630). Resistivity data was measured with a Veeco Instruments PPP5000 Four Point Probe.

From the described resistivity model follows that the average grain size has an important impact, and that there are less stable processes with respect to resistivity around the maximum of \bar{E}_B . In situ boron-doped poly-layers are typically of high crystallinity because of the usually high nucleation rate showing a large number of defects. It needs to be noted that TEM images can not reveal the perfectness of the crystallites and can not provide information of the actual prevailing defect density required for the estimation of the layer conductivity. The observed grains may be full of defects like sub grain boundaries, dislocations, and twins. The importance of this consideration becomes obvious when the data given by [Bou96] is considered. Boukezzata et al. observed the previously stated decreasing grain size with increasing deposition temperature (TEM measurement), but at the same time, a constant grain size, one order of magnitude smaller, was measured by means of Raman spectroscopy. The Raman value corresponds to the mean size of perfect crystal domains. That is, the electrical effective grain size of as-deposited layers did not change significantly although the mechanical and optical grain size was influenced. A higher crystal perfectness of the as-deposited layers, as well as a stronger crystal growth of high temperature deposits, was observed. The lowest resistivity values are achieved

electrically
effective
grain size

with re-crystallized amorphous or partly crystalline layers, either if recrystallization takes place during deposition or in a successive anneal (see [Mar88]). Amorphous deposits have typically a high hydrogen content which promotes crystal growth and leads to comparably larger grain sizes.

dopant
activation

A high dopant activation follows from the deposition dynamics. The boron atoms act as nucleation centers. Therefore, the dopants are readily incorporated into the growing crystallites. A nearly constant boron activation in as-deposited layers of 70 % which does not decrease before solid solubility is exceeded by two orders of magnitude is reported [Haj89]. This surprisingly high boron incorporation and activation is supported by a number of other publications [Fre95] [Nak86]. However, the solid solubility of boron is approximately one order of magnitude below that of phosphorus (see Fig. B.8). This accounts in conjunction with the commonly smaller grain sizes for the higher resistivity of boron-doped layers.

anomalous change
of resistivity

The resistivity of thick poly-crystalline as-deposited layers (type PBOR560 and PBOR560BT) increased during anneal at moderate temperatures below 800 °C (see Fig. 2.33). Thin deposits (thickness <400 nm) did not show this trend. Examples for the observed anomalous behavior of thick films can also be found in literature (see e.g. [Lee82], [Yl603] or [Nak86]). The increasing resistivity can be explained with the conduction model as described above. The conductivity of the layer may decrease in two cases if the provided thermal energy during anneal is too low for a strong primary crystal growth: N increases due to additional dopant activation in cases where $d_c \times N < Q_t$ holds, or hydrogen desorption increases the number of dangling bonds thus increasing Q_t . This interpretation is supported by an observable drop of the resistivity of the same layers below the as-deposited value if annealing temperature is increased above 900 °C. The resistivity of thin deposits is to a greater extent influenced by the start layer. Their resistivity decreases even at low annealing temperatures. A very high boron incorporation at the beginning of the layer formation is reported [Haj89]. Therefore, it can be supposed that $d_c \times N > Q_t$ may hold because of a high c_B in the initial film growth regime.

annealing &
grain growth

The electrical and mechanical properties of poly-silicon layers can be tuned by means of annealing. The general aspects of the discussion about recrystallization and primary grain growth of Section 2.3.1 hold similarly for the case of in situ boron-doped layers. In addition, the influence of the boron dopant must be considered. Segregation of atoms at grain boundaries is reported to affect the anneal. This effect is known as the solute drag effect. However, studies have shown that dopant segregation, if occurring,⁶⁹ does not have a great action. Furthermore, boron has been shown *not* to segregate at grain boundaries and n-type dopants have been demonstrated to *promote* the growth instead of hindering it [Kim88]. Additionally, explanations assuming segregation effects fail in cases where co-doping leads to a compensation of dopant effects on the annealing procedure. This shortcoming is resolved by a vacancy dominated diffusion model.⁷⁰ That is, the grain boundary mobility M defined by (2.37) is proportional to the number of vacancies and the density of va-

⁶⁹ Dopant segregation is reported to occur for n-type dopants like phosphorous or arsenic.

⁷⁰ Interstitial diffusion can be ruled out due to the measured activation energies for the diffusion of Si and B in silicon. In both cases E_A is close to 4 eV well above the typically values of below 2 eV for interstitial diffusion [Sze85].

cancies is influenced by the dopant type and concentration. It is demonstrated that n-type dopants change the vacancy density stronger than p-type dopants [Kim88]. Both types promote crystal growth speed in higher densities but the effect can be neglected in case of B doping boron because of the lower solid solubility (see also Fig. B.8) [Kim88]. That is, the commonly very fine grained in situ boron-doped layers are thermally more stable than n-type doped layers. Their grain boundary mobility is almost identical to that of intrinsic poly although growth starts at a smaller initial grain diameter.

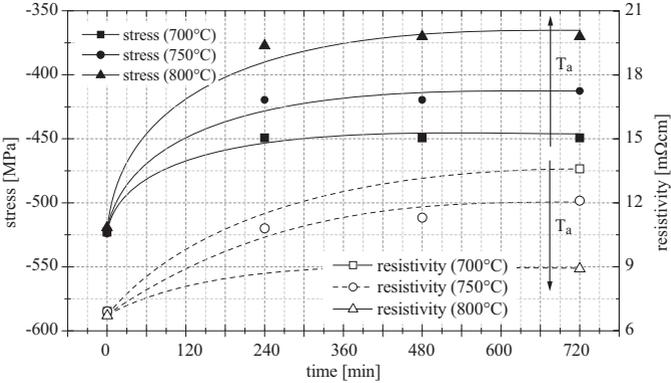


Fig. 2.33: Stress and resistivity change of crystalline as-deposited in situ boron-doped poly-silicon during anneal. All samples were simultaneously deposited on silicon substrates (960 nm, parameter set PBO560BT see Tab. B.11). Stress and resistivity depend on grain size and can be annealed asymptotically (lines are only added as guides for the eye). The resistivity increases because $d_c \times N < Q_t$ holds for the as-deposited layer.

The mechanical stress of in situ boron-doped poly-silicon film is associated with the deposit's morphology as discussed for un-doped poly in Section 2.3.1. Therefore, the general annealing trends depicted in Fig. 2.24 for un-doped poly hold analogously for in situ boron-doped layers. A high compressive intrinsic stress results for crystalline as-deposited films due to their high small grained morphology. This leads to a high overall compressive film stress on silicon substrates (see Fig. 2.33). Amorphous or semi-amorphous layers can be tensile with a stress level depending on the magnitude of recrystallization (see Fig. 2.9(b), PBOR580). A 350 MPa shift of the stress level on silica caused by the increased thermal stress component are measured (refer to Fig. 2.3 and Fig. 2.9(b)). Intrinsic and thermal stress can counterbalance on fused silica leading to total stress levels of low tensile magnitude. This makes in situ boron-doped crystalline as-deposited poly-silicon films particularly attractive for surface micromachining on fused silica. Unlike n-type dopants, boron does only promote the primary crystal growth to a negligible extend (see preceding paragraph). The annealing kinetics of in situ boron-doped poly are for this reason very similar to those of un-doped poly. This feature can be beneficial if the mis-

mechanical stress

match of TEC renders the very fine grained boron-doped poly layer tensile on fused silica.⁷¹ That is, the as-deposited fine grained layers change their stress slowly and can be tuned in asymptotic long anneals by adjusting the process temperature (see Fig. 2.33). The resulting stress trend can be understood and predicted by considering (2.36) because of the proportionality of stress to the deposit's grain size. Stress adjustment is particularly simplified due to an almost linear relation of stress and annealing temperature in a small temperature range as can be observed in Fig. 2.33. This feature is allowing a straight forward stress adjustment by only changing T_a while keeping annealing duration constant.

O₂ diffusion
& oxidation

Reversible oxygen penetration into silicon and poly-silicon was described already in the preceding section for un-doped poly-silicon films. Oxygen diffusivity in silicon is described by (2.38). It is also applicable for poly-crystalline films but the actual penetration depth may increase proportional to the crystallographic defect density. This influence of the fine-grained structure shows up also in reported oxidation rates of in situ boron-doped poly-silicon, which are about 4/3 of the rates given for single-crystalline silicon [Bou96]. This ratio is reflected in estimated oxygen penetration for relevant cases of this work summarized in Tab. 2.6.

Physical vapor deposition

Possible issues during physical vapor deposition on fused silica may arise related to the thermal and thermo-mechanical properties of the substrate material. In comparison to silicon, both thermal conductivity ($\lambda_{th@32\text{ }^\circ\text{C}} = 1.31\text{ W/mK}$) and expansion ($\alpha_{20\text{ }^\circ\text{C}} = 0.5 \times 10^{-6}\text{ K}^{-1}$) are low [Sch07]. The TECs of common metal deposits are two orders of magnitude above that of silica. Even low deposition temperatures can result in considerable film stress levels.

as-deposited stress

Only a sputter deposition of an aluminum metallization was required in course of this work with the process conditions summarized in Tab. B.14. The process temperature was not measured explicitly but is expected to be roughly 150 °C and caused by the kinetic energy of the sputtered aluminum atoms. This leads to a thermal stress of 270 MPa on silicon and 300 MPa on silica. These stress magnitudes are calculated with an approximate TEC of $23 \times 10^{-6}\text{ K}^{-1}$ and a biaxial modulus of 105 GPa for aluminum [Kap00]. An intrinsic compressive stress component is present in sputtered aluminum layers due to the poly-crystalline morphology of the deposit. Therefore the overall stress magnitude is lowered and was measured to be 100 MPa on silicon and silica (see Fig. 2.34).

effect of thermal
anneal and humidity

In theory, the thermal stress increases to 950 MPa and 1125 MPa on silicon and silica, respectively, if the layer relaxes during a forming gas anneal at 500 °C. These rather higher stress levels must be expected to relax due to the ductile nature of aluminum. In practice, the measurement data presented in Fig. 2.34 does not indicate an explicit trend of the layer stress. In contrast, it can be noted that humidity has an important affect on the overall stress. Humidity diffuses readily into, and out of the layer causing reversible stress changes with a magnitude of 75 MPa – 100 MPa.

⁷¹ The fine grained poly-crystalline as-deposited layers are highly compressive if deposited on silicon and remain compressive under all applicable annealing conditions.

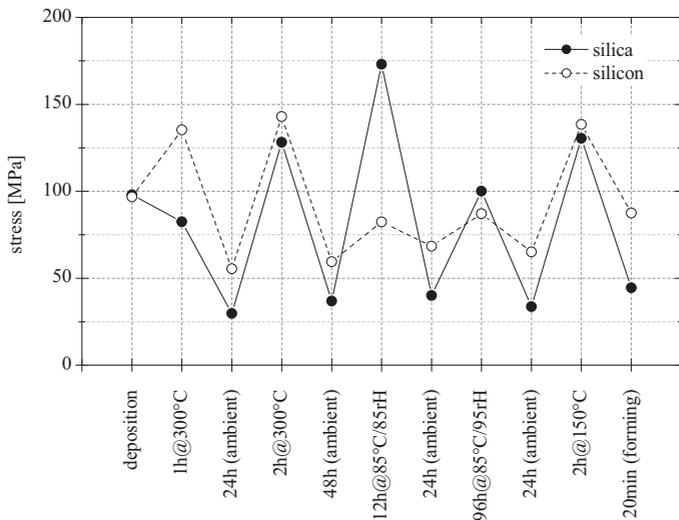


Fig. 2.34: Stress of sputtered aluminum on silicon and silica and the influence of humidity and thermal anneals. Aluminum was sputtered directly onto a blank silicon substrate and onto a silica wafer covered with 200 nm PBOR560. Forming was conducted in N_2/H_2 ambient at 400 °C.

These changes are more pronounced for the layer on silica.⁷² This observation may indicate a differing layer morphology on silica (see next paragraph). The results show that large aluminum areas should not be located close to a stress sensitive transducer.

The preceding approximative calculation of the as-deposited stress was based on the assumption that deposition temperatures on silicon and silica are identical. This is not the case because of the differing thermal properties of both substrate materials. The surface temperature on silica is higher than on silicon for similar process conditions. The thermal conductivity of silica is lower and the kinetic energy of the impinging atoms is therefore not readily transferred to the chuck as for silicon substrates the case. The particle bombardment heats up the substrate and the higher the surface temperature is the higher is the desorption rate of impinging atoms lowering the net deposition rate. Therefore, layers, either sputtered or deposited by means of other plasma enhanced processes, will be thinner on silica (or on free standing structures) having a differing morphology.⁷³

Pure aluminum melts at $T^{(melt)} = 933 \text{ K}$ (660 °C) but interaction with the sili-

surface
temperature
increase

Al/Si-interface
instability

⁷² The measurement data scatters because of differing times between climate stress application and stress measurement.

⁷³ The process temperature during reactive ion etching is somewhat higher for the same reason on silica increasing the isotropic chemical layer attack.

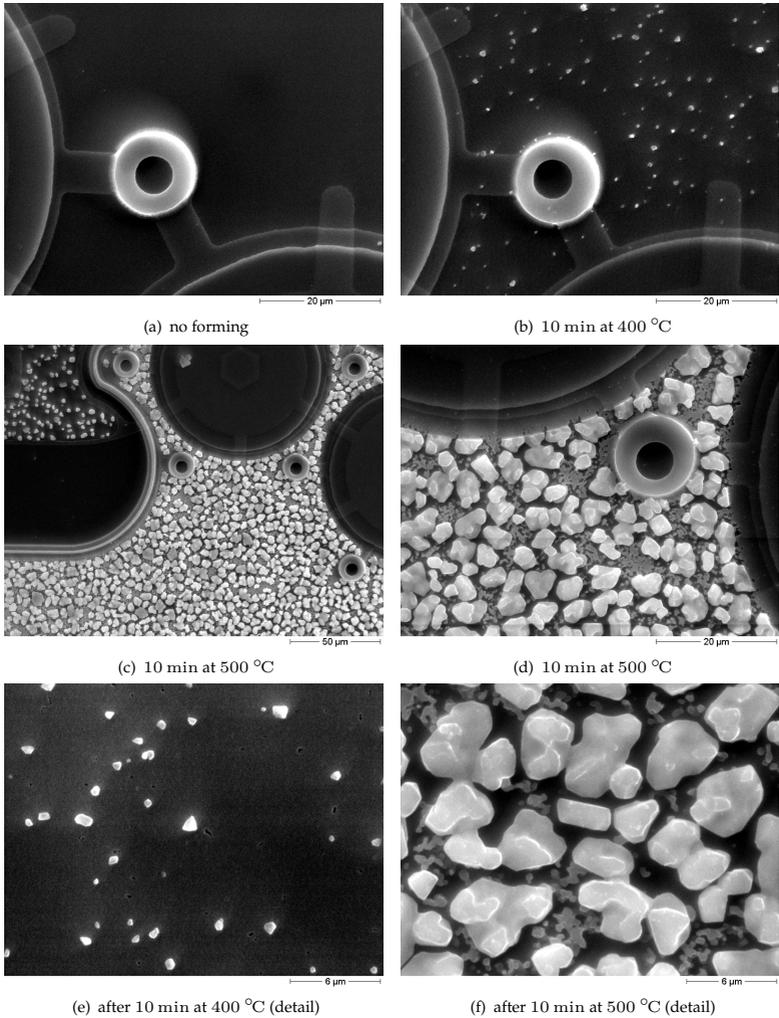


Fig. 2.35: SEM pictures of precipitations caused by forming gas anneal of pure aluminum on poly-silicon. The pictures show the poly-silicon surface after aluminum removal with A-etch. Forming took place in H_2/N_2 ambient for the given duration (plus additional 6 min of N_2 purge).

con surface starts already at lower temperatures [Sze88].⁷⁴ For this reason, Al/Si-interfaces are only considered to be stable up to 250 °C. Typical interconnection failures caused by aluminum in CMOS processes are *spiking*, *precipitation*, and *electromigration*. Aluminum diffuses in a thermally activated process into the silicon bulk forming Al-spikes. Precipitations occur during cool-down after a thermal anneal (see Fig. 2.35). Excess Si and Al agglomerates and gives rise to non-ohmic contacts to n-type silicon because the Si-precipitations are p-doped up to the solid solubility limit.⁷⁵ Aluminum poly-silicon interface properties are believed to influence the performance of the presented sensor at higher frequencies and the long-term stability at high operation temperatures (> 150 °C). Changes in the contact resistance or interface capacitance will influence the actual sensor reading and should be constant. Surface states are present at the poly-Si/Al-interface, which must be charged and discharged when an ac voltage is applied to the contact leading to power dissipation. This contact impedance is believed to be of similar nature as the interface trapped charges in MOS devices as discussed in [Sze81] and [Nic82]. Therefore, this impedance is expected to give rise to temperature and frequency dependency of the presented sensor (see Fig. 3.56) which has to be prevented by appropriate forming.

influence on the
sensor perfor-
mance

Table 2.7: Contact resistance of aluminum to in situ boron-doped poly-silicon (PBOR560). The resistances were measured with *Kelvin* test structures before and during successive anneal in forming gas (H₂/N₂) and on a hotplate in ambient atmosphere. The forming in the furnace required an additional purge cycle of 6 min in N₂ at process temperature.

10 min forming		ambient anneal@300 °C	
temperature [°C]	resistance [kΩμm ²]	time [min]	resistance [kΩμm ²]
none	35.8	0	25.1
300 °C	11.5	5	7.7
400 °C	7.0	10	6.6
500 °C	7.9	15	6.2
		720	3.8

Contact resistance is influenced by the interface cleanliness, the dopant type and level, and crystalline structure of the contact materials. The ability of aluminum to reduce SiO₂ is the reason why it is so common despite of its low temperature stability. Reduced oxygen from the contact interface is transported into the Al-bulk during post deposition anneal in N₂/H₂ ambient. This procedure is called *forming* and is typically performed for 30 min–60 min at 350 °C–450 °C [Nic82]. Silicon

contact resistance
Al forming

⁷⁴ All interactions of Si and Al are solid state diffusion controlled processes which require, as a rule of thumb, a temperature of at least 1/3 of the melting point of the solid in which the diffusion takes place. This gives a critical temperature of 563 K (290 °C) for silicon (silicon: $T^{(melt)} = 1688$ K) and 311 K (38 °C) for aluminum [Sze88].

⁷⁵ A detailed discussion can be found in [Sze88]. Experimental results related to aluminum metallization problems can be found e.g. in [Zho03] presenting experimental data for long-term anneals (up to 4 h) in a temperature range of 300 °C–550 °C.

interface atoms with dangling bonds are either saturated with H_2 or diffuse into the Al bulk.⁷⁶ Aluminum is a p-type dopant and therefore *Schottky* contacts should not be expected to p-type substrates. However, still high-ohmic non-linear contact resistances can form to low-doped p-type single crystal silicon substrates and have been measured (see Fig. B.9).

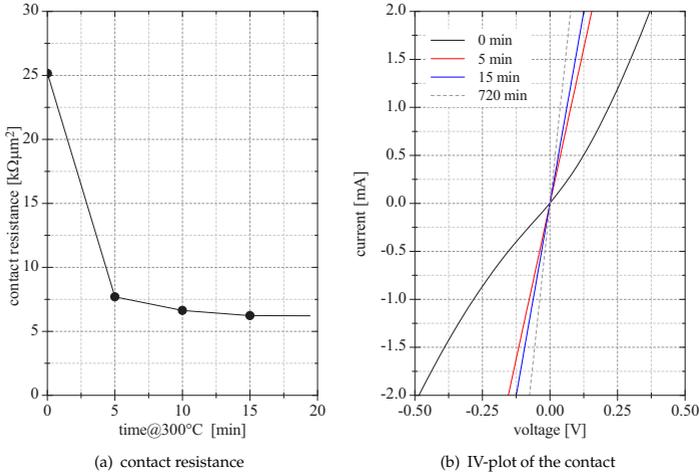


Fig. 2.36: Contact resistance of a $1\ \mu\text{m}$ pure aluminum layer to an in situ boron doped poly-silicon film (PBOR560) of 200 nm. The resistance was measured with a *Kelvin* test structure having a contact area of $100\ \mu\text{m}^2$ during a successive anneal on a hotplate in ambient atmosphere at $300\ ^\circ\text{C}$.

Table 2.8: Measured sputter etch rates for various LPCVD layers (process parameters are summarized in Tab. B.14).

material	rate [nm/min]
PBOR560	3.5
TEOS4Z	12.6
LTO450Z4	11.8
TOX	7.2
Nit-Z20	9.0

In situ boron-doped poly-silicon is chosen as electrode material for the presented

⁷⁶ Additionally, minute amounts of H_2O in layers, like e.g. oxide, below the Al metallization reduce at the Al-interface and the resulting free atomic H annihilate dangling bonds in a superior way. Improving the stability of MOS structures [Dea69].

sensor. Its high p-type dopant level and the distorted poly-crystalline interface prevents the formation of a *Schottky*-contact. Still a non-linear contact resistance is measured after deposition (see Fig. 2.36(b)) which can be attributed to oxide and dangling bonds at the interface. Contact resistances were measured with a *Kelvin* resistor similar to the descriptions given in [Hol04] [San00] [Sch88]. Annealing experiments were conducted for 10 min in H₂/N₂ ambient at 300 °C – 500 °C. The magnitude of Al/Si inter-diffusion during these anneals is revealed by SEM pictures presented in Fig. 2.35 which are showing the sensor surface (mainly PBOR560) after removal of the annealed aluminum with A-etch. The onset of precipitation formation is at about 400 °C and large crystallites are already observed after 10 min at 500 °C (see Fig. 2.35(f)). The corresponding contact resistances are given in Tab. 2.7. Additional annealing tests were conducted on a hotplate at 300 °C in ambient atmosphere. The measurement data shows that the contacts are ohmic and of low resistivity already after 5 min (see Fig. 2.36). Moreover, extensive additional anneal for 12 h at 300 °C in ambient decreases the resistivity to 50 % of the magnitude measured after 5 min (see Tab. 2.7) and does not lead to precipitations.

contact to poly-Si

annealing at ambient atmosphere

Not particularly related to processing on fused silica but of interest for the presented sensor is the required sputter etch step prior to the metal deposition. This surface cleaning step is necessary but removes a markedly fraction of the underlaying material. This results in thinning of test structure dielectrics and in a decreased thickness of the transducer layer (see Fig. 3.43 for an example). The measured sputter etch rates are summarized in Tab. 2.8.

sputter etching

Step coverage and penetration depth

The step coverage and penetration depth are important features of a CVD process. They are of special concern when a vacuum seal must be fabricated or if high aspect ratio cavities should be covered with conductive material for the purpose of electrical via formation. In the first case, the penetration is unintended in contrast to the latter case where a perfect coverage of the interior of a hole or trench is required. Two facts are important for the general understanding:

1. **Gas diffusion into and within the cavity does not take place.** Approximated mean free path lengths λ of source gas molecules during CVD processing are summarized in Tab. 2.9 (see Tab. B.11 for process condition details). The mean free path is calculated with [Liu99]

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 p_a} \quad (2.43)$$

where d and p_a denote the molecule diameter and process pressure, respectively, k and T have their usual meaning. The assumed diameters can be found next to calculated mean free paths in Tab. 2.9. The results show clearly that λ exceeds the typical feature size by far. The small silane molecule during poly-silicon depositions has a mean free path of 650 μm – 1400 μm and λ equates to 60 μm – 120 μm even for the large CVD oxide precursors. For this reason, collisions between precursor molecules are not the driving force for

material transport into and within the cavity. On the other hand, interaction with the cavity walls gains importance. Usually the *Knudsen* number \mathcal{K}_n is used to access which transport dominates. It relates the mean free path to the mean feature dimension ℓ (smallest length of a feature which confines the molecular motion)

$$\mathcal{K}_n = \frac{\lambda}{\ell}. \quad (2.44)$$

Gas diffusion as described by *Fick's law* prevails for $\mathcal{K}_n < 0.001$ whereas a free molecular flow is assumed for $\mathcal{K}_n > 10$ which is dominated by wall interactions. The range of $\mathcal{K}_n = 0.1 \dots 10$ is referred to as the transition regime where gas diffusion is not in equilibrium, i.e. continuum diffusion models fail but inter-molecular collisions must still be considered [Hak99]. This is only possible with direct computational simulations as e.g. conducted in [Cor93] for LPCVD. Common LPCVD conditions result in $\mathcal{K}_n > 10$ or are at least within the transition regime. TEOS is the deposit which enters first the transition regime if feature dimensions exceed $6 \mu\text{m}$ (see Tab. 2.9). The other extreme is Poly4Zol for which molecular flow can be assumed up to a feature size of $140 \mu\text{m}$.

2. **Re-emission controls the homogeneity of the deposit in the cavity.** It can be found that surface diffusion has only a negligible impact on the conformity of LPCVD deposits [Che91]. Instead re-emission of adsorbed atoms takes place to an incredible extend and causes spreading of the molecules in all spacial directions [Wul91] [Cor93]. A sticking coefficient σ_{CVD} can be defined to access the magnitude of particle re-emission. σ_{CVD} represents the ratio of atoms which are integrated into the deposit per unit area and unit time

$$n_i = \frac{r_d}{V_m} = \frac{r_d \rho}{M} \quad (2.45)$$

to the overall number of surface contacts per unit area and unit time

$$n_c = \frac{p_d}{2 m_M u} = \frac{p_d}{2 \sqrt{3 k T m_M}}. \quad (2.46)$$

The calculation requires the deposition rate r_d and pressure p_d , the molar mass of the film M , the film density ρ , the molecular precursor mass m_M , and the average precursor molecule velocity u . This gives the sticking coefficient

$$\sigma_{\text{CVD}} = \frac{2 r_d \rho}{M p_d} \sqrt{3 k T m_M}, \quad (2.47)$$

which equates to $(9 \dots 32) \times 10^{-6}$ for silane, to $(3 \dots 8) \times 10^{-6}$ for the silicon nitride source gas molecules, and to $(14 \dots 19) \times 10^{-6}$ for the large oxide precursors (see Tab. 2.9). Although highly approximative, the calculated values are in good agreement with literature data (see e.g. [Gri02]). The closer σ_{CVD} gets to zero the more atoms are re-emitted from the wall and the more homo-

geneous gets deposition. At σ_{CVD} equal to unity all arriving molecules are integrated into the deposit without re-emission.

Table 2.9: Approximate mean free path lengths λ (2.43) and sticking coefficients σ_{CVD} (2.47) of reactants during CVD processes for the CVD process parameters listed in Tab. B.11. Numeric values for deposit density ρ , molar mass of the deposit M , and molecular diameter of the source gas molecule d are given as assumed for the calculation (DES: di-ethyl-silane $\text{SiH}_2(\text{C}_2\text{H}_5)_2$; DCS: di-chlor-silane SiH_2Cl_2 ; TEOS: tetra-ethyl-ortho-silicate $\text{SiO}_4(\text{C}_2\text{H}_5)_4$).

layer	λ/d [$\mu\text{m}/\text{\AA}$]	ρ [g/cm^3]	M [g/mol]	σ_{CVD} (source) [1×10^{-6}]
Nit-D20	460/6.0 (DCS)	2.8 – 2.9 [Mak83]	109.9	3 (DCS) 7 (NH_3)
Nit-Z20	460/6.0 (DCS)	2.8 – 2.9 [Mak83]	128.0	4 (DCS) 8 (NH_3)
PBOR560	800/3.5 (SiH_4)	2.33 (silicon)	28.1	9 (SiH_4)
PBOR580L	650/3.5 (SiH_4)	2.3 (<silicon)	27.8	10 (SiH_4)
Poly4Zol	1400/3.5 (SiH_4)	2.33 [MS96]	28.1	32 (SiH_4)
aSiX585	1100/3.5 (SiH_4)	2.25 [MS96]	27.1	14 (SiH_4)
TEOS4Z	60/11.5 (TEOS)	2.18 – 2.35 [Car02]	60.1 (SiO_2)	19 (TEOS)
LTO450Z4	120/6.0 (DES)	2.25 [Lev93]	60.1 (SiO_2)	14 (DES) 8 (O_2)
PECVD lf-oxide	155/3.5 (SiH_4)	2.25	60.1 (SiO_2)	774 (SiH_4) 36 (N_2O)

The estimated sticking coefficients summarized in Tab.2.9 explain why especially nitride depositions are almost perfectly conform. One gets a good impression on the possible penetration depth of precursor molecules if the inverse of σ_{CVD} is taken. This number represents the average number of wall reflections of a molecule which is spatially confined in a cavity until is attached to its walls. The data in Tab. 2.9 indicate that roughly 250 000 reflections take place for a SiH_2Cl_2 molecule during nitride deposition (Nit-Z20) and that there are still 50 000 and 70 000 impingements for TEOS and LTO, respectively. The resulting high deposition rates in cavities and good step coverage abilities are impressively illustrated by Fig. 3.50 which depicts the cross-section of a wet etched bulk silica cavity with was coated with in situ boron-doped poly-silicon and sealed with LPCVD TEOS. Another example is presented in Fig. 3.39 showing FIB (FIB: focused-ion-beam) cross-sections of the presented sensor. It shows that LTO sealant penetrates all the way into the sensor cavity resulting in an undesired LTO deposition of roughly 45 nm within the cavity. A comparison of LTO

and TEOS sealant penetration into the sensor cavity is presented in Fig. 3.37. Both materials penetrate similarly into the sensor cavities although the process temperatures deviate considerably. This observation becomes reasonable if the similarity of σ_{CVD} for both CVD processes are noted (see Tab. 2.9).

2.3.2 Layout and pattern transfer

The low TEC of fused silica increases the thermal stress component of most CVD films as discussed in Section 2.2. Generally high stress levels in combination with the low biaxial modulus of the substrate result in deformations with impact on the accuracy of lithographic pattern transfer.

Planar stress causes a surface strain which concentrically shifts lithographic alignment keys. The magnitude of this shift can be calculated with the formulas given in Appendix B.1.4. It must be noted that each deposited layer adds another shift to the marker. As an example, the plane stress deformation of a 100 nm Nit-Z20 layer on a 500 μm fused silica substrate can be calculated with (B.9). The initial diameter of $d_S = 100$ mm is contracted by

$$\Delta d_S = -\frac{1}{6} d_S t_S K \approx -0.3 \mu\text{m}. \quad (2.48)$$

Actual observed magnitudes of deformation are larger. The causes are double sided wafer coatings and not fully planar attachments of the wafer to the lithographic chuck. The maximum of marker displacement can be calculated with (B.7) which considers additional shifts due to substrate bending. For the above example, a single side coating results in case of free bending in an overall shift of

$$\Delta d_S = -\frac{2}{3} d_S t_S K \approx -1.1 \mu\text{m}. \quad (2.49)$$

Substrate bending causes a deflection with an adverse impact on the alignment procedure itself. Manipulation of (2.4) yields the wafer deflection h_b as function of layer stress σ_F , bulk modulus E_S' , and substrate diameter d_S

$$\frac{h_b}{t_F} = \frac{3}{4} \frac{\sigma_F}{E_S'} \frac{d_S^2}{t_S^2} \quad (2.50)$$

where t_F and t_S denote the thicknesses of film and substrate, respectively. The wafer bow is generally larger on silica substrates for two reasons: the low biaxial modulus of the substrate and the higher thermal stress magnitudes. Figure 2.37 illustrates the consequences for 100 mm substrates. The resulting bow due to various stress magnitudes versus substrate thickness is plotted (example bow values for 150 mm substrates are presented in Fig. B.14). The deflection caused by a 100 nm Nit-Z20 insulation equates to approximately 5.3 μm on a 500 μm thick silicon substrate but increases to 39.8 μm on silica. The bow increases for thinner substrates with $1/t_S^2$.

Finally, automatic wafer handling of silica substrates may become an issue. The transparent substrate can cause some mask aligners to fail during wafer flat detection. A simple solution to this problem is to leave a ring of a non-transparent film around the wafer border. (Such a ring should be patterned for the purpose of stress

concentric shift of
alignment keys

vertical
deflection

substrate's
transparency

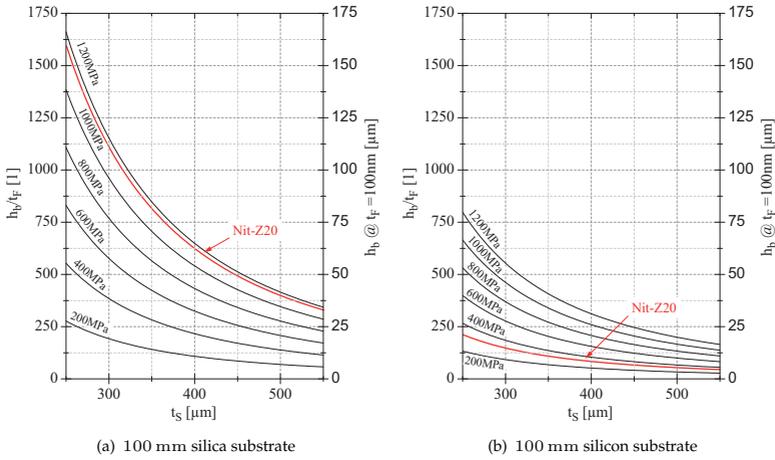


Fig. 2.37: Normalized wafer bow h_b/t_F versus substrate thickness for various stress levels on 100 mm fused silica and silicon substrates (h_b : substrate deflection; t_F : film thickness).

relieve.) A markedly influence of the substrates transparency on resist exposure was not observed.

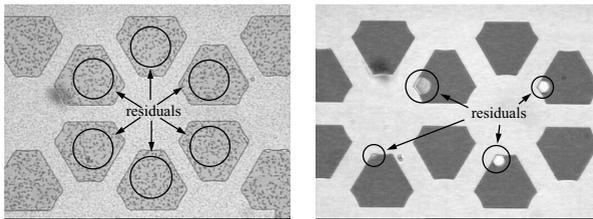
2.3.3 Wet etching

Wet chemical etching processes are of particular importance on fused silica. Layer thicknesses must be limited due to the increased stress levels. This thickness limits in combination with the low selectivity and homogeneity of dry etching processes render them not applicable in many cases. Thin and highly stressed layers are of special concern for stress sensitive transducers because of their impact on the local stress. The inhomogeneous removal of a couple of nano-meters during RIE processing can have a markedly effect on the homogeneity of the transducer performance. For this reason wet etching was preferred as fabrication means whenever possible. The utilized etchants and techniques are common and only slightly tuned to the special need of the presented sensor. Therefore, the individual processes are only briefly discussed. Some extra stress is placed on oxide etching because its rate control and selectivity towards the nitride passivation layers is of high importance for the presented sensor. Etchant recipes are summarized in Tab. B.16.⁷⁷

⁷⁷ An overview of wet etchants for micromachining purposes is given by [Wil96] and may be used as starting point for an etchant selection.

Poly-silicon etching

Different chemicals have been evaluated to etch poly-crystalline silicon with selectivity towards nitride and oxide [Sai04]. The intention was to select a process which offers a good rate control, i.e. which is only weakly dependent on the poly silicon's doping level and morphology, and has a low adjustable rate. Anisotropic silicon etchants like TMAH (TMAH: tetra-methyl-ammonium-hydroxide, $(\text{CH}_3)_4\text{NOH}$) did not meet the requirements because of the encountered difficulty to remove crystallites at the substrate interface completely (see Fig. 2.38(a)). These crystallites cause etch duration deviations and impede well controlled undercuts.⁷⁸ Different mixtures of nitric acid (HNO_3) with hydrofluoric acid (HF) diluted in water or acetic acid (CH_3COOH) have been tested. It was found that acetic acid increased the acidity of the solution and lead to an increased resist mask attack (MicroChemicals, AZ1518). Good results have been achieved with a modified water diluted nitric acid (P-etch). This solution etches PBOR560 with a reproducible rate of $110 \text{ nm}/\text{min}$. A proper choice of the mix-ratio guaranties a bubble free etch process. Bubbles, if occurring, stick to the surface and cause residuals (see Fig. 2.38(b)). Special care must be taken with the choice of wetting agent. The use of isopropanol improves the results.⁷⁹ Best results were obtained with the addition of a fluorosurfactant.



(a) crystalline residuals after poly-Si etching in TMAH

(b) residuals caused by bubbles during etching in phosphoric acid

Fig. 2.38: Examples of residuals after wet-chemical etching of PBOR560.

Oxide etching

Fused silica is chemically equivalent to thermal oxide of high purity and etches with a similar rate (see Tab. B.17). As mentioned before, the stress dependent thickness limit of some deposits on fused silica prohibits the use of RIE instead of wet chemical processes in many cases. Consequently, well defined lateral dimensions must be achieved by oversized mask design and well controlled wet chemical undercuts. Three distinct oxide etch conditions occurred in course of this work:

⁷⁸ This is especially the case for the highly boron-doped PBOR560 layer which is of great importance for the presented sensor.

⁷⁹ Care must be taken if isopropanol is added to P-Etch because it may react readily with the etchant! Triton X-100 ($\text{C}_{14}\text{H}_{22}\text{O}(\text{C}_2\text{H}_4\text{O})_n$) as non-ionic surfactant reacts with the etchant and does not lead to stable etch rates.

1. Etching of low density oxides with well controlled undercut.

A low and stable etch rate is required if as-deposited LTO or TEOS must be etched with an accuracy better than 50 nm. Standard BOE (BOE: buffered oxide etch) is not well suited because of its high etch rate of approximately 500 nm/min. This rate can be reduced by dilution. Ammonium fluoride (NH₄F) should be added at the same time to strengthen the buffer and to guaranty constant etch rates (see mod. BOE in Tab. B.16).

2. Etching of an oxide sacrificial layer with nitride as bulk protection.

In this work, silicon nitride was chosen as insulation layer and bulk etch protection at the same time. The choice was mainly caused by the lack of LPCVD layer alternatives and resulted in a challenging sacrificial etch procedure. Generally, HF-based etchants also attack SiN_x. The lower the stoichiometric index x is the lower becomes the etch rate in HF-solutions. Unfortunately, also the insulating properties of the nitride degrade with decreasing x and confine the choice of nitride deposition parameters. Nit-Z20 (SiN_{1.04}) represents a good compromise of insulation properties and chemical resistance.

As much as possible of the insulation and passivation layer should remain after sacrificial layer etch completion. Therefore, the selectivity towards the sacrificial layer oxide etchant must be maximized. The selectivity of HF-based solutions towards silicon oxide and nitride can be influenced by variation of the parameters: temperature, concentration, and pH-value.

The etch rates obey *Arrhenius'* law [Büh97] with higher apparent activations energies for nitrides than for oxides. It follows that the selectivity can be increased by lowering the process temperature as can be observed in Fig. 2.39. For instance, reducing the temperature to 0 °C raises the selectivity of annealed TEOS:Nit-Z20 to about 1330 in mod. fluoric acid. This compares to a selectivity of 380 in BOE at 20 °C (etch rates data is given in Tab. B.15, Tab. B.17, and Tab. B.18). Nit-D20 (SiN_{0.61}) with cumbersome insulation properties is especially tuned as wet etchant protection and is etched with a selectivity towards annealed TEOS of 9340 in mod. fluoric acid at 0 °C.

temperature

The influence of concentration and pH-value on the etch rates of nitride and oxide is discussed in [Kno00] and [Kno01] (a brief summary is given in [Kno05]). The results indicate that nitride is primarily etched by mono-fluorides such as F⁻ and HF, whereas oxide is mainly attacked by di-fluoride species, i.e. HF₂ and H₂F₂. As consequence, the addition of an acid like HCl (equivalent to the introduction of a high number of protons) decreases the pH-value and shifts the equilibrium of the solution towards neutral fluoride species (H₂F₂, HF). This decreases the SiO₂-rate as well as the SiN_x-rate, but the latter one to a lower extend.⁸⁰ On the other hand, dilution of HF-solutions shifts the

concentration
ph-value

⁸⁰ This can be best understood by consideration of the results presented in [Kno01]. There are also literature sources stating an increase of etch rate by adding HCl (at constant HF molarity!) [Mon94] and a reduction of the selectivity towards nitride [Büh97]. The equilibrium concentration of mono- and di-fluorides within the etchant is a non-monotonous function of molarity and pH-value, i.e. its gradient changes the sign. Throughout this work, the HF concentration was very high (50 % HF: 24.5 mol; HF/HCl: 12.25 mol [Mon93]) and at the same time the pH-value was kept very low. In this regime the selectivity is a monotonic function and the experimental observations fit best to the results and interpretations given by [Kno05].

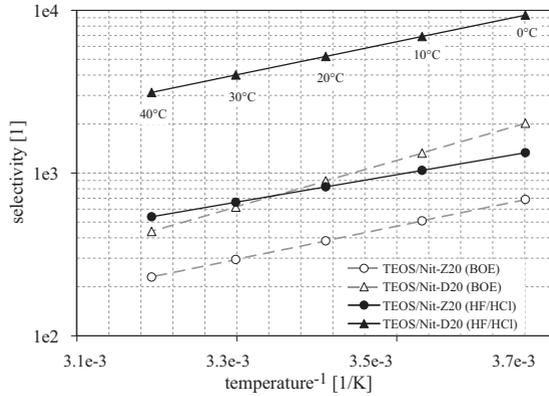


Fig. 2.39: Selectivity versus temperature of LPCVD TEOS (annealed 1 h@950 °C) on various silicon nitride films etched in BOE and HF/HCl.

equilibrium towards the mono-fluorides, thus, reduces the selectivity of the oxide etch with respect to silicon nitride. Consequently, best results must be expected for high concentrated solutions with a low pH-value (see [Kno05]). For this reason, sacrificial layer etch in course of this work was conducted in a mixture of concentrated 50 % HF and 37 % HCl (experimental results are summarized in [Bis05a]). An additional benefit of the HF/HCl is a lowered attack of silicon during long sacrificial etch procedures. Reported surface roughening of silicon during long exposures to buffered HF is attributed to the concentration of OH groups which decrease in number with decreasing pH-value [Miy94].

silicon
attack

The etch rates of deposited oxides (TEOS, LTO) are affected by thermal annealing procedures prior to wet the etching. Annealing leads to shrinkage and densification of these layers of up to 5 % (see Fig. 2.22 and Fig. B.4). However, the etch rate is primarily influenced by the reduction of the hydrogen content of the film, which is as well reduced during thermal anneals [Büh97]. Therefore, the etch rates of annealed TEOS are roughly one third of the as-deposited rates (see Tab. B.17).

oxide
anneal

The etch channel design must be considered carefully if the process time needs to be minimized. Test structures as depicted in Fig. B.11 have been designed to measure the impact of channel width, height, and length on the sacrificial layer etch rate. The test results are summarized in Tab. B.19 and illustrated in Fig. 2.40. It is reported that the etch rate during sacrificial etching is reaction rate limited in the beginning but becomes diffusion limited with increasing etch depth [Mon94] [Mon94b]. The reactant diffusion into the cavity scales with the channel cross-section and large cross-sections lead to high etch rates. As a matter of course, the etch hole cross-section must be chosen equal to or

etch channel
geometry

larger than the channel cross-section. Channel length simply adds to the required overall etch depth and has no impact on the etch rate. Thicker sacrificial layers surprisingly tend to etch faster. This result has been often confirmed (and was also reported in [Mon94]) by tests but no explanation can be given.

3. Etching of large cavities into the bulk silica.

Information on wet bulk micromachining of fused silica is summarized in Section 2.4.1.

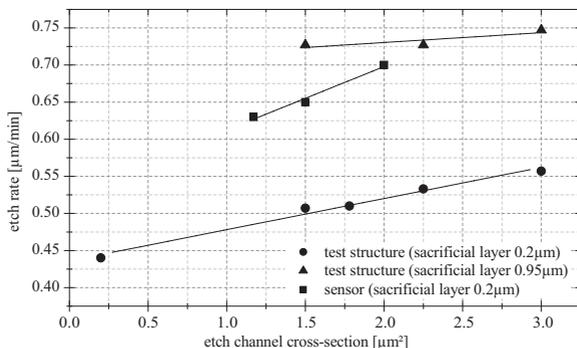


Fig. 2.40: Sacrificial layer etch rates versus etch channel cross-section. Etching of the as-deposited TEOS sacrificial layer took place in a HF/HCl-solution at 0 °C.

Nitride etching

Nitride etching was performed in phosphoric acid (H_3PO_4). Processing took place at 135 °C and obeys *Arrhenius'* law with a rate constant and an apparent activation energy as given in Tab. B.15. Actual rate data is summarized in Tab. B.18. As-deposited TEOS or LTO can be used as hard-mask. Both of these masking layers are etched with rates lower than 0.01 nm/min. Silicon nitride can also be etched by HF solutions (see preceding paragraph and [Kno00] [Kno01] [Kno05]).

Aluminum etching

Pure aluminum was selected as metallization for the presented sensor because of its simplified wet chemical removal. Experiments have been run with AlSiTi deposits requiring an additional dip in diluted HNO_3/HF solution. The dip is necessary to remove silicon grains originating from the metal bulk which settle during wet chemical etching on the wafer surface. This dip also attacks all uncovered polysilicon and is for this reason not applicable for the presented sensor process.

A modified phosphoric acid (A-etch) was used as etchant and processing took place at 35 °C at constant agitation. Two general issues exist:

AlSiTi
etching

issues
Al etching

- Surface wetting is poor and especially small holes may not be etched reproducibly. Two simple solutions exist: an immersion of the wafer in a water/*Triton X-100* bath or a surface activation in an oxygen plasma of low energy prior to the etching procedure.
- Bubbles occur (a mixture of H_2 -NO- NO_2) during etching and may lead to unreproducible results even if the wafers are at constantly agitated. A frequent and complete removal of the wafer out of the etchant is required.

Aluminum is amphoteric, i.e. it can be etched with either alkaline or acidic solutions [Smo04]. As consequence, it is also attacked by alkaline containing developers.

etching of
Cr/Al stacks

Wet chemical removal of a chromium electroplating base layer on top of aluminum is required for the fabrication of the present sensor. The implementation of metal stacks must be carefully considered because a voltaic cell forms if two different metals are immersed in a conductive liquid. A stack of chromium and aluminum e.g. produces an electrochemical potential of 0.95 V. Such a galvanic cell may give rise to corrosion during device operation, but may also vastly increases the undesired etch attack of one of the films as e.g. aluminum during chromium patterning. Best results were obtained by the use of highly concentrated chromium etchants. By this means, the bulk chromium etch rate is maximized and the overall etch duration is minimized. The undercut is not in first place related to the bulk concentration of the etchant but to the ionic transport caused by the potential difference which is in first order independent of the bulk concentration. In this way, metal stacks are best etched with concentrated solutions.

2.4 Bulk micromachining of fused silica

The basic process information summarized in this section was collected during prove of concept studies aiming at the fabrication of electrical through substrate vias into the silica bulk. Details about the proposed via concept, which may be helpful to understand the proceeding discussion, are given in Section 3.2.3 and Section 3.3.8.

2.4.1 Wet and dry bulk etching

masking
material

Wet chemical bulk micromachining of fused silica requires dense masking material which prevents the penetration of the very small F^- ions. Metal layer stacks in combination with a photoresist are frequently proposed as masking material in literature. These are reported to provide limited protection for the formation of shallow channels ($10\ \mu\text{m} - 25\ \mu\text{m}$) [Che04] [Flu96]. With diligent substrate preparation and lithography a photoresist may also be appropriate as mask. The formation of $30\ \mu\text{m}$ deep channels into bulk silica with buffered hydrofluoric acid and resist mask is reported in [Gro01].

LPCVD masks
on fused silica

Poly-silicon is exceptionally well suited for masking purposes due to the very high selectivity of the HF based solutions towards silicon. Bulk micromachining of fused silica allows the application of LPCVD mask material with deposition temperatures up to $800\ ^\circ\text{C}$, i.e. the usage of nitride or poly-silicon. Already the formation of amorphous silicon masks on *Pyrex*[®] at $545\ ^\circ\text{C}$ result in clustering of the aluminum

oxide in the substrate material. These agglomerates do not etch in HF-solutions and give rise to rough surfaces after wet-chemical processing. Some reports have been published which describe the use of LPCVD poly masks mainly for the fabrication of micro fluidic channels (see e.g. [Rou01] or [Ver03]). Poly-silicon is dense enough to prevent any F⁻-penetration and etch depths up to 170 μm are reported [Gre97]. However, pinholes and point defects are observed in case of fully amorphous LPCVD silicon ($T_d = 545^\circ\text{C}$) [Ber00]. These defects limited the process time to 3 h–4 h. Such defects could not be observed in this work and in situ boron-doped poly-silicon (PBOR560) which was used as masking material. An additional advantage of poly-silicon masks is their good adherence to the bulk silica which results in circular etch cavities whereas metal masks lead to very wide cross-sections as result of HF diffusion along the mask-bulk interface causing mask delamination.

Cavities with a depth of 200 μm have been etched into the bulk with 550 nm PBOR560 masks as well as with a layer stack of 120 nm Nit-Z20 and 310 nm PBOR560. A SEM picture of the resulting cavity geometry is presented in Fig. 2.41(c). The achieved aspect ratios were equal to two as expected for an ideal isotropic etch attack. The diameters of the etchant inlet hole of the masks ranged between 2 μm –6 μm but their actual size is of negligible importance for the formation of very deep cavities (see Tab. 2.10 for the process parameters). Both of the implemented LPCVD masks are well suited for the formation of deep cavities but a layer stack of nitride and poly-silicon showed a somewhat higher resistance to mechanical damage, an important feature if the masking material must remain on the wafer during subsequent processing steps.

Table 2.10: Deep wet bulk silica etching process data.

etchant	temperature [°C]	time [min]	depth [μm]	rate [nm/min]	aspect ratio
50 %-HF	20	135	49.7	368.2	2.06
50 %-HF	20	660	200	303.0	1.98

Deep reactive ion etching (DRIE) of silicon has become a standard process. More recently also DRIE of glass, quartz, and fused silica has attracted some attention. Typical applications, which require high aspect ratios in oxide, are electrical substrate vias [Li02], micro fluidic devices [Ver03], or quartz resonators [Abe99]. The approaches are similar: the lack of process selectivity towards resist masks confines the choice to metal layers, very thick LPCVD deposits, patterned bonded silicon wafers.⁸¹ Besides the choice of a proper mask material, difficulties are related to high surface roughness of the etched cavities which is caused by contamination of the etch interface during the process. These contaminations may originate from mask material re-deposition, impurities in case of a glass bulk, or from polymers caused by the C₃F₈ chemistry. A limiting factor for small hole diameters is the sharp

dry etching

⁸¹ Reported selectivities are: fused silica:Cr (50:1, SF_x/C_xF_y, [Don04]), Pyrex[®]:Ni (14:1, SF₆, [Li01]), quartz:Ni (30:1, SF₆, [Abe99]), fused silica:Ni (40:1, C₃F₈, [Cer03]), fused silica:Al (>18:1, SF_x/C_xF_y, [Don04]), fused silica:Si (18:1, C₄F₈/CH₄, [Pav04]), fused silica:Si (25:1, SF_x/C_xF_y, [Don04]).

decrease of etch rate at a certain aspect ratio. The the higher the aspect ratio is the smaller is the number of impinging ions on the cavity bottom. A maximum aspect ratio of 5-7 for small hole patterns of $10\ \mu\text{m}$ diameter are reported in [Li02]. Etch rates vary typically in a range of $200\ \text{nm}/\text{min}$ – $500\ \text{nm}/\text{min}$ but also high rates of $1.2\ \mu\text{m}/\text{min}$ can be achieved with a *Bosch* process ($\text{SF}_x/\text{C}_x\text{F}_y$) [Don04]. Electrical

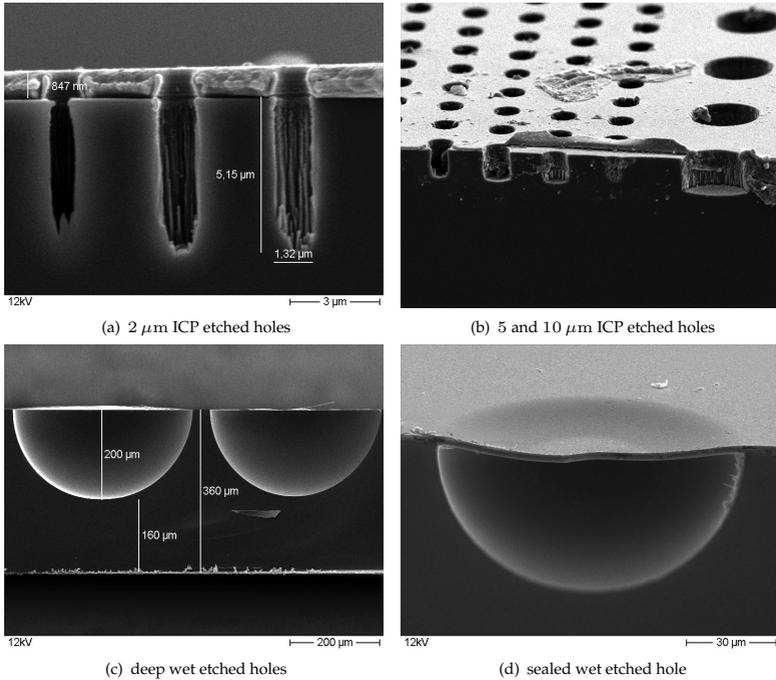


Fig. 2.41: SEM pictures of wet and dry bulk micromachining results. Process data is given in Tab. 2.10 and Tab. 2.11.

DRIE experiments

vias fabricated by means of a combined dry/wet front and back side process are suggested in Section 3.3.8. The approach requires small holes (diameter $\leq 3\ \mu\text{m}$) with a depth of about $30\ \mu\text{m}$. The aspect ratio of 10 is considered to be the technological limit of deep reactive ion etching of silica. Similar to wet-etching, mask material selection is difficult. Nickel is frequently reported to offer sufficient selectivity for a SiO_2 etch [Cer03] [Abe99] [Li01] and was chosen as mask material. One micron of Ni was electroplated on a sputtered Cr/Au ($5\ \text{nm}/25\ \text{nm}$) plating base. A photoresist served as micro-form (*Microchemicals* AZ1518) which was wet-chemically stripped in solvent after completion of the plating process. The Au seed layer was removed by means of physical etching in an Ar-plasma followed by a wet-chemical

Table 2.11: Summary of bulk silica DRIE etching results. (two hours etching, 10 sccm CHF₃, 15 sccm CF₄, 800 W coil-power, 50 W chuck-power, 5 mTorr process pressure).

mask opening [μm]	fused silica etch			nickel mask attack	
	depth [μm]	rate [nm/min]	aspect ratio [1]	depth [nm]	rate [nm/min]
1.7	3.5	29.2	2.05	275	2.28
4.6	6.1	38.8	1.33	275	2.28
500	15.8	131.7	0.03	275	2.28

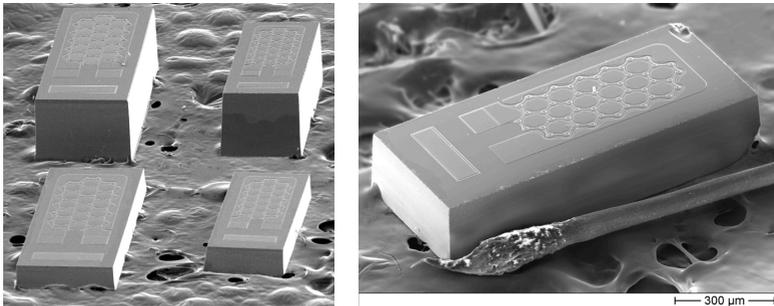
etching of the chromium adhesion promoter with Cr-etch. ICP etching of the fused silica bulk was conducted on a STS etcher at 5 mTorr with a gas flow of 10 sccm CHF₃ and 15 sccm CF₄. Coil- and chuck-power were set to 800 W and 50 W, respectively (details can be found in [Bis05a]). The results summarized in Tab. 2.11 show an etch rate of 131.7 nm/min for large 500 μm mask openings which compare well to the results of [Li01] who is giving a rate of 200 nm/min at the same chuck-power. The depth limit for small holes becomes also obvious from the results given in Tab. 2.11. 2 μm holes could not be etched beyond approximately 5 μm during two hours of processing (5 μm mask openings result in only slightly deeper cavities of about 6 μm). Figure 2.41 shows SEM pictures of the results (some more pictures are presented in Fig. 3.50). A high surface roughness and spikes can be observed and must be attributed to Ni re-deposition on the cavity bottom which was not removed during progression of the etch due to the low chuck-power.

2.4.2 Wafer thinning

Key feature of surface micromachined transducers is their small thickness which is determined by the thickness of the chosen substrate. The presented surface micromachined pressure sensor is with its height of 0.5 mm already comparably thin but some medical applications and consumer electronics require even smaller dimensions. Nowadays, the overall package height of any cell phone components must not exceed 1.4 mm, but this limit will be reduced successively to 1 mm and 0.8 mm in future (including the package's bottom, lid, die-attach bond line, bond-wire loop height, and coating thickness). From a mechanical point of view, the transducer support should be as rigid as possible and the packaging process must be expected to become more challenging the thinner the die will be. Regardless of the expected back-end difficulties, wafer thinning by means of wet-chemical etching and mechanical grinding was evaluated in course of this work. The trials addressed a general transducer height reduction and the facilitation of an electrical through substrate via process (see. Section 3.3.8).

Isotropic wet-chemical etching can be employed to thin the bulk silica wafers. A notable surface roughening takes place during long exposures to fluorine etchants. It follows that the surface must be protected if thinning takes place prior to surface micromachining. As discussed in Section 2.4.1, either poly-silicon masks or with

some limitation also silicon-rich nitrides are suitable as hard mask material and can be removed wet-chemically with a very good selectivity towards the bulk silica. A 100 nm Nit-D20 film offers sufficient protection for one sided removal of 250 μm of bulk silica material (see Tab. B.17 and Tab. B.18). However, such a thinning process would take approximately 24 h and LPCVD mask materials are most likely only applicable in an early stage of a surface micromachining process. These are fundamental shortcomings of a wet-chemical thinning approach. It means that at least some transducer fabrication steps must take place on the thinned bulk material. The fragile and brittle wafers may fracture readily and also precise lithography will become challenging on thin silica substrates. As discussed in Section 2.3.2 a large bow has to be expected and also the concentric shift of alignment keys due to layer stress scales linearly with the substrate thickness. For example: a one-sided 100 nm Nit-Z20 layer on a 300 μm fused silica wafer with a diameter of 100 mm results in a bow of roughly 110 μm (see Fig. 2.37) and, according to (2.49), an alignment key shift of about 3 μm . For this reason wet-chemical thinning was ruled out as thinning means for this work.



(a) comparison prior and after thinning

(b) a sensor with a height of 170 μm next to a human hair

Fig. 2.42: SEM pictures of mechanically thinned sensor dice.

wafer grinding

Wafer grinding and polishing of fused silica was evaluated on a *Logitech PM5*. Thinning was conducted after transducer fabrication with a thick photoresist/dicing tape protection of the sensor structures. A slurry with 9 μm calcined Al_2O_3 particles supplied by *Logitech* was used for grinding (process details are given in [Bis05a]).⁸² The total thickness variation caused by the surface roughness of the mechanically crafted silica substrates was in the range of 6 μm – 14 μm . After start of the grinding process, the surface quality degraded quickly to a stable roughness corresponding to the particle size within the slurry but is also related to the chosen process parameter-set including slurry supply rate, grinding speed, and contact pressure (details about process parameter dependency of TTV, TIR, warp and bow can be found in [Bis05]). No additional theoretical discussion of the grinding and polishing process parameters are given here because the low reproducibility of the results (indicated by the

⁸² The slurry mix ratio was 9:1 (DI-water:powder).

error bar in Fig. B.13) do not allow a further interpretation of the influence of the individual parameter. The measured grinding rates deviate by approximately 20 % and require a two step grinding procedure with a thickness and rate measurement step in between. Cause for the low stability of the process is the slurry supply which is adjusted in a awkward procedure caused by a cumbersome design of the reservoir valve. A decrease in slurry flow rate leads to increased grinding rates and very rough surfaces with the danger that the whole wafer fixture is forced out of its regular guided position. On the other hand, a too high slurry flow rate at a high grinding speed decreases again the rate due to hydroplaning and hopping of the wafer fixture may occur. The most reproducible results were obtained at high slurry supply rates, medium contact pressure and a medium grinding speed (see Fig. B.13). This parameter set lead to a grinding rate of typically $0.4 \mu\text{m}/\text{min}$ and a TTV of $6 \mu\text{m} - 8 \mu\text{m}$.

The remaining surface roughness after grinding could be reduced to approximately $R_a = 10 \text{ nm}$ by subsequent polishing at a rate of roughly $70 \text{ nm}/\text{min}$. The procedure was run on a *Logitech PM5*. Wafers were polished on a felt covered support (OP-Felt supplied by *Struers*) and a suspension of 40 nm particles (OP-S supplied by *Struers*) (details are given in [Bis05a], see also Fig. B.12).

polishing

Figure 2.42 depicts examples of the presented sensor after mechanical grinding to a thickness of $170 \mu\text{m}$. Mechanical thinning of fused silica was found to be very similar to processing of silicon wafers only the grinding rate increased by approximately a factor of two.

2.4.3 Dicing

The bulk silica is more brittle than silicon. Similar process parameters result in wider trenches as can be observed in Fig. 2.43. Furthermore, the brittleness of the substrate causes higher physical strain of the dicing tape/die interface and gives rise to vibration and delamination of small chips if the yield stress of the adhesive is exceeded. Chipping is more pronounced and a safety keep-out area of $\approx 40 \mu\text{m}$ from the expected trench width should be adhered to. Generally, a very low adhesion of glass and fused silica substrates on the dicing tapes must be noted especially after an exposure to fluoride solutions. This observation can be attributed in some degree to surface roughening, which is observable after extended bulk etching in HF (as also reported by [Mor03]). However, it is supposed that the low adhesion of the silica to the dicing tape originates primarily from polar OH-groups which cover the SiO_2 surface. It is commonly known that these hydrophilic surface groups exhibit a bad affinity to non-polar adhesives. The same phenomenon degrade the adhesion of photoresist and adhesion promoters are used to render the surface non-polar [Koc07]. A common lithographic adhesion promoter is HMDS (HMDS: hexamethyl-di-silazane). It replaces adsorbed hydrogen with methyl-groups which bond at $135 \text{ }^\circ\text{C}$ to form a non-polar surface termination. The same procedure in accordance to lithographic processing conducted prior to substrate lamination on the dicing tape improves the adhesion and trench quality remarkably. Reliable dicing of 0.5 mm^2 fused silica chips at speeds up to $3.5 \text{ mm}/\text{sec}$ became feasible by means of HMDS coating (process parameters are given in Tab. B.20).

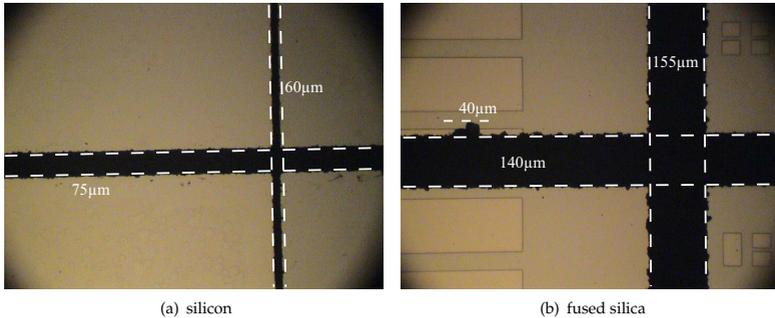


Fig. 2.43: Comparison of dicing trenches in silicon and fused silica.

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*In theory there is no difference between theory and practice.
In practice there is.*

Yogi Berra

3

A Capacitive Pressure Sensor on Fused Silica

THIS chapter describes a miniaturized surface micromachined capacitive pressure sensor fabricated on fused silica. The presented process is based on the technological details summarized in the preceding chapter which will be frequently referred to. Theoretical fundamentals on the transducer's mechanics and electrical behavior are required. These will be provided as well as a discussion of the implemented layout and fabricated prototypes. The chapter is organized as follows

1. **Analytic model of the plate transducer**

Analytic expressions for the transducer deflection and capacitance are derived. The general characteristics of capacitive pressure sensors are discussed. In addition, the influence of design factors are analyzed and possible operation modes are compared.

2. **Sensor concept**

The basic concept of the sensor is motivated and developed design variations are presented. The section highlights the impact of the sensor design on the final pressure sensor system discussing the implementation of reference cells and the sensor packaging.

3. **Sensor design and fabrication**

The sensor layout is presented in detail with notes on the fabrication process. Technological aspects are only discussed with focus on the special application and are based on the general technological description given in Chapter 2.

4. **Electromechanical modeling and characterization**

A design dependent overall sensor model is derived. The section contains simulation results of the static sensor characteristics such as offset capacitance and resistances. It is shown that the complex sensor geometry can be adequately modeled with a simplified equivalent circuit. The validity of the electromechanical model is demonstrated by comparison to characterization results of fabricated prototypes. In addition, distinct sensor characteristics are discussed such as: temperature coefficients, drift, and hysteresis.

3.1 Theory

This section summarized the theoretical fundamentals to design and model a capacitive surface-micromachined pressure sensor. Most of the presented formulas are well known, however, they are given in a dimensionless form especially adapted for surface-micromachined transducers having a fixed gap height and topography. The presented non-dimensional approach leads to generalization and makes the formula's appearance compact and intuitive.

Unfortunately, the oversimplified model of a rigidly clamped plate undergoing only small deflections does not lead to sufficiently accurate results suitable to design the transducer geometry. Layer stress (initial deflection), the elastic support (the topography of surface-micromachined transducers), and large deflections must be considered. This will be done in a handy way resulting in a simple analytical approximation of the mechanical transducer behavior with adequate accuracy.

operation modes

The operational range of the presented sensor is divided into two distinct modes: normal- and touch-mode operation. The transducer plate can deflect freely during normal operation until it touches the surface of the counter-electrode at touch-down pressure. At pressure loads beyond touch-down pressure, the transducer is in touch-mode operation and the contact area increases with increasing load. An analytical solution for the plate deflection during touch-mode operation is presented. The existing difficulty that the relation of pressure and touch-down radius can not be solved analytically for the radius as function of pressure is bypassed by means of dimensionless formulas. The presented approach allows to find an approximative expression which is of general validity for circular plate transducers.

The derived mechanical fundamentals are finally merged in Section 3.1.6 and applied to the realistic situation of a surface micromachined plate transducers. It follows an approximation for the magnitude of the deflection and the shape of the transducer's midplane profile. The sensor capacitance is calculated based on these results for normal- and touch-mode operation. The final analytical sensor model is sufficiently accurate for a transducer design. Additionally, it is used to illustrate the general characteristics of capacitive diaphragm type pressure sensors in Section 3.1.8 highlighting the distinct features of normal- and touch-mode transducers.

3.1.1 Deflection of circular plates under uniform load

The deflection of plates is extensively discussed in literature (see e.g. [Tim87], [Szi74], [Rei88], [Tim05]). Therefore, only a brief and intuitive derivation of the basic differential equation can be found in Appendix C.1.2. The presented formulas are based on the *Kirchhoff-Love* plate theory which is valid for small deflection to thickness ratios ($< 1/5$) of plates with intermediate thickness to lateral dimension ratios ($< 1/10$). The full set of premises for the applicability of the applied theory can be found in Appendix C.1.1.

According to the *Kirchhoff-Love* plate theory, the differential equation for the plate's midplane W as function of radial distance from the center R and an arbitrary con-

differential equation
of midplane profile

centric pressure load P equates to

$$\frac{1}{R} \left[R \left(\frac{1}{R} (R W_{,R}),_{,R} \right) \right]_{,R} = 32 P, \quad (3.1)$$

with the short hand form

$$\frac{\partial W}{\partial R} = W_{,R}$$

to represent partial derivatives. A detailed derivation of (3.1) can be found in Appendix C.1.2. The upper case characters indicate normalized quantities and the notation $W_{,R}$ denotes a partial derivative of W with respect to R .

Normalized quantities are made dimensionless with the scales summarized in Tab. 3.1. The individual scales are chosen in a way that the normalized variables: deflection W , radial position R , and touch-down radius R_t run from 0 to 1. The applied normalization is tailored for surface-micromachined transducers. It reflects the limited gap w_{\max} , which confines the vertical displacement. Additionally, the fixed gap allows the definition of a touch-down pressure p_t which is used as scale for the pressure load. It can be noted throughout the following sections that the implemented normalization simplifies the analytical and numerical calculations. Furthermore, graphs of normalized quantities are general.

Differential equation (3.1) can be integrated yielding the general solution for plate deflections caused by a uniform pressure load

general solution

$$W = P R^4 + \frac{C_1}{4} R^2 + C_2 \ln R + C_3 \quad (3.2)$$

which must be solved for the proper boundary conditions. Once such a solution is found, the radial and transverse bending moments M_R and M_T can be calculated. These are acting on the midplane and are functions of the plate's curvature (see definition (C.8))

bending moments

$$\begin{aligned} M_R &= - \left(W_{,RR} + \nu \frac{1}{R} W_{,R} \right) \\ M_T &= - \left(\frac{1}{R} W_{,R} + \nu W_{,RR} \right). \end{aligned} \quad (3.3)$$

The plate's curvature is directly related to the bending moments because the *Kirchhoff-Love* plate theory neglects all in-plane strain and assumes pure bending.

Stress within the transducer plate is of minor interest for capacitive pressure sensors. Their plate deflection determines the sensor output in contrast to piezo-resistive sensors having an output signal proportional the mechanical stresses within their transducer plate. Therefore the design of a capacitive pressure sensor must only ensure that the plate's yield stress is not exceeded at any location of the plate. The maximum stress is found at the surface of the plate and normalization of (C.5) gives

maximum bending stress

$$\begin{aligned} \Sigma_R &= -M_R \\ \Sigma_T &= -M_T. \end{aligned} \quad (3.4)$$

Table 3.1: Summary of dimensionless variables (D denotes the flexural rigidity (C.7)).

variable	definition	scale	comment
W	$= \frac{w}{w_{\max}}$	$w_{\max} = w_{\text{gap}} - w_{\min}$	plate deflection
W_0	$= \frac{w_0}{w_{\max}}$	$w_{\max} = w_{\text{gap}} - w_{\min}$	center deflection
P	$= \frac{p}{p_t}$	$p_t = \frac{64 D w_{\max}}{r_{\max}^4}$	uniform pressure load
R	$= \frac{r}{r_{\max}}$	r_{\max}	radial position
R_B	$= \frac{r_b}{r_{\max}}$	r_{\max}	bottom-electrode radius
\mathcal{H}	$= \frac{h}{w_{\max}}$	$w_{\max} = w_{\text{gap}} - w_{\min}$	plate thickness
R_t	$= \frac{r_t}{r_{\max}}$	r_{\max}	touch-down radius
M_R	$= \frac{m_R}{m_0}$	$m_0 = \frac{1}{64} p_t r_{\max}^2$	radial bending moment
M_T	$= \frac{m_T}{m_0}$	$m_0 = \frac{1}{64} p_t r_{\max}^2$	transverse bending moment
Σ_R	$= \frac{\sigma_R}{\sigma_0}$	$\sigma_0 = \frac{3}{32} \frac{p_t r_{\max}^2}{h^2}$	radial stress (bending)
Σ_T	$= \frac{\sigma_T}{\sigma_0}$	$\sigma_0 = \frac{3}{32} \frac{p_t r_{\max}^2}{h^2}$	transverse stress (bending)
Σ_M	$= \frac{\sigma_M}{\sigma_{m_0}}$	$\sigma_{m_0} = E \frac{w_{\max}^2}{r_{\max}^2}$	membrane stress (in-plane)
Ψ	$= \frac{\psi}{\psi_0}$	$\psi_0 = E w_{\max}^2$	membrane stress function

It can be noted that the normalized stresses are equal to the normalized bending moments. That is because pure bending is assumed. As consequence, the stresses are symmetrically distributed over the plate's thickness and are in direct relation to the acting moments (see (C.8)).

Special solutions for (3.2) are derived and discussed in the following subsections. These solutions consider rigidly and elastically clamped plates as well as the case of plates in touch-mode operation. Furthermore, the applicable range of the presented solutions will be expanded to large deflections in Section 3.1.5 considering the influence of in-plane strain.

3.1.2 Normal-operation (clamped edge)

Transducer plates in normal-operation can deflect freely with a center slope equal to zero. The slope at the edge must be zero for a rigidly clamped transducer as well as

the deflection along the circumference of the plate. Under these circumstances the boundary condition for (3.2) are

boundary condition
clamped

$$\begin{aligned} W^{(\text{clamped})} \Big|_{R=1} &\stackrel{!}{=} 0 && \text{no deflection at support} \\ W_{,R}^{(\text{clamped})} \Big|_{R=0} &\stackrel{!}{=} 0 && \text{zero slope at center} \\ W_{,R}^{(\text{clamped})} \Big|_{R=1} &\stackrel{!}{=} 0 && \text{zero slope at support} \end{aligned} \quad (3.5)$$

and result in the well known solution

midplane clamped

$$W^{(\text{clamped})} = P(1 - R^2)^2 \quad (3.6)$$

which is valid for pressure loads below touch-down pressure, i.e. $P = 0 \dots 1$. It can be noted that the deflection W is linearly related to the applied pressure load P in this most simplified case with a midplane profile as given in Fig. 3.6(a). The dimensional deflection can be calculated by re-scaling back to the dimensional variables

$$\frac{w}{w_{\max}} = \frac{p}{p_t} \left[1 - \left(\frac{r}{r_{\max}} \right)^2 \right]^2.$$

It can be noted that plate touch-down ($w/w_{\max} = 1$) occurs when p is equal to the touch-down pressure p_t , i.e. when the normalized load P and deflection W is unity. The touch-down pressure for small deflections of a clamped plate results from the normalization of (C.11) yielding (3.1) which is then solved for the boundary conditions (3.5):

touch-down
pressure

$$p_t^{(\text{clamped})} = \frac{64 D w_{\max}}{r_{\max}^4}. \quad (3.7)$$

The maximum deflection W_0 is found at the center where R is zero

maximum deflection
clamped

$$W_0^{(\text{clamped})} = P \quad \text{or} \quad w_0^{(\text{clamped})} = w_{\max} \frac{p}{p_t}. \quad (3.8)$$

Pasting the special solution (3.6) into (3.3) yields the bending moments, which are acting on the midplane of the clamped plate:

bending moments
clamped

$$M_R^{(\text{clamped})} = 4P(1 + \nu - R^2(3 + \nu)) \quad (3.9)$$

$$M_T^{(\text{clamped})} = 4P(1 + \nu - R^2(1 + 3\nu)). \quad (3.10)$$

At the same time, the stress at the plate surface is found with (3.4)

bending stress
clamped

$$\Sigma_R^{(\text{clamped})} = -4P(1 + \nu - R^2(3 + \nu)) \quad (3.11)$$

$$\Sigma_T^{(\text{clamped})} = -4P(1 + \nu - R^2(1 + 3\nu)) \quad (3.12)$$

being maximal at the edge where $R = 1$

$$\Sigma_{R_{\max}}^{(\text{clamped})} = 8P \quad (3.13)$$

$$\Sigma_{T_{\max}}^{(\text{clamped})} = 8P\nu. \quad (3.14)$$

It can be observed that, similar to the center deflection, the bending moments and bending stresses are linearly related to the applied load and are therefore proportional to the plate's local curvature. Example plots of bending moments versus radial position are given in Fig. 3.4(b).

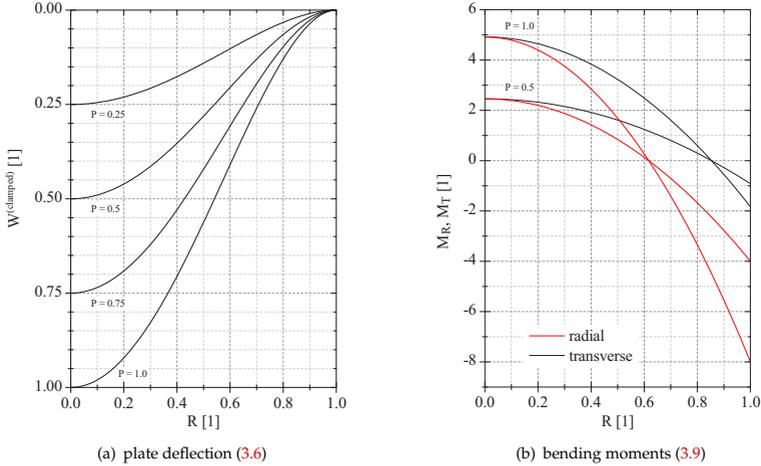


Fig. 3.1: Deflection and bending moments of plates undergoing small deflections. The moments are calculated for $\nu = 0.229$ (PBOR560).

3.1.3 Elastically clamped edge

Commonly surface-micromachined plates are fabricated on top of previously deposited and patterned layers. A complex topography can result if the actual transducer plate is conformally deposited on a layer stack. Topography at the plate edge leads to a compliant support and a surface-micromachined plate can no longer be considered as rigidly clamped. The deflection increases in comparison to a rigidly clamped transducer. As consequence of support compliance, it is not straightforward to chose a thicker sacrificial layer in order to increase the pressure range in normal operation. Increasing support compliance will even *lower* the touch-down pressure in certain cases.

A special solution of (3.2) for an elastically supported plate can be found by application of proper boundary conditions. Again, the slope at the plate center, and the

deflection at the edge is set to zero. The slope at the support must be proportional to the radial bending moments at the edge as defined by (3.3). This relation is assumed to be linear and is incorporated by means of compliance γ in the set of boundary conditions:

boundary conditions
elastic

$$\begin{aligned} W^{(\text{elastic})} \Big|_{R=1} &\stackrel{!}{=} 0 && \text{no deflection at support} \\ W_{,R}^{(\text{elastic})} \Big|_{R=0} &\stackrel{!}{=} 0 && \text{zero slope at center} \\ W_{,R}^{(\text{elastic})} \Big|_{R=1} &\stackrel{!}{=} \gamma M_R \Big|_{R=1} && \text{elastic support.} \end{aligned} \quad (3.15)$$

Solving (3.2) for these boundary conditions results in

$$W^{(\text{elastic})} = \frac{1 + \gamma(5 + \nu) - R^2(1 + \gamma(1 + \nu))}{(1 - R^2)(1 + \gamma(1 + \nu))} P(1 - R^2)^2. \quad (3.16)$$

It can be seen that the general geometry of the midplane surface is similar to that of a rigidly clamped plate. The deviation can be described by a function $F^{(\text{elastic})}$, which depends on compliance γ and R

midplane elastic sup-
port

$$\begin{aligned} W^{(\text{elastic})} &= F^{(\text{elastic})} W^{(\text{clamped})} \\ F^{(\text{elastic})} &= \frac{1 + \gamma(5 + \nu) - R^2(1 + \gamma(1 + \nu))}{(1 - R^2)(1 + \gamma(1 + \nu))}. \end{aligned} \quad (3.17)$$

The edge is fully clamped if the compliance γ is zero. It follows that solution (3.17) must approach the solution of a clamped plate for the limit $\gamma \rightarrow 0$, i.e. $F^{(\text{elastic})}$ must approach unity

$$\lim_{\gamma \rightarrow 0} W^{(\text{elastic})} = \frac{1 - R^2}{1 - R^2} P(1 - R^2)^2 = W^{(\text{clamped})}.$$

On the other hand, the solution for a simply supported plate must follow from solution (3.17) for the limit $\gamma \rightarrow \infty$, i.e. all bending moments at the edge must vanish because $M_R \neq 0$ would result in an infinite slope at the support

midplane simply
supported plate

$$\lim_{\gamma \rightarrow \infty} W^{(\text{elastic})} = \frac{5 + \nu - R^2(1 + \nu)}{1 + \nu} P(1 - R^2) = W^{(\text{simply})} \quad (3.18)$$

Importance of (3.17) for surface-micromachined transducers is stressed by Fig. 3.2(a). It can be observed, that the center deflection of the elastically clamped transducer may be 5 times higher than the displacement of a rigidly clamped plate (extreme case of a simply supported plate). However, γ of the presented sensor is measured to be approximately 0.02, i.e. the compliance of the support increases the deflection by approximately 8%. Fig. 3.2(a) illustrates that the general shape of the deflection profiles for small values of γ does not deviate significantly from the profile of

pressure scale
elastic support

a rigidly clamped plate. That is, an elastic support mainly changes the magnitude of the center deflection. In addition, (3.16) still provides a linear relation of load P and deflection magnitude as the case for a clamped plate. Therefore, by neglecting small geometric deviations, an approximation of (3.17) can be given in the form of (3.6) but with an adjusted pressure scale. Touch-down of the elastically supported plate center takes place at

$$W_0^{(\text{elastic})} = \frac{1}{K^{(\text{elastic})}} P \quad (3.19)$$

$$K^{(\text{elastic})} = \frac{1 + \gamma(1 + \nu)}{1 + \gamma(5 + \nu)}. \quad (3.20)$$

This result is illustrated in Fig. 3.2(b) giving $K^{(\text{elastic})}$ as function of compliance γ . It can be noted by comparison of (3.19) and (3.8) that $K^{(\text{elastic})}$ simply scales the touch-down pressure

$$p_t^{(\text{elastic})} = K^{(\text{elastic})} p_t^{(\text{clamped})}. \quad (3.21)$$

It follows that the deflection of an elastically supported plate with a moderate support compliance can be approximated with

$$W^{(\text{elastic})} = P^{(\text{elastic})} (1 - R^2)^2, \quad (3.22)$$

where $P^{(\text{elastic})}$ is normalized with $p_t^{(\text{elastic})}$.

bending moments
elastic support

The bending moments are calculated with deflection (3.17) and the general definition of the moments (3.3)

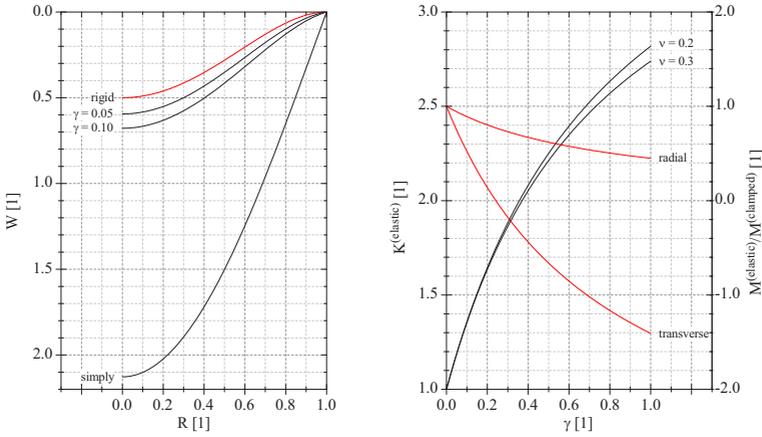
$$\begin{aligned} M_R^{(\text{elastic})} &= 4P \left(3 + \nu - R^2(3 + \nu) - \frac{2}{1 + \gamma(1 + \nu)} \right) \\ M_T^{(\text{elastic})} &= 4P \left(3 + \nu - R^2(1 + 3\nu) - \frac{2}{1 + \gamma(1 + \nu)} \right). \end{aligned} \quad (3.23)$$

The compliant support decreases the radial bending moments and for small values of γ also reduces the transverse moments. Fig. 3.2(b) illustrates this by giving the ratios of elastic and clamped plate bending moments at the transducer support. The radial and transverse stresses are, as always the case for small deflections, directly related to the bending moments by (3.4).

measurement of
support compliance

All the given formulas are of limited use if the actual numerical value of compliance γ is unknown. In practice it is difficult to calculate γ from the geometry of the edge support. However, the compliance can be obtained from geometric measurement data acquired at a known pressure load P . From condition three of (3.15) follows that

$$\left. \frac{w_{\max}}{r_{\max}} W_{,R}^{(\text{elastic})} \right|_{R=1} = \gamma \left. \frac{w_{\max}}{r_{\max}} M_R \right|_{R=1} \quad (3.24)$$



(a) deflection profiles (3.17) at $P = 0.5$ of rigidly, (b) increase of center deflection $K^{(elastic)}$ and bend-
 compliantly, and simply ($\gamma \rightarrow \infty$) supported plates ing moment ratios versus support compliance γ
Fig. 3.2: Influence of a compliant support on the plate deflection. The bending moment ratios
 were calculated at plate support for the respective touch-down pressure. (ν was let to 0.229 for
 all computations.)

must hold. This yields with (3.23) the compliance as function of load P

$$\tan \vartheta = -\gamma \frac{w_{\max}}{r_{\max}} \frac{8P}{1 + \gamma(1 + \nu)} \tag{3.25}$$

for a slope ϑ measured in radians at the edge support (see Fig. 3.3). Solving for γ leads to

$$\gamma = \frac{\tan \vartheta}{8 P \frac{w_{\max}}{r_{\max}} - (1 + \nu) \tan \vartheta}. \tag{3.26}$$

Slope ϑ should be measured at a pressure close to touch-down in order to achieve a good accuracy. However, it is unclear what scale for P should be applied in such a case because large deflection corrections may most likely be required (see Section 3.1.5). For this reason, it is important to note that only bending moments from small deflection theory enter the derivation of (3.26). Therefore, P is equivalent to w_0/w_{\max} (small deflections \rightarrow linear relation of P and W) and the compliance should be calculated from the measurement data of ϑ and w_0 with

$$\gamma = \frac{\tan \vartheta}{8 \frac{w_0}{r_{\max}} - (1 + \nu) \tan \vartheta}. \tag{3.27}$$

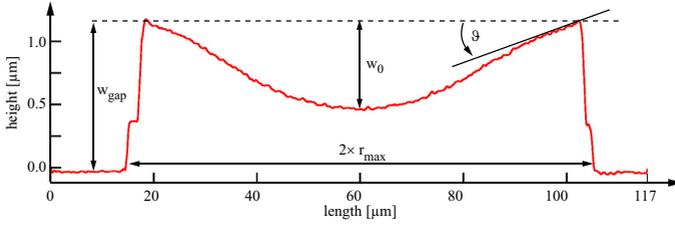


Fig. 3.3: Example surface profile of a transducer plate showing the affect and measurement of the support compliance γ . An angle $\theta > 0^\circ$ can be noted at the plate edge. The given profile was taken with a Keyence VK-9700 Series 3D laser scanning microscope.

3.1.4 Touch-down operation

A comprehensive discussion of a capacitive touch-mode pressure sensor is presented in [Hab95] but no explicit solution for the midplane profile and touch-mode capacitance is given. Numerical results for individual plate designs are presented and compared to measurement data in [Wan99] and [Ko99]. Furthermore, a power series solution is derived by [Men99] and a heuristic analytic approximation, originally suggested by [Ko99], is expanded and discussed in [Dai07].

A different approach to derive a solution for the midplane profile in touch operation is suggested in this section. It is an analogy to the solution of a ring plate. That is, the cross-section of a plate with a stiffened circular center region of radius r_t at a deflection of $w = w_{\max}$ has an identical midplane profile as a plate without reinforced center touching a counter electrode at distance w_{\max} with a touch-radius of r_t . Thus, the general differential equation (C.11) must be solved with the boundary conditions

$$\begin{aligned} W^{(\text{elastic})} \Big|_{R=1} &\stackrel{!}{=} 0 && \text{no deflection at support} \\ W_{,R}^{(\text{elastic})} \Big|_{R=R_t} &\stackrel{!}{=} 0 && \text{zero slope at touch-radius} \\ W_{,R}^{(\text{elastic})} \Big|_{R=1} &\stackrel{!}{=} 0 && \text{clamped edge} \end{aligned} \quad (3.28)$$

where $R_t = \frac{r_t}{r_{\max}}$ denotes the scaled radius of the reinforced plate center (or the plate section in touch with the counter surface). In addition, shearing force Q at the touch-down radius (edge of stiffened center region) must be equal to [Tim05]

$$\frac{r_{\max}}{p_t} Q \Big|_{R=R_t} \stackrel{!}{=} -\frac{P}{2} R. \quad (3.29)$$

This results in the deflection

$$W^{(\text{touch})} = P \left((1 - R)^2 + 2R_t^2(1 - R^2) + 4R_t^2 \ln R_t \right) \quad (3.30)$$

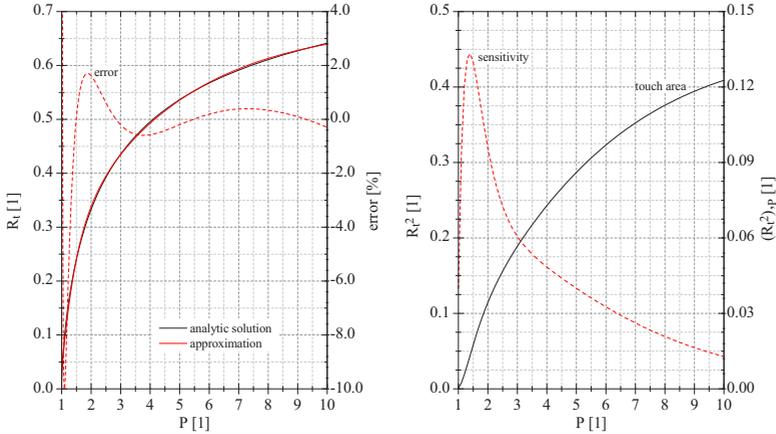
boundary conditions
touche-mode

shearing force
touch-mode

which approaches the solution of a clamped plate for $R_t \rightarrow 0$

$$\lim_{R_t \rightarrow 0} W^{(\text{touch})} = P(1 - R^2)^2 = W^{(\text{clamped})}. \quad (3.31)$$

Example touch-mode deflection profiles are presented in Fig. 3.5(a).



(a) touch-radius versus pressure (analytic solution (3.32), approximation (3.34), error of approximation) (b) non-dimensional touch-area and sensitivity (derivative of touch-area) versus pressure

Fig. 3.4: Comparison of the analytic solution and approximation for the touch-radius. Given is also the non-dimensional touch-area R_t and its derivative with respect to P (both calculated with (3.34)) being proportional to the sensitivity of a capacitive transducer during touch-operation.

Solution (3.30) seems to be reasonable but the relation of R_t and P is still unknown. It can be found by noting that the non-dimensional deflection W must be unity at $R = R_t$. Thus, solving (3.30) for touch-down pressure P at $R = R_t$ and $W = 1$ yields

$$P = \frac{1}{1 - R_t^4 + 4R_t^2 \ln R_t} \quad (3.32)$$

which can be pasted into (3.30) giving the midplane profile as function of R_t

$$W^{(\text{touch})} = \frac{(1 - R)^2 + 2R_t^2(1 - R^2) + 4R_t^2 \ln R_t}{1 - R_t^4 + 4R_t^2 \ln R_t}. \quad (3.33)$$

Unfortunately, the required inverse relation of (3.32), i.e. for R_t as function of P can not be given analytically. However, the function

pressure vs touch-radius

midplane touch-mode

approximation of touch-radius

$$R_t = R_{t0} + R_{t1} (1 - e^{-P/P_1}) + R_{t2} (1 - e^{-P/P_2}) \quad (3.34)$$

can be fitted to (3.32). It must be noted that approximation (3.34) is free of any geometry or material parameter because of the applied parameter scaling procedure. For this reason, this fit can be used as a general solution to calculate the touch-radius as function of pressure for all circular plates undergoing small deflections. Therefore, a general solution for the midplane during touch-down is obtained when (3.34) and (3.33) are used in succession to calculate touch-radius and deflection. Some example midplane profiles are presented in Fig. 3.5(a).

The suggested fit is compared to the analytic solution in Fig. 3.6(a) also displaying the error caused by the approximation. The fit coefficients summarized in Tab. 3.2 result in an error for the non-dimensional touch-area R_t^2 smaller 4% for $1.5 \leq P < 10$ and smaller 20% for $1 \leq P < 1.5$ (see Fig. 3.6(a)). The touch-area, i.e. R_t^2 is of special interest because it will turnout that the capacitance of a transducer in touch-operation is basically determined by this area. For this reason, Fig. 3.4(b) presents the touch-area versus applied pressure and its derivative with respect to P being proportional to the capacitive transducer's sensitivity.

Table 3.2: Summary of non-dimensional coefficients for touch-radius approximation (3.34) fitted for three different pressure ranges.

variable	$P^{(\max)} = 5$	$P^{(\max)} = 10$	$P^{(\max)} = 25$
R_{t0}	-62.851	-1.3463	-0.78215
R_{t1}	62.630	1.4843	1.07616
R_{t2}	0.79186	0.53164	0.44456
P_1	0.15938	0.51184	0.76055
P_2	1.6779	3.6009	6.4474

Radial and transverse bending moments can be calculated from deflection (3.33) and the general definition of radial and transverse bending moments (3.3)

$$M_R^{(\text{touch})} = 4 \frac{R_t^2 (\nu - 1 - R^2(1 + \nu)) - R^2 (1 + \nu - R^2(3 + \nu))}{R^2(1 - R_t^4 + 4R_t^2 \ln R_t)} \quad (3.35)$$

$$M_T^{(\text{touch})} = 4 \frac{R_t^2 (1 - \nu - R^2(1 + \nu)) - R^2 (1 + \nu - R^2(3 + \nu))}{R^2(1 - R_t^4 + 4R_t^2 \ln R_t)}. \quad (3.36)$$

Example calculations of bending moments at different touch-radii are presented in Fig. 3.5(b). They indicate that most of the energy is stored in radial moments. Pure bending is assumed and therefore the normalized stresses are equal to the negative normalized moments given by (3.4).

The maximum pressure $P^{(\max)}$, which will cause an output change of a capacitive sensor is reached when touch-radius R_t is equal to the bottom-electrode radius R_B .

bending moments touch-mode

maximum pressure causing a capacitance change

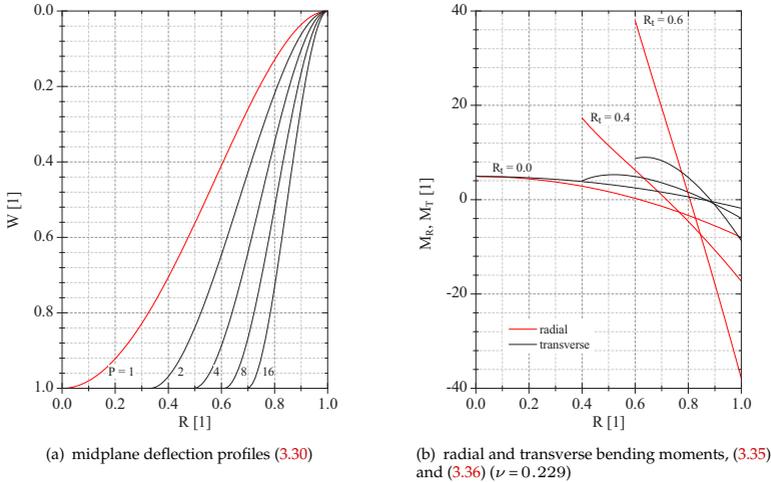


Fig. 3.5: Midplane deflection profiles and bending moments in touch-mode operation.

It can be calculated with (3.32) yielding

$$P^{(\max)} = \frac{1}{1 - R_B^4 + 4R_B^2 \ln R_B}. \quad (3.37)$$

$P^{(\max)}$ increases rapidly with increasing bottom-electrode radius as can be observed in Fig. 3.16(a) further below. Similarly, the maximum radial bending stress increases strongly with the touch-radius (see Fig. 3.16(b)). Therefore, the bottom-electrode radius R_B of a sensor solely designed for touch-operation should not be greater than 0.75 as can be concluded from the summarizing discussion in Section 3.1.8.

3.1.5 Large deflections and membrane stress

In this section, a linear and a non-linear approximation for the midplane profile under large deformations are derived. It is the goal to improve the accuracy of the already discussed formulas and to extend their validity for practical application without losing simplicity.

The preceding sections assumed small deflections. Whether a deflection may be considered being small or not can be assessed with the ratio of

$$\mathcal{H} = \frac{h}{w_{\max}} \quad (3.38)$$

measuring the transducer thickness h in terms of the maximum deflection w_{\max} . The error of $W^{(\text{clamped})}$ will be below 2% in cases where \mathcal{H} exceeds 5 (see the de-

viation of small and large deflection touch-down pressure in Fig. 3.6(a)). Under these circumstances, most of the elastic energy is stored in bending stresses. As \mathcal{H} decreases, the midplane is increasingly strained and approaches asymptotically the shape of a deflected membrane where no bending moments are present any more and all energy is stored as in-plane strain. Therefore, a decreasing \mathcal{H} causes the actual deflection to deviate non-linearly from the linear relation of load and center deflection (3.8) predicted by the small displacement approach. Already for $\mathcal{H} = 1$, a common situation for a surface-micromachined transducer plate, the deflection at $P = 1$ is underestimated by approximately 30%.¹ This shows that small deflection approaches does not lead to a satisfactory prediction of the touch-down pressure in many practical cases.

approximate deflection during large displacements

Beyond touch-down, the midplane undergoes virtually no further strain and the formulas for touch-mode operation can be derived as presented in Section 3.1.4 assuming pure bending. Therefore, it is appropriate to use large deflection theory to predict an accurate touch-down pressure $p_t^{(\text{large})}$ as scale for the deflection magnitude, but to maintain the linear relation of load and center deflection. With this approach, the approximated center deflection intersects the non-linear large displacement solution at touch-down pressure. Such a solution generally underestimates the deflection magnitude during normal operation but the simple small-deflection formulas for normal- and touch-mode operation can still be used. Most important, the transition between normal- and touch-mode operation can be predicted accurately.

Radial and transverse membrane in-plane stress σ_{mr} and σ_{mt} needs to be considered for large plate deflections. This can be achieved by means of a stress function ψ with the properties [Tim05]

$$\sigma_{mr} \Big|_{z=0} = \frac{\psi_{,r}}{r}, \quad \sigma_{mt} \Big|_{z=0} = \psi_{,rr} \quad (3.39)$$

which is integrated in the set of differential equations for the deflection w as can be found in [Tim05]

$$\begin{aligned} \nabla_r^4 w - \frac{h}{r} (\psi_{,r} w_{,r})_{,r} &= \frac{p}{D} \\ \nabla_r^4 \psi + \frac{E}{r} w_{,r} w_{,rr} &= 0. \end{aligned}$$

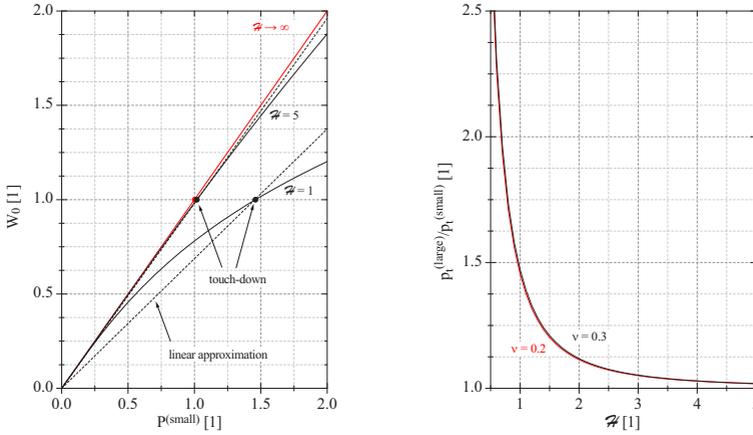
The ansatz

$$w = w_0 \left(1 - \frac{r^2}{r_{\max}^2} \right)^2 \quad (3.40)$$

$$\psi = w_0^2 (b_1 r^2 + b_2 r^4 + b_3 r^6 + b_4 r^8) \quad (3.41)$$

¹ The actual error also depends on ν as will be shown further below.

differential equations large-deflection



(a) center deflection according to small (3.6) and large (3.46) displacement theory, and linear approximation of large displacements with (3.53) and (3.54) ($\nu = 0.229$)

(b) touch-down pressure shift due to membrane stress versus \mathcal{H} for large displacements calculated with (3.53)

Fig. 3.6: Influence of membrane stress on the center deflection. (Small displacement theory is approached asymptotically for normalized plate thickness $\mathcal{H} \rightarrow \infty$). The suggested linear approximation (3.53) for large displacements intersects the non-linear solution at plate touch-down.

leads to

$$\psi = w_0^2 E \left(\frac{1}{12} \frac{5 - 3\nu}{1 - \nu} \frac{r^2}{r_{\max}^2} - \frac{1}{4} \frac{r^4}{r_{\max}^4} + \frac{1}{9} \frac{r^6}{r_{\max}^6} + \frac{1}{48} \frac{r^8}{r_{\max}^8} \right) \quad (3.42)$$

and to the relation

$$\frac{w_0}{w_{\max}} + \kappa \left(\frac{w_0}{w_{\max}} \right)^3 \left(\frac{w_{\max}}{h} \right)^2 = \frac{p r_{\max}^4}{D w_{\max}} \quad (3.43)$$

with $\kappa = \frac{(1 + \nu)(23 - 9\nu)}{56}$.

Stress function (3.42) and reads with the scales summarized in Tab. 3.1 as

$$\Psi = W_0^2 \left(\frac{1}{12} \frac{5 - 3\nu}{1 - \nu} R^2 - \frac{1}{4} R^4 + \frac{1}{9} R^6 + \frac{1}{48} R^8 \right) \quad (3.44)$$

and (3.43) reduces to

$$W_0 + \frac{\kappa}{\mathcal{H}^2} W_0^3 = P. \quad (3.45)$$

normalized stress function

center deflection
large displacement

It can be solved for the center deflection W_0 with the real solution

$$W_0 = \sqrt[3]{\frac{\Lambda}{18} \frac{1}{\kappa}} - \sqrt[3]{\frac{2}{3\Lambda}} \mathcal{H} \quad (3.46)$$

with $\Lambda = \mathcal{H}^2 \left(9\kappa^2 P + \sqrt{3\kappa^3(4\mathcal{H}^2 + 27P^2\kappa)} \right)$.

midplane large
deflection

Ansatz (3.40) assumes identical small- and large-deflection midplane geometries. Solely the magnitude of the center deflection is scaled in (3.46) accounting for the present membrane stress by means of parameter \mathcal{H}

$$W^{(\text{large})} = W_0(P, \mathcal{H}) (1 - R^2)^2. \quad (3.47)$$

Small and large displacement theory deviates with increasing center deflection because of the increasing magnitude of membrane stress. This can be observed in Fig. 3.6 which compares both approaches and gives the ratio of $p_t^{(\text{large})}/p_t^{(\text{small})}$ as function of \mathcal{H} .

affect of mem-
brane stress on
touch-pressure

However, (3.46) is not very handy but it can be used to calculate a more accurate large deflection touch-down pressure $p_t^{(\text{large})}$ for the purpose of re-scaling all previous results. Therefore, it can be noted, that $W_0 = 1$ must hold at plate touch-down, thus, solving (3.46) for the wanted P yields

$$P = 1 + \frac{\kappa}{\mathcal{H}^2}. \quad (3.48)$$

That is, the actual touch-down pressure is increase by $\frac{\kappa}{\mathcal{H}^2}$ due to the in-plane membrane stress. The magnitude of this stress scales with \mathcal{H}^{-2} and is depicted in Fig. 3.6(b). From the same figure can be noted that ν , which enters the equation through κ , has only a negligible effect on the touch-down pressure shift. The in-plane stress distribution can be calculated from (3.44) and (3.39) giving a radial component of

$$\Sigma_{\text{MR}} = W_0^2 \left(\frac{5 - 3\nu}{6(1 - \nu)} - R^2 + \frac{2}{3}R^4 - \frac{1}{6}R^6 \right). \quad (3.49)$$

This membrane stress has its maximum at the plate center

$$\Sigma_{\text{MR}_{\text{max}}} = W_0^2 \frac{5 - 3\nu}{6(1 - \nu)} \quad (3.50)$$

with the actual magnitude of

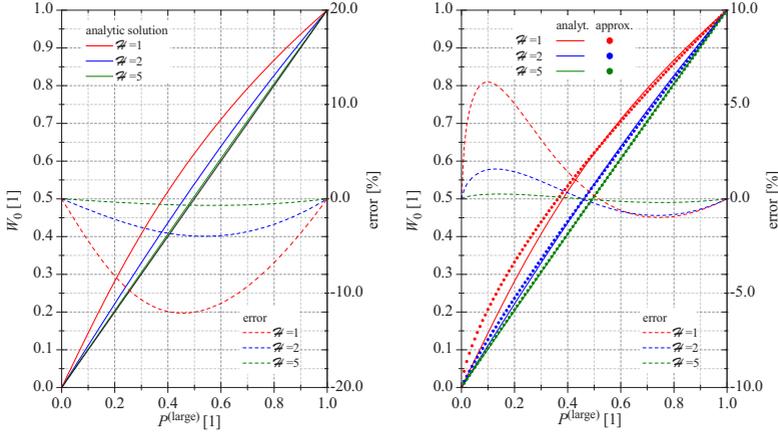
$$\Sigma_{\text{MRT}} = \frac{5 - 3\nu}{6(1 - \nu)} \quad (3.51)$$

at plate touch-down where W_0 is unity. It can be noted that $\sqrt{\Sigma_{\text{MR}}}$ is proportional to W_0 and that for a linear approximation of the deflection ($W_0 \propto P$) also $\sqrt{\Sigma_{\text{MR}}} \propto P$

must hold. Therefore, (3.48) can be extended for such an approximation to

$$P = 1 + \frac{\kappa}{\mathcal{H}^2} \sqrt{\frac{\Sigma_M}{\Sigma_{MRT}}} = 1 + \frac{\kappa}{\mathcal{H}^2} \sqrt{\frac{\Sigma_F + \Sigma_{MRT}}{\Sigma_{MRT}}} \quad (3.52)$$

where Σ_M accounts for the overall present in-plane stress. This stress may be the sum of the in-plane stress due to large-deflection Σ_{MRT} and an initial stress of the transducer film Σ_F . If no initial stress is present, (3.52) reduces to (3.48) at plate touch-down.



(a) center deflections (3.46) in comparison to linear approximation (3.53) (b) center deflections (3.46) in comparison to non-linear approximation (3.55)

Fig. 3.7: Center deflection for large displacements in comparison to linear and non-linear approximations. (The error is given relative to w_{max} assuming $\nu = 0.229$.)

A linear approximation of the plate deflection accounting for in-plane stresses and which intersects the true non-linear solution at touch-down pressure can be given:

$$W^{(large)} \approx P^{(large)} (1 - R^2)^2 \quad (3.53)$$

with the large deflection scale $P^{(large)} = p/p_t^{(large)}$ provided by (3.52)

$$p_t^{(large)} = K^{(large)} p_t^{(small)}$$

with
$$K^{(large)} = 1 + \frac{\kappa}{\mathcal{H}^2} \sqrt{\frac{\Sigma_F}{\Sigma_{MRT}}} + 1. \quad (3.54)$$

The linear approximation's accuracy increases with \mathcal{H} , i.e. the more the deflection approaches the linear small-deflection case (see Fig. 3.7(a) and Fig. 3.6(a)). The error

linear approximation
midplane large
deflection

is given in Fig. 3.7(a) being smaller 12% for $\mathcal{H} = 1$.

A more accurate calculation of the plate deformation for cases $\mathcal{H} < 5$ can be obtained with

$$W^{(\text{large})} \approx \left[P^{(\text{large})} \right]^{1 + \frac{\kappa}{\mathcal{H}^2}} (1 - R^2)^2. \quad (3.55)$$

This non-linear relation is found heuristically and provides more accurate results especially for $W_0 > 0.4$ as can be observed in Fig. 3.7(b).

3.1.6 Deflection of surface-micromachined plates

This section assembles the collection of individual and detached results from the preceding calculations. It provides a recipe for a step by step approximation of the midplane profile of a surface-micromachined plate. Before hands, the common difficulties which must be met are summarized and illustrated.

The discussions of the preceding sections showed that the most simplified approach of a rigidly clamped plate undergoing small deflections usually leads to large deviations between measurement and model data for surface-micromachined plates. Reasons for these deviations are in first place topography and in-plane stress. The stress may be either caused by the fabrication process or by large displacements. The effect of stress and topography on the deflection of a plate is illustrated in Fig. 3.9. It summarizes the resulting center deflections w_0 at 0 bar and 1 bar load for various topographies and plate stress levels obtained by means of FEM simulations. The numerical computations were run on *COVENTOR-Ware* for a typical sensor geometry which corresponds to *Design-1* presented in Section 3.2.1. Cross-sections of the modeled plate quarters are depicted in Fig. 3.9(c).² Fig. 3.9(a) clearly shows that film stress causes a bending moment at the support which must be balanced resulting in an initial plate deflection being proportional to the magnitude of stress and the compliance of the support. Furthermore, Fig. 3.9(b) shows that the plate topography and the compliance of the support influences the magnitude of the deflection under pressure load. Radial embossments, as caused by the bottom-feedthroughs, increase the rigidity slightly (compare the results for model 4 and 5 in Fig. 3.9).

A different view of the same problem is presented in Fig. 3.10 depicting plots of center deflection versus pressure of a plate affected by bottom-electrode topography. It can be noted that the deflection seems to become more linear the higher the membrane stress level is. However, these plots would be very similar if they would have been scaled with their individual touch-down pressure. It can be observed that the sensitivity generally decreases with increasing membrane stress. Furthermore, sensitivity generally increases with increasing topography. And again, an initial deflection at 0 bar can be observed for the modeled cases being proportional to the stress level and the topography. More FEM results are summarized in Fig. C.5 and Fig. C.6 showing typical variations of the center deflection caused by fabrication process dependent layer thickness variations affecting the transducer compliance.

Unintentional sealant deposition within vacuum sealed sensor cavity is an additional difficulty during sensor modeling. The problem is described in Section 3.3.5

² The modeled plates are of rotational symmetry but *COVENTOR-Ware* provides only cartesian symmetry boundary conditions, i.e. at least a quarter of a plate must be modeled.

non-linear approx-
imation midplane
large deflection

effect of stress
and topography

effect of seal-
ing procedure

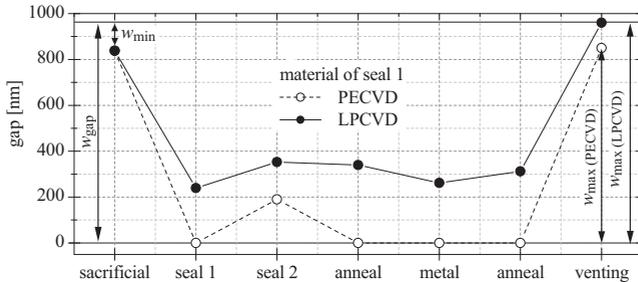
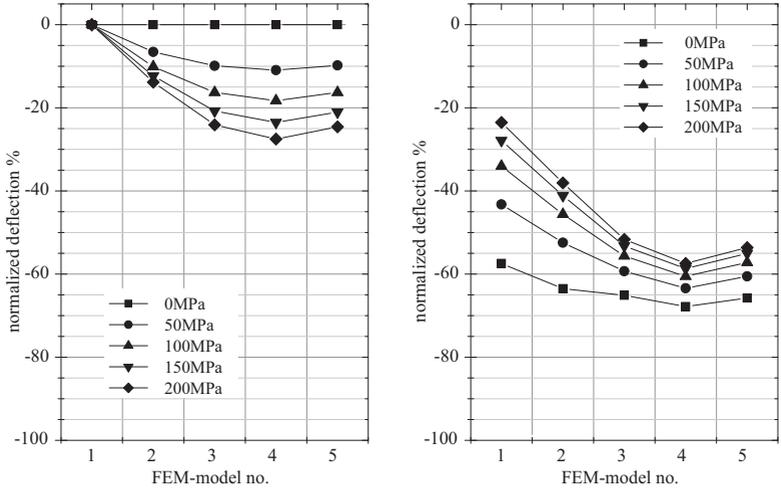


Fig. 3.8: Comparison of the center deflection w_0 during the process flow of two identical transducers, one sealed with LPCVD and the other with a PECVD oxide (seal 1). Seal 2 is an additional second PECVD nitride passivation layer simultaneously deposited on both presented samples. The deflection is given after the indicated process steps (deposited layers are patterned). The initial deflection w_{\min} caused by stress must be noted. The effect of sealant deposition within the cavity is apparent in the deflection after venting. The data was taken with a Keyence VK-9700 Series 3D laser scanning microscope.

showing that the amount of sealant within the cavities can not be neglected for LPCVD sealants. Approximately 45 nm were measured on the inner walls after vacuum sealing with LTO and TEOS in case of the presented sensor (see Fig. 3.39). A far lower influence on the mechanical sensor characteristics were measured for PECVD sealants. In these cases, the penetration depth during sealant deposition is much lower, as discussed in Section 2.3.1, and almost not sealant can be found within the cavity. The impact of the sealant on the mechanical performance of the sensor is highlighted by Fig. 3.8. It compares the measured gap at atmospheric pressure of identical transducers after sealing with LPCVD TEOS and PECVD If-oxide. It can be observed that both sensors have identical effective gaps after sacrificial layer removal. It is equal to the fabricated gap w_{gap} minus an initial deflection w_{\min} caused by stress in the transducer layer in conjunction with the compliant support. The PECVD oxide sealed sensor touches the counter electrode after sealant deposition and patterning, while there is still a gap of 240 nm measured for the TEOS sample. It can be further noted, that the PECVD sealed sensor returns to the initial gap after venting but that the gap of the TEOS sample is increased. This is due to a stress which is exerted by the TEOS onto the inner surface of the transducer plate.

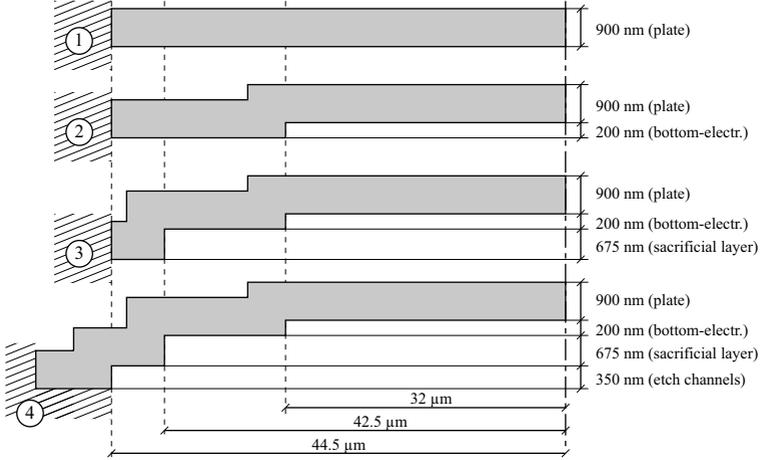
Effects which should be included in a sensor model of practical use are:

1. The topography of the plate renders the support compliant decreasing p_t .
2. Large deflections must be assumed in most practical cases (for $\mathcal{H} < 5$) causing in-plane strain and increasing p_t .
3. Film stress may be present which increases p_t .
4. A plate with topography under a non-zero film stress will also have an initial deflection at $p = 0$ decreasing the effective gap and re-scaling p_t .
5. Radial embossments in the transducer plate increase its rigidity and p_t .



(a) 0 bar center deflection for the topographies given in Fig. 3.9(c)

(b) 1 bar center deflection for the topographies given in Fig. 3.9(c)



(c) cross-sections of simulated transducer plate topographies

Fig. 3.9: FEM simulation results for the center deflection w_0 of plates with various topographies at two pressure loads. The geometries ① through ④ are of rotational symmetry. Model ⑤ is similar to model ④ but also integrates the topography of radial bottom-electrode leads (not illustrated) breaking the symmetry.

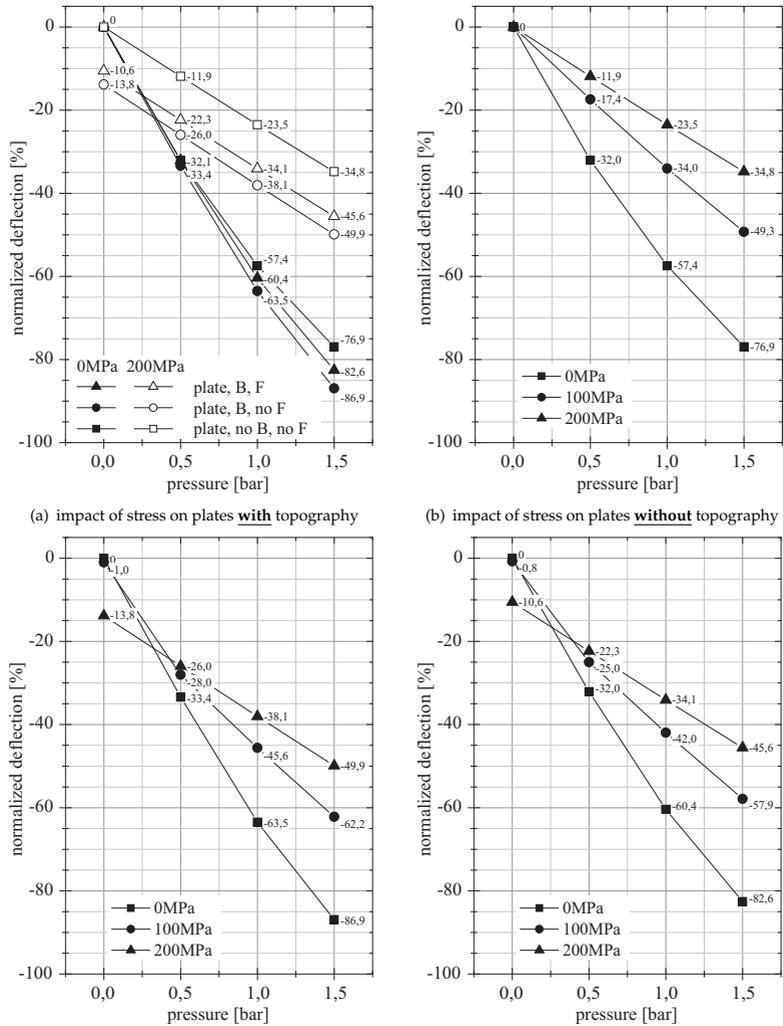


Fig. 3.10: FEM simulation results for the center deflection of plates based on model geometry ② depicted in Fig. 3.9(c). Deviations from the standard model are indicated: B (bottom-electrode), F (feedthrough).

Two additional difficulties exist for vacuum sealed cavities:

6. Entrapped gas within the sensor cavity increases p_t . The gas may originate from the sealing process but could also result from outgassing of incorporated gas residuals or any other organic residuals.
7. Sealant may be deposited inside of the sensor cavity making the transducer more rigid. In such a case a stress gradient within the transducer layer stack is also very likely which will cause non zero bending moments at zero load.

Effects 1–6 can be included in an analytical model by using the approximative formulas presented in the sections 3.1.1 through 3.1.5. The model requires the knowledge of the transducer geometry, the mechanical properties of the transducer material, and two additional quantities which need to be measurement

- minimum center deflection w_{\min} at zero pressure
- slope ϑ at the membrane support and center deflection w_0 at a pressure $p < p_t$.

step by step modeling procedure

The step by step modeling procedure is as follows:

1. **maximum effective gap:**

Residues or sealant material with a thickness $t_{\text{res}} = t_s + t_r$ (see Fig. 3.11(a)) and the initial deflection w_{\min} due to stress and topography reduces the fabricated gap height w_{gap} to a maximum effective gap of

$$w_{\max} = w_{\text{gap}} - w_{\min} - t_{\text{res}}. \quad (3.56)$$

2. **touch-down pressure for the rigidly clamped plate:**

$p_t^{(\text{clamped})}$ is calculated with (3.7). A non-zero cavity pressure p_{cav} from the sealing process or due to outgassing must be added to the calculated touch-down pressure.

3. **compliance of the support:**

Support compliance γ can be calculated from (3.27) with the measured values for ϑ and w_0 . The influence of the elastic support is incorporated in the scale coefficient $K^{(\text{elastic})}$ as given by (3.20).

4. **membrane stress:**

The influence of large deflection (i.e. deflections in cases where $\mathcal{H} < 5$ holds) membrane stresses or film stress from the fabrication process is incorporated in the scale coefficient $K^{(\text{large})}$ as given by (3.54).

5. **touch-down pressure of the real transducer:**

The actual pressure scale for the transducer can be calculated with

$$p_t^{(\text{real})} = K^{(\text{elastic})} K^{(\text{large})} \left(p_t^{(\text{clamped})} + p_{\text{cav}} \right). \quad (3.57)$$

All subsequent calculations are done with the non-dimensional pressure

$$P = \frac{p}{p_t^{(\text{real})}}. \quad (3.58)$$

6. **transducer deflection:**

Finally, the deflection can be calculated with (3.6), (3.33), and (3.34) together with the coefficients given in Tab. 3.2:

$$\begin{aligned}
 W &= P(1 - R^2)^2 && \text{for } P \leq 1 \\
 \left. \begin{aligned}
 R_t &= R_{t0} + R_{t1} (1 - e^{-P/P_1}) \\
 &+ R_{t2} (1 - e^{-P/P_2}) \\
 W &= \frac{(1 - R)^2 + 2R_t^2(1 - R^2) + 4R_t^2 \ln R_t}{1 - R_t^4 + 4R_t^2 \ln R_t}
 \end{aligned} \right\} && \text{for } P > 1
 \end{aligned}$$

3.1.7 Capacitance of circular plates

Once the transducer’s deflection profile is known its capacitance needs to be calculated. The actual overall capacitance composes of two parts: an offset value and the capacitance of the pressure deformed transducer plate. The offset is caused by the membrane support which overlaps the bottom-electrode leads. It will be calculated in Section 3.4.1 and is not considered in the following discussion which focuses on the capacitance of the circular plate located over an insulated bottom-electrode.

It is the intention of this section to provide analytic expressions for the capacitance of pressure deformed plates in normal- and touch-mode operation. These calculations must be as accurate as possible to be meaningful during the sensor characterization. Therefore, not only the deflection must be included accurately but also all additional dielectrics within the cavity. This will become especially important during touch-down where the sensor characteristics are determined by the touch-down area and the dielectric between the two sensor electrodes.

The cross-sectional view of the sensor chamber as considered in the following calculations is given in Fig. 3.11. It can be observed that the dielectrics within the cavity are the bottom-electrode insulation, the unintentionally deposited sealant, and the gap creating the capacitances C_i , $C_{s,r}$ and C_g , respectively. The individual thicknesses of these layers are t_i , $t_{s,r}$ and w , as indicated in Fig. 3.11(a). The resulting differential capacitances are

insulation structure and individual contributions

$$dC_g = \epsilon_0 \frac{2\pi r dr}{w_{\max} - w}, \tag{3.59}$$

$$dC_i = \epsilon_0 \epsilon_i \frac{2\pi r dr}{t_i} \tag{3.60}$$

$$dC_s = \epsilon_0 \epsilon_s \frac{2\pi r dr}{t_s} \tag{3.61}$$

if angular symmetry is considered. Roughness of the contact surfaces is of minor importance in normal operation but has a serious impact after plate touch-down. It is therefore included as C_r for both cases: normal and touch operation. The rough surface is modeled as a mixture of vacuum with ϵ_0 and a second material ϵ_r . This material may be the sealant but might also be the insulation if no sealant has pene-

contribution of surface roughness

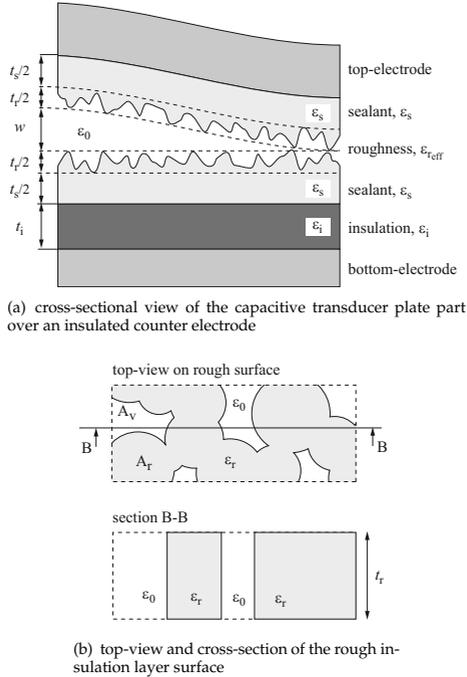


Fig. 3.11: Dielectric structure of a capacitive absolute pressure transducer as considered for the present case. The rough surface within the sealed cavity is modeled as a compound of two dielectrics with an irregular pillar structure.

trated into the cavity. The rough layer has a thickness of t_r and an effective permeability $\epsilon_{r,eff}$ which can be calculated in different ways. Here, a pillar like structure is assumed as depicted in Fig. 3.11(b). That is, all pillars have the same height t_r but individual diameters and shapes resulting in an overall area fraction A_v/A_r of vacuum and the material with ϵ_r . This gives a differential capacitance of

$$dC_r = \epsilon_0 \epsilon_r \frac{1}{\zeta + 1} \frac{2\pi r dr}{t_r} + \epsilon_0 \frac{\zeta}{\zeta + 1} \frac{2\pi r dr}{t_r} \tag{3.62}$$

with $\zeta = \frac{A_v}{A_r}$

or expressed with an effective permeability

$$dC_r = \epsilon_0 \epsilon_{r\text{eff}} \frac{2\pi r dr}{t_r} \quad (3.63)$$

$$\text{with } \epsilon_{r\text{eff}} = \frac{\epsilon_r + \zeta}{\zeta + 1}.$$

The individual capacitances are connected in series and yield the overall differential capacitance of

$$\frac{1}{dC} = \frac{1}{dC_g} + \frac{1}{dC_i} + \frac{1}{dC_s} + \frac{1}{dC_r} \quad (3.64)$$

$$\frac{1}{dC} = \frac{(w_{\text{max}} - w) + \frac{t_i}{\epsilon_i} + \frac{t_s}{\epsilon_s} + \frac{t_r}{\epsilon_{r\text{eff}}}}{2\pi\epsilon_0 r dr}.$$

The influence of all additional dielectrics besides the vacuum gap can be summed up in a parameter β

$$\beta = \frac{t_i}{\epsilon_i w_{\text{max}}} + \frac{t_s}{\epsilon_s w_{\text{max}}} + \frac{t_r}{\epsilon_{r\text{eff}} w_{\text{max}}} \quad (3.65)$$

lumped affect of dielectric stack

being zero for a pure vacuum capacitance with no additional insulation. In this way, the total differential capacitance can be written as

$$dC = \frac{2\pi\epsilon_0 r dr}{w_{\text{max}}(1 + \beta) - w} \quad (3.66)$$

overall differential capacitance

which reduces for a transducer with no additional dielectric insulation ($\beta = 0$) to simply

$$dC = \frac{2\pi\epsilon_0 r dr}{w_{\text{max}} - w}. \quad (3.67)$$

Normal-mode operation

The transducer plate can deform freely until $P = 1$ resulting in a midplane profile as given by (3.6). The transducer capacitance during normal operation of an individual plate composes of a static offset capacitance C_{offset} and of a pressure dependent normal-mode capacitance C_n

$$C^{(\text{normal})} = C_{\text{offset}} + C_n. \quad (3.68)$$

The calculation of C_{offset} will be discussed in Section 3.4.1.

C_n is obtained by integrating (3.66) over the bottom-electrode surface which is in most practical cases smaller than the surface of the transducer plate. This leads for

a circular geometry and a bottom-electrode radius of $r_b < r_{\max}$ to

$$C_n = \epsilon_0 \pi \int_0^{r_b} \frac{2r}{w_{\max}(1+\beta) - w} dr. \quad (3.69)$$

This integral is made dimensionless with the scales given in Tab. 3.1

$$\frac{C_n}{C_z} = \frac{1}{P} \int_0^{R_B} \frac{2R}{\frac{1}{P}(1+\beta) - (R^2 - 1)^2} dR \quad (3.70)$$

where C_z denotes the capacitive scale given by the vacuum capacitance of an undeflected plate at zero pressure load with radius r_{\max} at distance w_{\max} to a counter electrode

$$C_z = \frac{\epsilon_0 \pi r_{\max}^2}{w_{\max}}. \quad (3.71)$$

Integral (3.70) can be transformed with the substitution $X = R^2 - 1$ to the standard integral

$$\frac{C_n}{C_z} = \frac{1}{P} \int_{-1}^{R_B^2-1} \frac{1}{\frac{1}{P}(1+\beta) - X^2} dX \quad (3.72)$$

which can be integrated with the primitive [Bro00]

$$\int \frac{dx}{x_0^2 - x^2} = \frac{1}{2x_0} \ln \frac{x_0 + x}{x_0 - x} \quad |x| < x_0. \quad (3.73)$$

The solution for a single circular capacitive transducer plate in normal operation equates to

single cell capacitance

$$\frac{C_n}{C_z} = \frac{1}{2} \frac{1}{\sqrt{P(1+\beta)}} \ln \left[\frac{\sqrt{\frac{1+\beta}{P}} + R_B^2 - 1}{\sqrt{\frac{1+\beta}{P}} - R_B^2 + 1} \frac{\sqrt{\frac{1+\beta}{P}} + 1}{\sqrt{\frac{1+\beta}{P}} - 1} \right] \quad (3.74)$$

for the general case and reduces to the well-known solution

$$\frac{C_n}{C_z} = \frac{1}{2} \frac{1}{\sqrt{P}} \ln \left[\frac{\sqrt{\frac{1}{P}} + 1}{\sqrt{\frac{1}{P}} - 1} \right]$$

for a vacuum capacitance having a bottom-electrode radius identical to the plate

radius.

The minimum and maximum capacitance during normal operation are found by taking the limit $P \rightarrow 0$ and $P \rightarrow 1$ of (3.74)

minimum and maximum capacitance

$$\frac{C_n^{(\min)}}{C_z} = \lim_{P \rightarrow 0} \frac{C_n}{C_z} = \frac{R_B^2}{1 + \beta} \tag{3.75}$$

$$\frac{C_n^{(\max)}}{C_z} = \lim_{P \rightarrow 1} \frac{C_n}{C_z} = \frac{1}{2\sqrt{1 + \beta}} \ln \left[\frac{\beta + (\sqrt{1 + \beta} + 1)R_B^2}{\beta - (\sqrt{1 + \beta} - 1)R_B^2} \right]. \tag{3.76}$$

Example capacitance versus pressure plots for normal operation are presented in Fig. 3.12 with bottom-radius R_B and β as parameters. It can be observed that β mainly influences the sensitivity and non-linearity for large deflections whereas R_B affects the zero pressure capacitance. Lowering R_B decreases the transducer's absolute capacitance and also slightly lowers the total capacitance change. Therefore, smaller bottom-electrode radii increase the relative sensitivity and narrow the slightly non-linear region when P approaches unity.

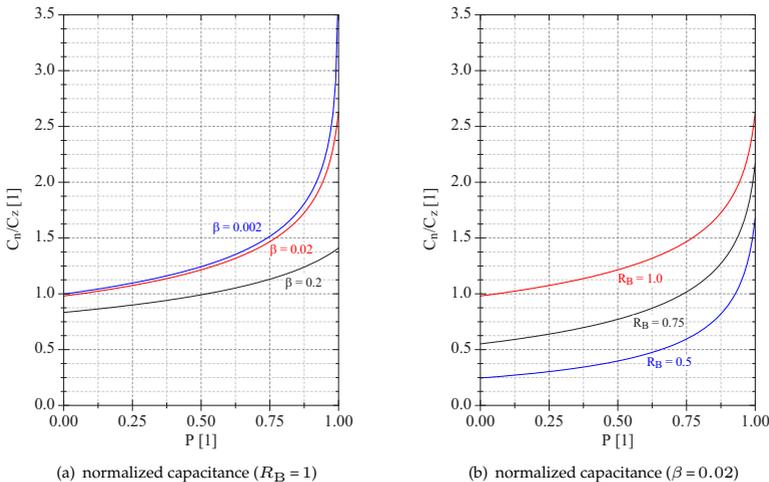


Fig. 3.12: Influence of bottom-electrode radius and dielectric insulation on the capacitance during normal operation. The capacitance was calculated with (3.74) and (3.71).

Touch-mode operation

The transducer plate touches the insulated counter electrode at touch-down pressure, when $P = 1$, and spreads if pressure is further increased. Therefore, the trans-

ducer output becomes the sum of three capacitances:

$$C^{(\text{touch})} = C_{\text{offset}} + C_t + C_{\text{nt}} \quad (3.77)$$

where C_{offset} , C_t , and C_{nt} denote the static offset capacitance, capacitance of the flat plate part in touch with the insulation, and the capacitance of the outer plate part still having a gap between plate and bottom-electrode, respectively.

C_{nt} can be calculated by integrating (3.69) from touch-down radius R_t over the bottom-electrode taking the midplane profile $W^{(\text{touch})}$ given by (3.33)

$$\frac{C_{\text{nt}}}{C_z} = \int_{R_t}^{R_B} \frac{2R}{(1 + \beta) - W^{(\text{touch})}} dR. \quad (3.78)$$

No closed analytic solution can be given for this equation and C_{nt} must be integrated numerically for the individual insulation properties β and touch-down radii R_t . It can be noted that C_{nt} is equal to $C_n^{(\text{max})}$ for the limit of $R_t \rightarrow 0$

$$\lim_{R_t \rightarrow 0} \frac{C_{\text{nt}}}{C_z} = \int_0^{R_B} \frac{2R}{(1 + \beta) - (R^2 - 1)^2} dR = \frac{C_n^{(\text{max})}}{C_z}.$$

Calculation of C_t is easily accomplished for the case of a *dielectric of homogeneous thickness*, i.e. $\beta = \text{const}$. The differential capacitance is given by (3.66) for $w = w_{\text{max}}$ and must be integrated over the touch-area

$$C_t = \int_0^{r_t} \frac{2\pi\epsilon_0 r dr}{w_{\text{max}} \beta}. \quad (3.79)$$

This results with the previously introduced non-dimensional quantities in

$$\frac{C_t}{C_z} = \frac{R_t^2}{\beta}. \quad (3.80)$$

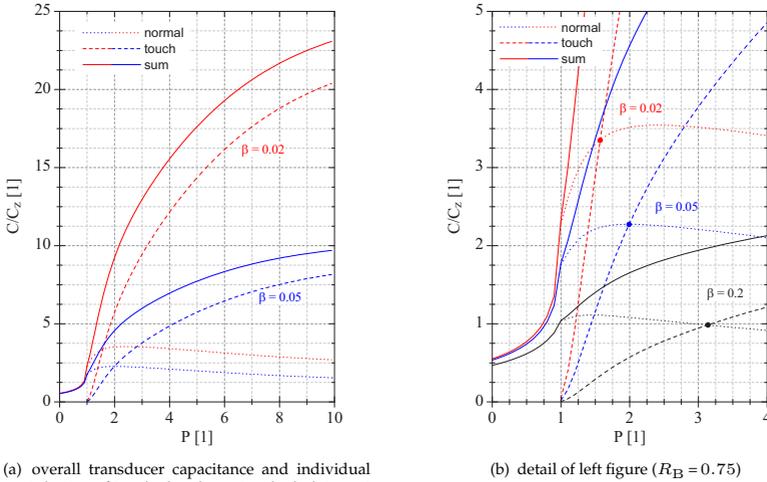
Actual values for C_t as function of applied pressure can be computed with R_t given by approximation (3.34).

The touch-area capacitance C_t has reached its maximum when the transducer plate is in contact with the whole bottom-electrode, i.e. the touch-radius is equal to the bottom-electrode radius. No gap between plate and bottom-electrode is present anymore and therefore $C_{\text{nt}}^{(\text{min})} = 0$. Thus, the maximum overall pressure dependent transducer capacitance is found to be

capacitance of un-
touched plate section

capacitance of
touched plate section
($\beta = \text{const}$)

maximum capacitance
($\beta = \text{const}$)



(a) overall transducer capacitance and individual contribution of touched and non-touched plate part ($R_B = 0.75$)

(b) detail of left figure ($R_B = 0.75$)

Fig. 3.13: Transducer capacitance in normal- and touch-mode operation. The capacitance of the touch-area C_t dominates beyond $P = 1$. It intersects with C_{nt} at a pressure determined by the insulation properties β . C_{offset} has been omitted.

$$C^{(max)} \approx C_z \frac{R_B^2}{\beta}. \quad (3.81)$$

The magnitude of the capacitances at transition from normal to touch operation, i.e. at $P = 1$, are

$$C_t^{(min)} = 0 \quad (3.82)$$

$$C_{nt}^{(P=1)} = C_n^{(max)} \quad (3.83)$$

Example calculations of C_t/C_z , C_{nt}/C_z , and $(C_t + C_{nt})/C_z$ are presented in Fig. 3.13. It can be noted that C_t dominates the overall capacitance in touch-mode operation. C_{nt} still increases after touch-down. It has a maximum which depends in magnitude and location on β . In addition, C_t depends on β , too, but is affected in a much stronger way. That is, the lower β gets the lower gets the pressure at which the curve C_t intersects the graph for C_{nt} (see Fig. 3.13(b)). In practice, the influence of C_{nt} may therefore be neglected because of the dominant C_t , and the capacitance of the gap can be assumed to be constant with the magnitude at plate touch-down $C_n^{(max)}$

$$C^{(touch)} \approx C_{offset} + C_t + C_n^{(max)}. \quad (3.84)$$

impact of un-touched plate section and transducer sensitivity

approximation of un-touched plate capacitance

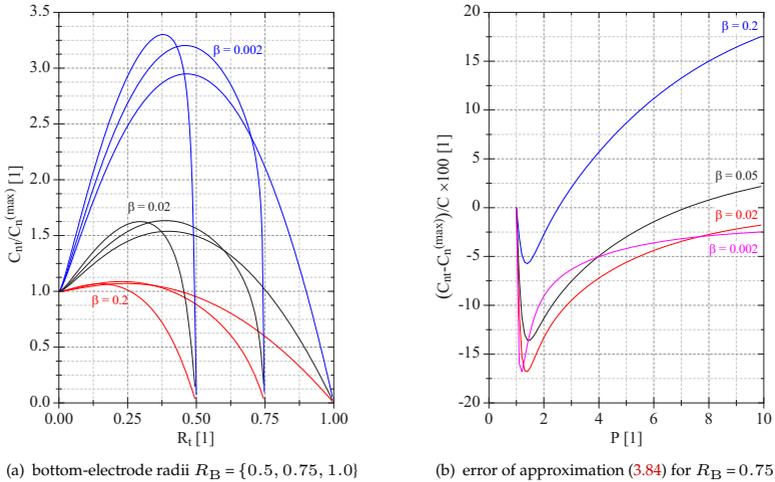


Fig. 3.14: Capacitance and influence of the not touched plate section C_{nt} during touch-mode operation. The magnitude of C_{nt} is a function of R_B and β . The impact of C_{nt} is demonstrated by the error if it is taken to be constant with magnitude $C_n^{(max)}$.

This allows an analytic approximation of the overall touch-down capacitance whereas an included C_{nt} would require numerical computations. The quality of this approximation depends on the sensor design. Results for $C_{nt}/C_n^{(max)}$ versus touch-radius R_t are given in Fig. 3.14(a) illustrating that the maximum magnitude of C_{nt} is inversely proportional to β and that the location of the maxima shifts towards higher pressures for larger bottom-electrodes. This means, a bottom-radius as small as possible should be chosen to improve approximation (3.84). In addition, a thin dielectric with a high permeability should be selected for a high sensitivity and a low impact of C_{nt} beyond touch-down. The resulting error of (3.84) for a bottom-electrode radius of $R_B = 0.75$ is displayed in Fig. 3.14(b). It shows that the assumption of a constant C_{nt} must be considered carefully but improves for high pressures and small values of β .

inhomogeneous dielectric insulation

A further concern during practical sensor fabrication is the dielectric removal during the sacrificial etch. It causes a *concentrically decreasing insulation layer thickness* of the bottom-electrode. The magnitude of removal is dependent on the selected dielectric and sacrificial layer material. It generally causes the sensor's sensitivity to increase with increasing pressure during touch-mode operation. Therefore, the saturation of the capacitive output is extenuated. It can be supposed that there is a β_0 of the dielectric in the center of the bottom-electrode and a $\beta_{r_{max}}$ at radial position r_{max} (both values of β can be calculated with (3.65)). This yields β as function of

radius

$$\beta = \beta_0 \left[1 + \left(\frac{\beta_{r_{\max}}}{\beta_0} - 1 \right) R_t \right]. \quad (3.85)$$

Starting from (3.79) leads to the integral

$$\frac{C_t}{C_z} = \frac{2}{\beta_0} \int_0^{R_t} \frac{\tilde{R}_t d\tilde{R}_t}{1 + \left(\frac{\beta_{r_{\max}}}{\beta_0} - 1 \right) \tilde{R}_t} \quad (3.86)$$

which can be integrated with the primitive [Bro00]

$$\int \frac{x dx}{ax + b} = \frac{x}{a} - \frac{b}{a^2} \ln(ax + b) \quad (3.87)$$

giving the capacitance of the touched plate section for an insulation with concentrically varying thickness

$$\frac{C_t}{C_z} = \frac{2}{\beta_{r_{\max}} - \beta_0} \left[R_t - \frac{\ln \left[1 + \left(\frac{\beta_{r_{\max}}}{\beta_0} - 1 \right) R_t \right]}{\frac{\beta_{r_{\max}}}{\beta_0} - 1} \right]. \quad (3.88)$$

capacitance of touched plate section
($\beta \neq \text{const}$)

Therefore, the maximum capacitance of the transducer increases dependent on the selectivity of the sacrificial etch and equates to

$$\frac{C_t^{(\max)}}{C_z} = \frac{2}{\beta_{r_{\max}} - \beta_0} \left[R_B - \frac{\ln \left[1 + \left(\frac{\beta_{r_{\max}}}{\beta_0} - 1 \right) R_B \right]}{\frac{\beta_{r_{\max}}}{\beta_0} - 1} \right]. \quad (3.89)$$

maximum capacitance
($\beta \neq \text{const}$)

3.1.8 Normal- versus touch-mode operation

So far, the transducer output in normal and touch operation was described neutrally from a mathematical point of view. An assessment of the individual advantages or possible concerns are given in this section. Before hands, the results of Section 3.1.1 to Section 3.1.7 are summarized in chart 3.15 which highlights the marked operation points of both types of capacitive pressure sensors:

summary marked transducer properties

- **Minimum capacitance** $C_n^{(\min)}$ is defined by (3.75) and depends on the bottom-electrode radius R_B and the implemented insulation β .
- **Touch-down capacitance** $C_n^{(\max)}$ can be calculated with (3.76). It is a function of the chosen counter-electrode radius and its insulation. The transducer geometry does not enter explicitly the solution because the normalized deflection profile at plate touch-down is identical for all circular transducers. The

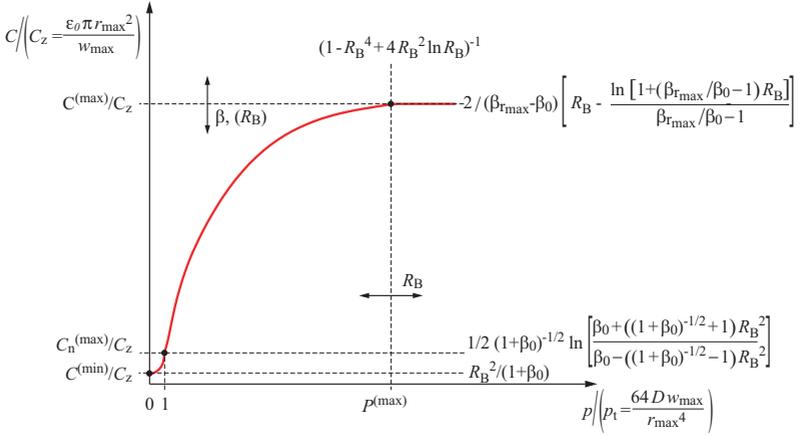


Fig. 3.15: General capacitance versus pressure plot for circular plate pressure sensors. Offset capacitance C_{offset} is not included and must be added to the given capacitance values.

individual transducer geometry affects only the capacitance scale C_z of the y-axis.

- **Maximum capacitance** $C^{(max)}$ is reached when the whole bottom-electrode is in contact with the transducer plate. Any further deflection beyond this point will not cause an increase of $C^{(max)}$ as given by (3.89). It must be noted that its magnitude is in first place a function of the insulation β . The discussion of this section does not consider an insulation layer thickness variation for the sake of simplicity and generality. Therefore the touch-mode capacitance is calculated with (3.81) and not (3.89).
- **Touch-down pressure** p_t is scale of the x-axis. It depends on the whole transducer geometry and additionally on the stress which may be present in the transducer layer. Therefore, p_t must be calculated with (3.7) and scaled with (3.57).
- **Maximum pressure** $P^{(max)}$ is defined as the highest pressure load which causes a change of the transducer output and is given by (3.37).

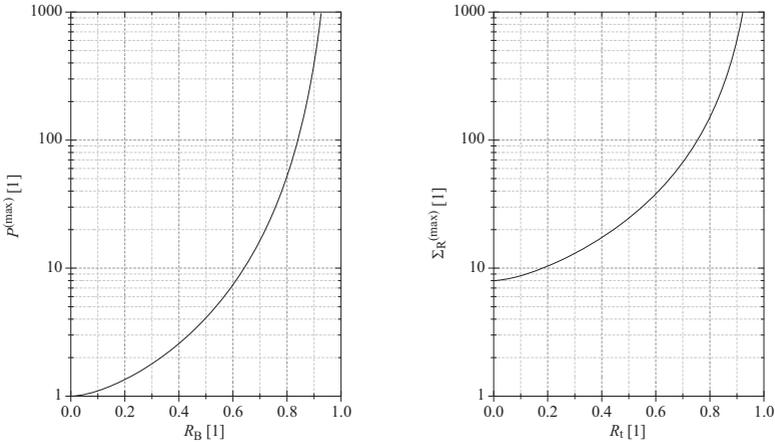
Whether normal- or touch-mode operation will be appropriate for the target application can be decided by going through the following itemization. It is a compilation of features which need to be considered to make a distinction:

- **Pressure range:** A sensor should be designed to either work in normal- or in touch-mode. The touch-down pressure, as the upper operation range limit of normal-mode sensors, can either be increased by making the plate thicker or by decreasing the plate radius. Both measures may cause technological difficulties. On the other hand, Fig. 3.16(a) shows that wide operation ranges could be implemented in touch-mode. Very high loads are required to push

distinct features of normal- and touch-mode

the plate onto the counter-electrode and $P^{(\max)}$ approaches infinity for the limit $R_B \rightarrow 1$. But the capacitance output saturates strongly. Therefore, the actual usable range of the bottom-electrode radius is limited. Already an R_B of 0.75 results in a $P^{(\max)}$ of roughly 28 and a maximum stress $\Sigma^{(\max)}$ of 100 as can be observed in Fig. 3.16(a) and Fig. 3.16(b). The design must ensure that the maximum stress does not exceed the yield-stress of the transducer material.

The difficulty, to achieve wide operation ranges in touch-mode, is related to the insulation thickness. Saturation of the sensor signal occurs and very thin insulation layers must be implemented to stretch out the usable pressure range (see Fig. 3.17(b)). Therefore, touch-mode sensors will be highly susceptible to all process influences concerning the insulation, as e.g. deposition of the dielectric, sacrificial etch, and surface roughness in general (see further below).



(a) maximum pressure (3.37) which causes a capacitance change versus bottom-electrode radius (b) maximum stress within the transducer plate caused by bending moments versus touch-radius

Fig. 3.16: Maximum operation pressure $P^{(\max)}$ of touch-mode sensors defined as the pressure at which the whole bottom-electrode is in touch with the transducer plate. The maximum mechanical stress at the surface of the plate’s edge must not exceed the transducer’s yield-strength. The actual stress magnitude can be calculated from the given non-dimensional radial stress $\Sigma_R^{(\max)}$ and the scales summarized in Tab. 3.1.

- **Sensitivity:** The general characteristics depicted in Fig. 3.15 indicate that normal-mode sensors will have a high sensitivity in their upper pressure range whereas touch-mode sensors will be most sensitive in their lower operation range. Pressure range and sensitivity are related and must be considered simultaneously. In both cases a very high sensitivity can be achieved in a narrow pressure range but also ranges of very low sensitivity exist. A distinction is

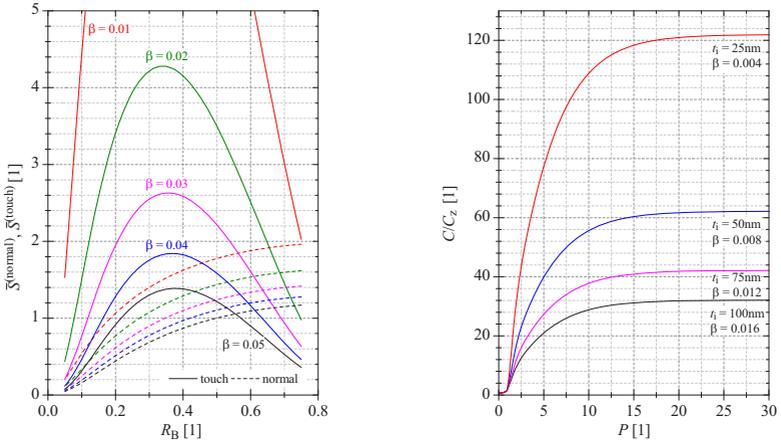
average sensitivity

possible if a wide range is wanted. In such a case, an average sensitivity for the whole allowable operation range can be defined:

$$\bar{S}^{(\text{normal})} = \frac{1}{C_z} \frac{C_n^{(\text{max})} - C_n^{(\text{min})}}{1} \quad (3.90)$$

$$\bar{S}^{(\text{touch})} = \frac{1}{C_z} \frac{C^{(\text{max})} - C_n^{(\text{max})}}{P^{(\text{max})} - 1}. \quad (3.91)$$

The graphs of Fig. 3.17(a) show that a high sensitivity over a wide pressure range can be achieved with touch-mode sensors. However, it can be observed that normal-mode sensors may have a higher average sensitivity for large bottom-electrode radii if thick insulation layers are implemented, i.e. β and R_B are large. The sensitivity and applicable pressure range of touch-mode sensors can be adjusted with the insulation β at a constant R_B as illustrated in Fig. 3.17(b).



(a) average sensitivities of normal- (3.90) and touch-mode (3.91) sensors

(b) sensor output for different insulation thicknesses and a bottom-radius of $R_B = 0.75$

Fig. 3.17: Average sensitivity of normal- and touch-mode pressure sensors. The output characteristic are presented for an exemplary transducer with different nitride insulation thicknesses ($\epsilon_{\text{SiN}} = 7.34$, $w_{\text{max}} = 840$ nm).

- **Linearity:** Both sensors perform best in their lower pressure range with respect to linearity. Normal-mode sensors become highly non-linear in vicinity of the touch-point. This behavior becomes more pronounced the thinner the insulation is designed as can be observed in Fig. 3.12(a). On the other hand, the linear range of touch-mode sensors can be increased by thinning down the insulation (see Fig. 3.17(b)). Therefore, R_B can be kept fixed, i.e. $P^{(\text{max})} = \text{const}$,

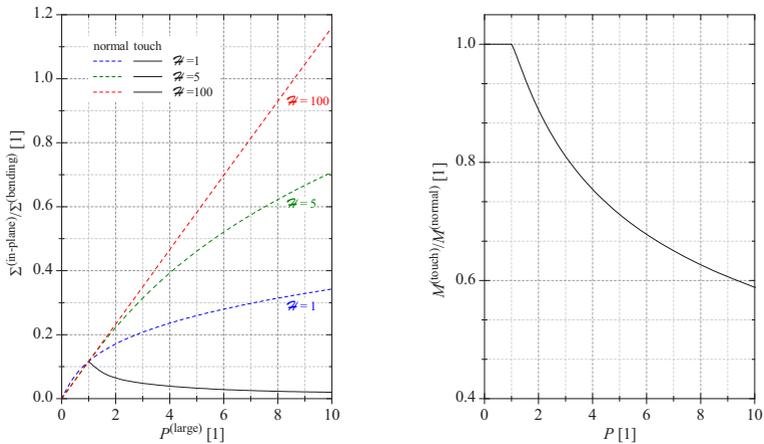
and solely $C^{(\max)}$ is shifted along the y-axis of Fig. 3.15 by decreasing the insulator thickness. In this way, linearity and average sensitivity is increased at the same time.

- Over pressure and pull-in:** The maximum over pressure is not a criteria for the operation mode selection in first place but might be if no insulation is implemented. In such a case plate touch-down may not be allowed and therefore the maximum pressure would have a much lower limit as set by the mechanical robustness of the plate.

An electrostatic pull-in might also confine the maximum allowable pressure if no insulation is present. An insulation expands the allowable deflection range during normal operation. That is because the insulation creates a capacitance in series to the capacitance of the gap and decreases therefore the actual electrostatic force on the diaphragm as discussed in [See97].³

A high resistance to over-pressure is a general feature for all diaphragm type

electrostatic pull-in



(a) ratio of in-plane and bending stress for normal- and touch-mode sensors (b) bending moment ratio for normal- and touch-mode sensors

Fig. 3.18: In-plane stress and bending moment ratio for normal- and touch-mode sensors. Plates need to sustain much lower mechanical stresses for a given load if operated in touch-mode.

transducers having a mechanically confined deflection range. If plate touch-down is allowed, normal- and touch-mode sensors will perform equally good. As soon as their plate touches the counter surface, the in-plane stress does not increase any further. The increasing pressure load after touch-down is balanced by increasing bending moments. The bending stress caused by these

³ No electrostatic instabilities were observed during this work indicating that the simplified parallel plate model, which is commonly applied to predict the pull-in voltage, must be expanded to be appropriate for a deflected plate transducer.

moments is much smaller if compared to the resulting moments in a plate of the same geometry which can deflect freely. This is because most of the applied force in touch-down is directly transferred to the counter surface and needs not to be sustained by the diaphragm. Fig. 3.18(a) illustrates this by comparing the large deflection in-plane stress of an unconfined plate to the maximum stress caused by bending moments of a confined plate. It can be observed that the given stress ratios generally, i.e. for all \mathcal{H} , decreases constantly after plate touch-down.⁴

In addition to the in-plane stress ratio, the bending moment ratio decrease as soon as the plate is in contact with the counter electrode surface. This is shown in Fig. 3.18(b). The same explanation as for the in-plane stress holds: the actual force, which needs to be balanced by the plate, decreases by the part of load exerted onto the touched area.

- **Stress and topography:** Stress within the transducer layer generally affects the pressure range and sensitivity of normal-mode sensors strongly as illustrated in Fig. 3.19(a). Equation (2.24) indicates that stress of a surface micro-machined transducer layer generally composes of an intrinsic σ_i , a thermal σ_t , and an external component σ_e . Intrinsic and thermal component account for the stress from the deposition process. The intrinsic component causes a static shift of the sensor characteristics and σ_t is temperature dependent with a magnitude proportional to the difference of the thermal expansion coefficients of substrate and transducer layer. It changes with the operation temperature of the sensor and causes a shift of the zero scale output and of the sensor's sensitivity. The external component σ_e sums up all additional strain which might be present. Such an additional strain can be caused by all deposits in vicinity to the transducer layer and deformation of the sensor bulk as result of the packaging procedure. Therefore, the sensor's characteristics during normal operation depend strongly on the fabrication conditions and on packaging stress. High temperature coefficients need to be expected in normal operation caused by σ_t and the thermal variation of σ_e .

The sensor characteristic beyond p_t is dominated by bending moments, as can be observed in Fig. 3.18(a). This explains the low influence in-plane stress on the sensors's sensitivity in touch-mode. This can be noted by comparing the change of capacitance and sensitivity in normal-mode and touch-mode illustrated in Fig. 3.19(a). Stress deviations of any kind mainly influence the zero range output of a touch-mode sensor. Sensitivity changes only slightly. Therefore, touch-mode sensors are generally more tolerant to process variations and packaging stress.

- **Surface roughness and hysteresis:** The sensor characteristics during touch-mode operation are dominated by the insulation layer. A high sensitivity, a wide operation range and a good linearity can be achieved with thin dielectrics having a high permeability. Thickness deviations and surface roughness, which influences the overall dielectric properties β , have a large impact

⁴ The different graphs for normal operation result from the scaling procedure which introduces \mathcal{H} . It must be noted that the unscaled deflection of the plate corresponding to the graph $\mathcal{H} = 1$ is actually a hundred times the deflection of the plate with an \mathcal{H} of 100.

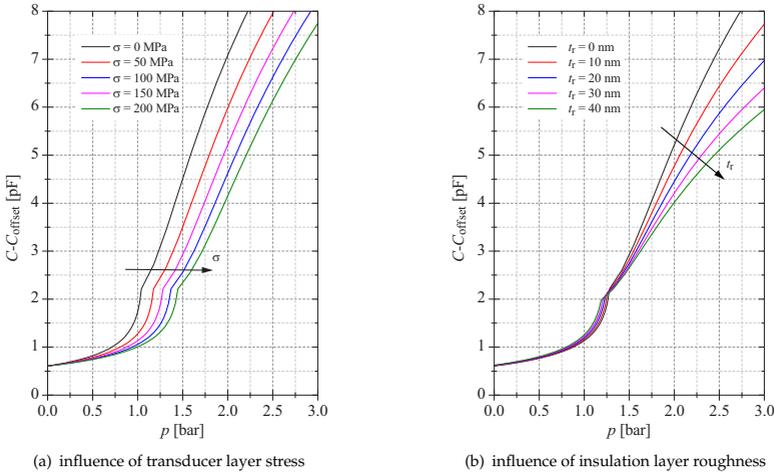


Fig. 3.19: Example capacitance versus pressure plots illustrating the influence of stress and surface roughness during normal- and touch-mode operation. The curves are calculated with (3.74) and (3.80) for a typical sensor design: a poly-silicon transducer plate with $h = 840$ nm and $r_{\max} = 46$ μm , a gap of $w_{\max} = 980$ nm, a nitride insulation of thickness $t_i = 90$ nm, and a rough surface layer as defined in Fig. 3.11 ($A_r/A_v = 1$).

on the output as illustrated by Fig. 3.19(b).

The capacitance in normal-mode is not greatly influenced by a rough insulation layer. The observable deviation of the presented curves in Fig. 3.19(b) mainly originates from a smaller gap between plate and counter-electrode which is modeled to be $w_{\max} = w_{\text{gap}} - t_r$.

An additional issue for touch-mode sensors is the occurrence of a hysteresis. It is supposed to be related to *Van-der-Waals* forces between transducer plate and insulation layer surface.⁵ The magnitude of this hysteresis is observed to dependent on the surface roughness and the contact material. That is, unintentionally deposited LPCVD oxide sealant material e.g. causes an increasing hysteresis if the applied pressure is cycled in touch-mode operation (see e.g. Fig. 3.75 and Fig. 3.76). It is speculated that exposed parts of an uneven counter-electrode surface are under high mechanical stress when in contact with the transducer plate. The high stress causes plastic strain of these bumps if their yield-stress is exceeded. Therefore, the surface roughness decreases in such a case increasing the contact area, increasing the magnitude of contact force, and increasing the hysteresis. At the same time the sensitivity and capacitance increases because of the decreasing t_r and increasing $\epsilon_{r,\text{eff}}$.

- **Robustness:** Degradation of the sensor can be caused by either mechanical,

⁵ An analytical and numerical model of the adhesive surface forces is presented in [Kna02] including measurement data for adhesion energy of a poly-silicon/poly-silicon contact.

electrical, or thermal loads. As discussed above, overpressure is usually not an issue for capacitive pressure sensors but pressure cycling can cause a mechanical wear of the insulation layer resulting in a drift of the touch-mode transducer.

Dielectric charging may be a concern for all capacitive transducers. Charges can be transported into the insulation layers if high voltage loads are applied. Therefore all capacitive sensors are threatened by electrostatic discharge ESD if no additional protection circuitry is present. This holds equally for normal- and touch-mode sensors. However, a higher magnitude of dielectric charging must be expected for touch-mode sensors because a very thin counter electrode insulation is advantageous with respect to sensitivity, linearity, and applicable pressure range. The insulation at the plate support can cause a sensor drift in either operation mode and must be designed with a proper thickness. Contact charging as described in [Cab00] and spark discharge [Wib98] is a more pronounced problem for normal-mode sensors. Especially designs with omitted bottom-electrode insulation and unintentionally deposited sealant may store charges after an accidental touch-down or after a spark discharge.

Thermal loads are a more serious problem for touch-mode sensors if the sensor is biased during heating. Charge transport in the insulation layer generally increases with temperature and the danger of a sensor drift due to dielectric charging must be considered.

3.2 Sensor concept

This section focuses on the sensor concept and discusses special design features such as the array arrangement of individual sensor cells, contact pad geometry and location, reference cells, and through substrate vias. It illustrates the consequences of individual approaches for the overall system design and packaging concept.

3.2.1 General design and design variations

The fabricated pressure sensor designs of this work feature a transducer array of 16 individual sensitive plates surface-micromachined on fused silica (see Fig. 3.20). Each transducer has a counter electrode which is fixed rigidly on the substrate's surface. Counter electrode and plate form a pressure sensitive capacitor (see also Fig. 1.9 and Fig. 2.1). All individual transducers of the array are switched in parallel in order to raise the sensor's output level and swing.

A number of different designs have been evaluated. These comprise variations of the individual plate's diameter (70 μm , 90 μm , 120 μm), alteration of the plate shape (round, hexagonal), and modification of the bond pad configuration (3 pads single side arrangement: Fig. 3.20(c), 2 pads opposing arrangement: Fig. 3.20(d)). The process description of the preceding sections focuses on the final design (*Design-2*) as depicted in Fig. 3.20(b). Other layouts showed up to be superfluous or to be inferior. Hexagonal plates with their pointed features increase the risk of fracture and were not implemented in *Design-2*. Similarly, the 70 μm and 120 μm plate diameter layouts were omitted (see Fig. 3.20(e)). These sensor versions were simply scaled copies of the original 90 μm -sensor cell and did not prove to be necessary. The 90 μm -sensors offered enough flexibility for tuning of the target pressure ranges. That is, sacrificial layer and transducer layer thicknesses could be adjusted in a range that allowed for sensing of ambient pressure (0.5 bar – 1.3 bar) in normal operation and for sampling within an industrial pressure range (1 bar – 8 bar) in touch-mode.

The sensitive top of the transducer array is made out of a single piece of poly-silicon. It is interconnected to a top-electrode bond pad. The individual bottom-electrodes are fixed rigidly on the substrate each interconnected to the U-shaped poly-silicon bond pad surrounding the whole transducer array (see Fig. 3.20(c) and Fig. 3.20(d)). Such a design keeps all poly-silicon bottom-electrode lines, i.e. all connections to and within the counter-electrode array, as short as possible. This measure lowers the series resistance of the sensor, raises the quality factor, and results in a compact sensor geometry. However, some difficulties arise by combining the individual plates into a mechanical continuous network. Transducers located at the array border are not clamped symmetrically. They are only attached to the rather flexible silica bulk on their outward oriented side which allows a stress relieve in these plates making them somewhat more sensitive. Outer and inner cells are mechanically not identical and have therefore differing touch-down pressures. Furthermore, the narrow gap between the array and the bottom contact (see Fig. 3.21(c)) can lead to adverse influence of humidity and other environmental contaminations on the sensor's performance. Most capacitive readouts are highly susceptible to changes in ohmic conduction taking place in parallel to the sensor. Such a parasitic

design variations

array geometry

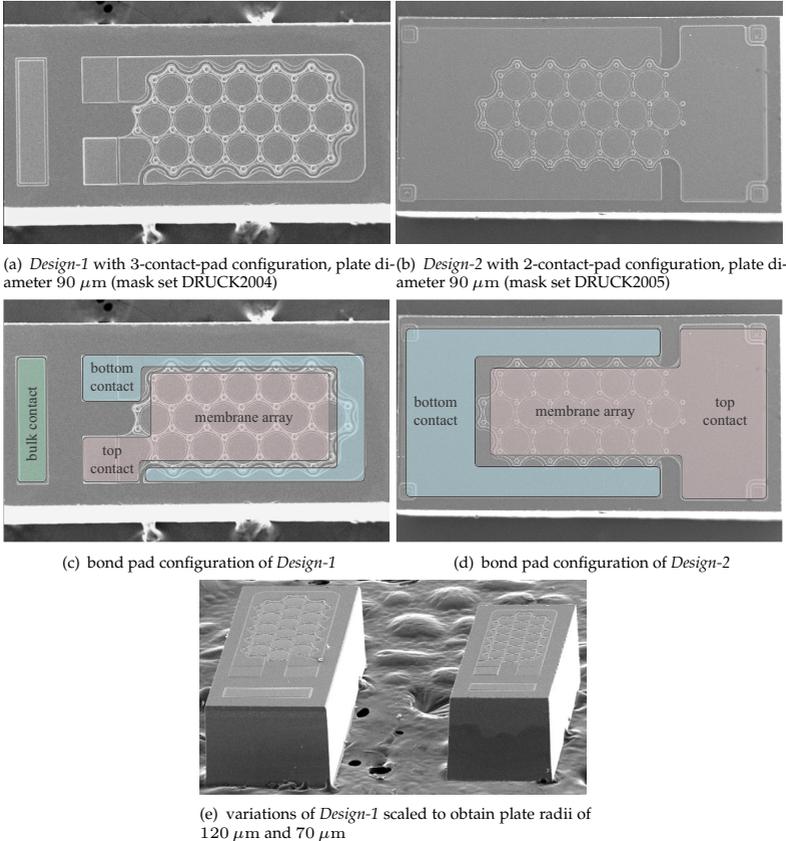


Fig. 3.20: SEM pictures of the fabricated pressure sensor designs.

current could be caused e.g. by humidity dependent surface conduction from the array border to the bottom-contact.

The general design features of the sensor are illustrated in Fig. 3.21. Each of the 16 fixed counter-electrodes are interconnected via six leads to its surrounding partners. Feedthroughs located at the array edge are in contact to the sensor's metallization. The whole bottom-electrode and all feedthroughs are covered by an insulation layer to prevent any electrical contact to the top-electrode at the array's mechanical support. The sensor cavities are defined by two stacked layers: a circular sacrificial layer which is covered by an additional etch-channel layer. Both layers are removed during a sacrificial etch through six etch channels with inlets which are

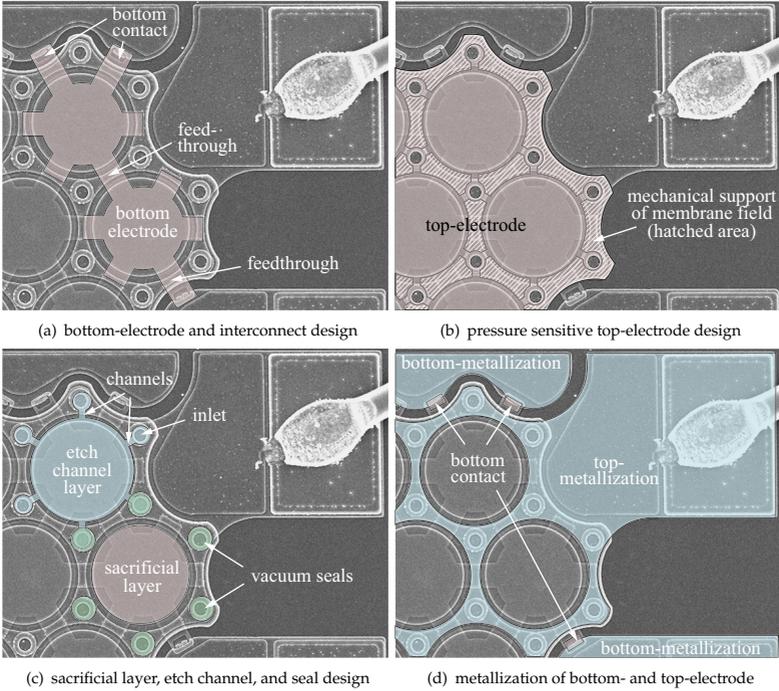


Fig. 3.21: Overview of general sensor design features (SEM pictures of *Design-1* sensors).

closed by seals during a subsequent vacuum process step. A single metallization layer is patterned to form the contact pads and the interconnection to the bottom- and top-electrode. The array is partly covered by the metallization running around the individual plates above their rigid mechanical support area.

3.2.2 Reference sensor cells

Some capacitive readouts require a second reference capacitor. The reference is intended to eliminate the impact of process deviations, to lower the influence of long-term sensor drifts, and to minimize the temperature dependence of the sensor. Therefore, the perfect reference cell is in layout and fabrication identical to the sensor cell but is reinforced with a stress-less type of the sensor's plate material at reference pressure.

Different reference implementations have been proposed in literature:

- **Cells with solid dielectric:** Additional cells are placed on the die which have

a solid dielectric. This dielectric could be the sacrificial layer simply remaining in these reference cavities (see Fig. 3.22(a), [Guo00]). Such cells must be smaller in size due to the higher permittivity of the solid dielectric in comparison to the permittivity of space in case of the sensor cells. For this reason, their layout must deviate from the sensor cell design and it is likely that process variations will also cause differing capacitance values. Additionally, the temperature dependency of the reference with solid dielectric differs from that of the sensor which is affected by mechanical stress. Finally, CVD oxides are frequently used as sacrificial layer. They require an additional treatment to improve their dielectric bulk and surface properties in order to form a stable reference capacitor.

- Reference electrode within the sensor cavity:** A second, fixed counter-electrode within the pressure sensor chamber can be used as means to provide a reference capacitance (see Fig. 3.22(b), [Cha98]). This extra electrode must be placed close to the plate support where the deflection is minimal. This concept compensates process deviations well because sensor and reference are processed identically and the reference is integrated within the sensor cell with the benefit of a small die size.
- Stiffened reference transducers (vacuum process):** Mechanically reinforced plates can form reference capacitors because of their greatly reduced pressure sensitivity (see Fig. 3.22(c), [Egg00a] [Dud94] [Kas02]). A common approach is to open LPCVD or PECVD passivation material only over the pressure sensitive transducers and to keep the reference cells covered. In this case, sensor and reference have the same dielectric and the reference geometry need not to be changed. However, the resulting reference is ideally equal the sensor's capacitance at zero pressure because the reinforcement took place in a vacuum

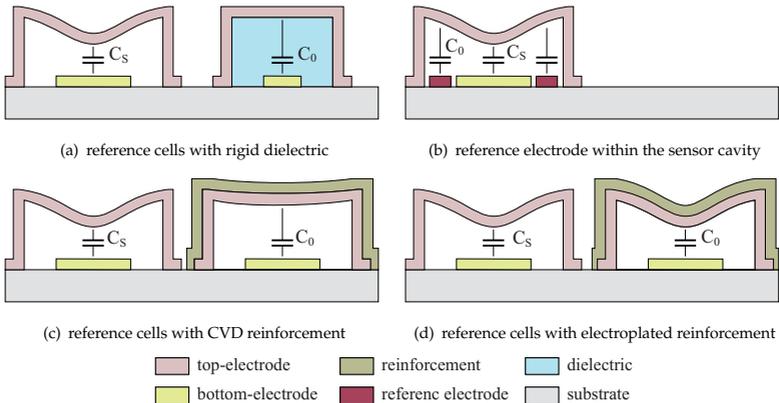


Fig. 3.22: Reference concepts for capacitive pressure sensors.

process. In operation, the actual sensor capacitance might therefore be quite different. This is especially the case if the sensor is run in touch-mode. Usually, all types of LPCVD or PECVD passivation layers are under mechanical stress. This stress can be tuned to some extent but the required thick reinforcement deposition will cause a flexure of the plate in case of *surface-micromachined* transducers. Furthermore, actual transducer layer and reinforcement form a stack which composes of materials with different TECs. Therefore, shifts in the reference capacitance in consequence of temperature changes must be considered. Moreover, LPCVD and PECVD oxide layers are prone to humidity uptake causing strain within the layer which can lead to undesired deflection changes of the stiffened reference cells.

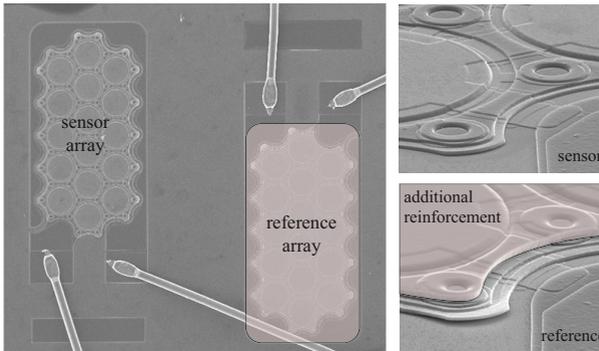


Fig. 3.23: Implemented concept of a barometric sensor reference. SEM picture of a sensor die with sensor and reference array. The reference array is stiffened by $3\ \mu\text{m}$ of electroplated nickel which covers the whole array (see right pictures for a comparison of a sensor cell and a reinforced reference cell).

- Stiffened reference transducers (atmospheric process):** In this work, a reinforcement is deposited on every second die by means of electroplating at atmospheric pressure (see Fig. 3.22(d)). The suggested approach is chosen because it guaranties identical fabrication processes for sensor and reference and it enables a fixture of the plates at high pressure. This is especially important if the sensor is run in touch-mode. In this case, its capacitance is much higher than at zero deflection in vacuum. A reference to vacuum would yield a much lower capacitance than the actual sensor value. Furthermore, the touch-down pressure is sensitive to process deviations. Such offset shifts would not be reflected in a vacuum reference. However, the electroplated metal has a different TEC which may lead to an extra temperature dependency of the reference cell.

A SEM picture of a fabricated sensor with a second reference array on the same fused silica die is given in Fig. 3.23. Sensor and reference array are fabricated identically including the metallization. Finally, a $3\ \mu\text{m}$ electroplated nickel reinforcement

is deposited as last process step at ambient pressure. This extra layer covers the reference array completely.

3.2.3 Sensor packaging and interconnection

It is one of the advantages of fused silica that a capacitive sensor can be designed as a two terminal floating capacitor. This is simplifying the electric contact to it, i.e. no extra bulk contact is required to pull the substrate to a fixed potential. Furthermore, two or more transducers on a single die, like e.g. a reference array, are electrically insulated from each other and can be sampled independently. However, it was not certain if a fabrication procedure on fused silica could be implemented in the beginning of this work and processes were run on silicon and silica in parallel. For this reason, *Design-1* featured a third bulk contact pad (see Fig. 3.20(c)) which was omitted in *Design-2* (see Fig. 3.20(d)).

Mechanical fixture and electrical interconnection concept depend on each other and information about the required packaging procedure of the sensor needs to be available prior to sensor design. Different interconnection and chip-mount options are summarized in Fig. 3.24 each having their individual benefits and drawbacks:

- **Flip-chip-mount, opposing pads:** Large pads at the maximum distance can be fabricated to prevent short-circuits caused by spreading of conductive glue. However, spreading of glue is still an issue because conductive particles must not get between pad and transducer array. Packaging stress is applied to the sensor die at the stress sensitive upper surface which supports the sensitive array. Moreover, the package induced stress is exerted from both sides of the transducer field. For this reason, a maximum impact of the thermal mismatch of package and sensor substrate must be expected for this package concept. In addition, the application of a protective coating without air inclusions may be difficult.
- **Flip-chip-mount, single sided pads:** Separation of the bond pads is, in comparison to the preceding approach, more difficult if the die size can not be increased and stud bumps may be required. On the other hand, a mechanical stress insulation can be achieved by a single sided die-attach at some distance to the array and must be considered as an advantage of this concept. The system can be coated by immersion.
- **Back side die-attach, opposing pads:** The back side die-attach puts the sensor bulk between package substrate and sensor surface. This approach results in a very robust die fixture. The bulk acts as stress barrier for any package strain. The opposing pads can be used to keep wire bonds short and they can be, like the electrical lines on the substrate, separated as much as possible. This approach is straightforward and reliable because standard adhesives and wire-bonding can be utilized, but the overall package height is increased by the wire bond loops and their coating.
- **Back side die-attach, single sided pads:** This concept leads to the best package stress insulation (an approach which is followed e.g. by [Nes04]). However, the die size may need to be increased for the somewhat more challenging die-attach.

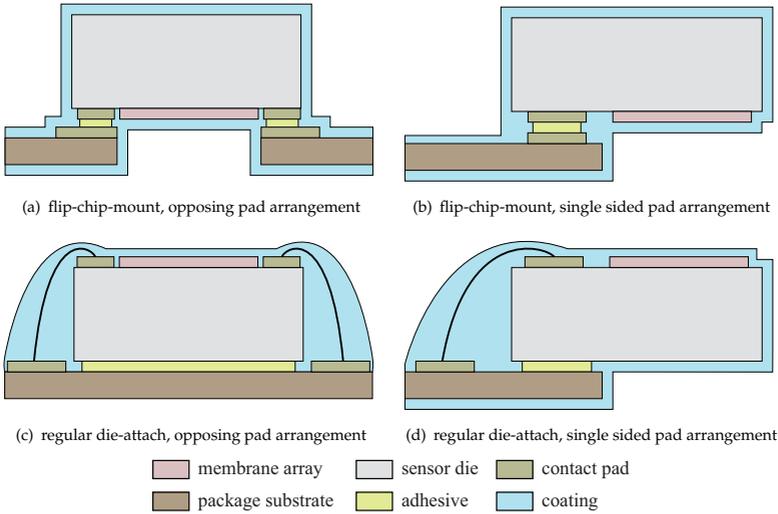


Fig. 3.24: Comparison of sensor packaging concepts.

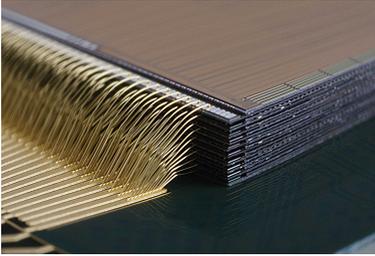
Conductive adhesive chip-mount

Although aimed for in the beginning, single sided flip-chip-mounts with conductive adhesive did not prove to be a simple matter. Difficulties were related to the small dimensions, i.e. small gaps between the contact pads and the transducer array. In addition, reliable contacts to the aluminum metallization can not be made and other, more complex, metallizations stacks must be developed. Cause for this is the native oxide which forms readily on every exposed aluminum surface. The same oxide also degrades the contact under environmental stress during the sensor's lifetime. Many efforts have been spent to implement a reliable conductive adhesive connection to Al surfaces but have failed [Sch06]. It is commonly agreed that inert contact metals such as Au or materials which form conducting or semiconducting oxides like Cu and Ni must be used as pad metallization for conductive adhesive mounts.

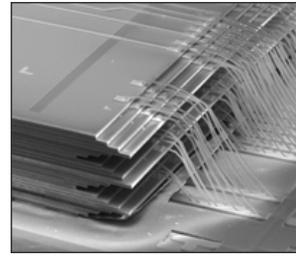
The implementation of a mechanically reliable low-stress die-attach is already challenging. If the adhesive bond must fulfill mechanical *and* electrical functionalities, i.e. mechanical fixture and electrical interconnection, hardly a perfect solution can be found. From an industrial point of view, standard packaging procedures are adhered to as long as possible. Flip chip mounts with conductive adhesive are only implemented if strong requirements demand its implementation. Very sophisticated high volume solutions for cheap and thin electronic devices exist with back-side die-attaches and wire bonds. The flash memory chips depicted in Fig. 3.25 can be taken as examples of how far these "standard technologies" can be driven. It can be in-

conductive adhesive chip-mount

potential of standard packaging approaches



(a) *ELPIDA Memory*, 20 chip layers, 1.4 mm overall package thickness [ELP07]



(b) *Hynix Semiconductor*, 16 GB NAND flash, 24 chip layers, 1.4 mm overall package thickness [Hyn07]

Fig. 3.25: Examples of stacked multi-chip flash memory modules illustrating how far and cost-effective high volume packaging with the standard concept of a back-side die-attach and wire bonding can be driven.

ferred that cost and miniaturization requirements for a miniaturized pressure sensor system can be met even with a back side die-attach and wire bonds.

downsizing the
package height

On first glance, the flip-chip mount with conductive adhesive leads to a lowered overall package height. On the other hand, it can be supposed that the additional height of wire bond loops and their coating could be balanced by a thinner die. In general, thinning the die is not desirable because it makes the die more fragile and susceptible to mechanical stress. That is, a thinner die is more affected by the package stress exerted from the back-side die-attach zone. Still, this mechanical setup is beneficial because it puts the bulk as a stress buffer between stressed back side and the transducers on the die's surface. This is not the case for the conductive flip-chip mount where the stress is directly introduced to the sensitive side of the die.

qualification
requirements

Considerable development time is necessary to implement a reliable metallization and low-stress conductive adhesive bond. This is especially the case if the work aims at a commercially successful products. In this case, the sensor and its package must be in accordance to today's industrial quality standards. The *Joint Electron Devices Engineering Councils (JEDEC, [JED08])* is a resource for internationally accepted semiconductor standards. Table 3.3 presents a summary of the most common stress tests as given by the *JEDEC*. The presented compilation of the device qualification procedures shows how severe the environmental stress testing is, even for the most general products (some additional standards and related *JEDEC* publications are summarized in Tab. C.1). These standards define the key requirements which must be present in mind during the transducer and package development process.

Table 3.3: Summary of JEDEC standards for stress test driven device and package qualification with examples of typical applicable conditions for consumer electronics (DUT: device under test).

standard	title/description
EIA/JEDEC JESD22-A101B	<i>Steady State Temperature Humidity Bias Life Test</i> typical 1000 h at 85 °C/85 %RH, no bias voltage
JEDEC JESD22-A102C	<i>Accelerated Moisture Resistance - Unbiased Autoclave</i> condition C: 96 h at 120 °C, 100 %RH, 2.1 bar
JEDEC JESD22-A103C	<i>High Temperature Storage Life</i> condition A: 1000 h at 125 °C
JEDEC JESD22-B103-B	<i>Vibration, variable Frequency</i> condition A (shipping): 30 min per axis, 6.27 G RMS acceleration
JEDEC JESD22-A104C	<i>Temperature Cycling</i> condition G/2 (whiskers): typ. 100 cycles at -40 °C/125 °C, 2 cph
JEDEC JESD22-A106B	<i>Thermal Shock</i> condition D: typ. 15 cycles, 150 °C/-65 °C, transfer time < 20 sec
IPC/JEDEC JESD22-A113E	<i>Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing</i> definition of procedures to simulate shipping, storage, reflow and cleaning of DUTs prior to the normal operation failure testing
JEDEC JESD22-A114D	<i>Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model</i> class 1A (minimum): 250 V, the voltage stress is applied to the DUT by a charged 100 pF capacitor and a 1.5 kΩ series resistor
EIA/JEDEC JESD22-A115A	<i>Electrostatic Discharge (ESD) Sensitivity Testing Machine Model</i> class 100 V (minimum): the voltage stress is applied to the DUT by a charged 200 pF capacitor
JEDEC JESD22-A118	<i>Accelerated Moisture Resistance - Unbiased HARST</i> condition A: 96 h at 130 °C, 85 %RH, 2.3 bar
JEDEC JESD22-A119	<i>Low Temperature Storage Life</i> condition A: 168 h at -40 °C
JEDEC J-STD-020C	<i>Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices</i> level 1: soak 168 h at 85 °C/85 %RH, 3× reflow at $T_{peak}=260$ °C
JEDEC JESD72	<i>Test Methods and Acceptance Procedures for the Evaluation of Polymeric Materials</i> included: mechanical integrity, operation life time, bond strength

Through substrate via

A through substrate via can be beneficial. It allows to maintain the advantageous back side die-attach but to use conductive glue for the interconnection. Such an approach enables an overall package thickness reduction, i.e. the package height can

be decreased due to the absence of wire loops while keeping the die thickness unchanged at the same time. Some prove-of-concept studies were completed in course of this work with the intention to overcome the difficulties of via implementation in silica. The proposed concept will be presented briefly in this section.

Many via concepts have been proposed for silicon wafers [Lem03] [Cho02] [Bur04] but most of them use deep reactive ion etching as means to get through the bulk. Etching of silicon oxide is slower and poses some extra demands on the required masking material (see Section 2.4.1). Only since recently there are extra dielectric etchers available like e.g. from *Alcatel Micro Machining Systems* (AMS 200 DE, [Alc08]) which may allow DRIE processes through the whole silica bulk, however, an alternative approach is suggested here.

Via formation may take place early in the transducer process flow. This could render the substrate fragile and could lead to topography which may interfere with subsequent lithography steps. On the other hand, if via formation follows the transducer process, the transducer must be securely protected. Dry etching of the silica bulk is more challenging than the same process on silicon and therefore wet-etching is preferred here having the drawback of large isotropic etch cavities. The proposed approach tries to solve these general issues by a via formation in two steps (see Fig. 3.26):

suggested two
step via concept

1. Front side via

The front side part of the via, which is only a couple of microns deep (for this work $30\ \mu\text{m}$), needs to be fabricated prior to or during the transducer process (see Fig. 3.26(a) and Fig. 3.48(a)). Only small hole diameters are required. These can be sealed by LPCVD films which leave a planar surface and which can withstand all subsequent high temperature processes. The substrate material is kept as rigid as possible until a late state of the process.

2. Back side via

The second part of the via is opened from the back side by means of wet-chemical etching. Isotropic etching leads to large openings depending on the substrate's thickness. Therefore, the required hole diameters can be downsized by substrate grinding prior to the back side via etch. The rigidity of the substrate is increased by grouping the back side holes and reducing the overall number of openings as illustrated in Fig. 3.26(a). The back side etch needs to be stopped when the front side part of the via is exposed. Finally, electroplated metal is deposited from the back side to form the contact pad and to interconnect to the front side via part.

Processing of the proposed via concept could not be completed within the timeframe of this work. For the same reason, the related packaging concept as depicted in Fig. 3.26(c) could not be implemented. A description of the related process development is summarized in Section 3.3.8 and additional details can be found in [Bis05a] and [Bis05].

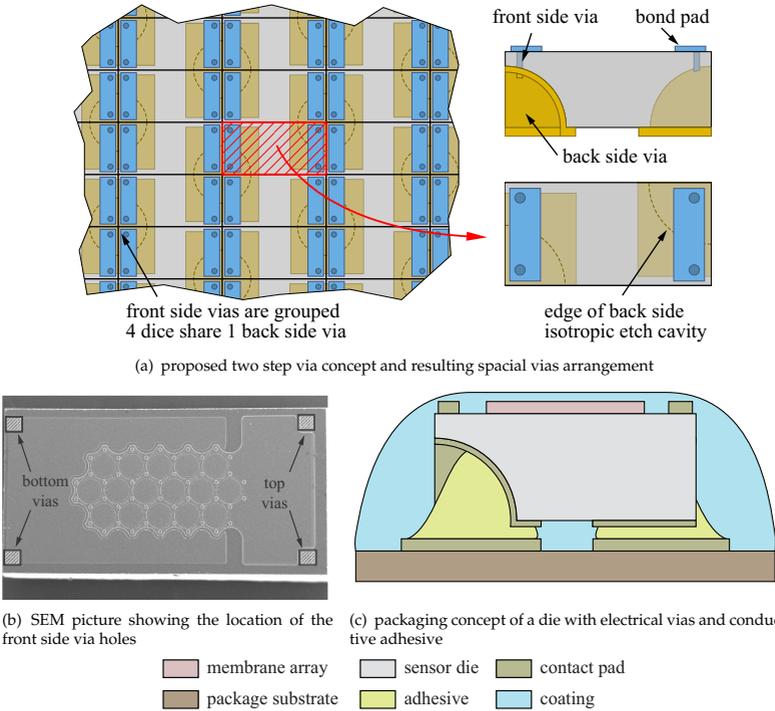


Fig. 3.26: Illustration of a two step through substrate via in fused silica. The back side contact is formed by an isotropic wet etch and an electroplated metallization. Front side vias either wet or dry etched are grouped and share one back side cavity to reduce the number of required cavities.

Implemented packages

The preceding argumentation favors a back side die-attach. The straightforward packaging concept as presented in Fig. 3.24(c) was used in this work for all die testing and proved to be a good choice. A picture of a packaged die is presented in Fig. 3.70(a). Information on package modeling of the presented sensor mounted with a back side die-attach can be found in [Her07].

Some additional testing was done with "reference" sensors which were only mechanically fixed by bond wires to a package substrate. The sensor's characteristics could be measured without any package interference from these samples. Wire bonding was accomplished by temporarily fixing the dies with photoresist into a package cavity. The resist was removed after wire bonding leaving the dies stressless supported by bond wires.

3.3 Sensor design and fabrication

This section on sensor processing adds sensor specific information to the general aspects of micromachining on silica presented in Chapter 2. It contains most of the fabrication details, which are required to fabricate the sensor depicted in Fig. 3.20(b) based on the final mask set DRÜCK2007.

3.3.1 Insulated bottom-electrode

alignment
keys

Alignment keys are dry-etched into the silica bulk prior to any other processing. They must be covered with nitride layers to ensure their protection during the wet-chemical etch sequences. Lithography with high accuracy on silica is difficult as explained in Section 2.3.2 and a concentric misalignment should be expected. An additional mask layer for the lithography marks is inevitable because the bottom-electrode as first structural layer is wet-chemically patterned. Despite the transparent bulk, marks of 200 nm depth are already well visible. Table C.2 summarizes the alignment rules which have to be adhered to during the following sensor process.

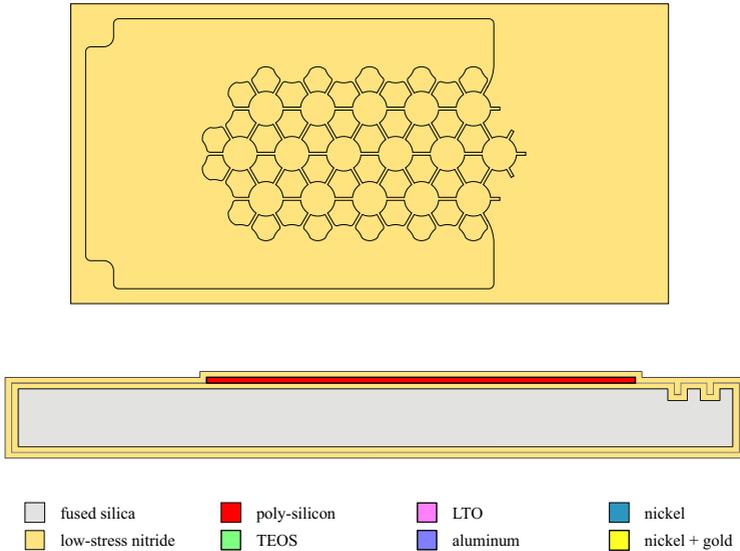


Fig. 3.27: Schematic layout and cross-section of the sensor until insulation nitride deposition.

nitride
protection &
insulation

One of the most serious problems during fabrication of the presented sensor on silica is the protection of the bulk material against hydrofluoric etchants. Silicon nitride was chosen as protection layer but must also serve as dielectric insulation of the bottom-electrode. As discussed in Section 2.3.1 and illustrated in Fig. 2.39, the better

the dielectric properties of nitride are the worse becomes the wet-chemical resistance to HF. For this reason, two nitride layers are deposited which are tuned individually for chemical protection (Nit-D20) and electrical insulation at a moderate stress level (Nit-Z20). A 45 nm thick protection layer is deposited below the bottom-electrode where no electric insulation is required. It could withstand many hours in HF/HCl (roughly 10 h) whereas the 90 nm insulation layer on top of the bottom-electrode would be already removed after about 3 h (see Tab. B.18). Both nitride layers are under high tensile stress (see Fig. 2.9(a) and Fig. 2.10(a)) and their combined thickness is limited. Cracks on the plain surface have been already observed for 250 nm of Nit-Z20 on silica. These cracks can not be noticed after deposition but become visible during the sacrificial etch. Both, nitride thickness and composition index have a strong influence on the sensor's characteristic. The parasitic off-set capacitance and parallel resistance is determined by thickness and index. Furthermore, thickness variations cause also deviations in the transducer array stress. Two stacked depositions should be used as means to improve the homogeneity over the LPCVD reactor load as explained in Section 2.3.1. The usually high inherent deposition rate inhomogeneity of about 7 % of the Nit-Z20 process (see Fig. 2.18) can be reduced by interchanging the wafer positions in the reactor during two subsequent runs to about ± 0.6 %. 1 % thickness deviation of the 90 nm insulation causes approximately a 1 % shift of the sensor's offset capacitance.

The given empiric thicknesses have proven to be sufficient and to prevent cracks along the transducer array boundaries where additional stress is exerted to the nitride. The localized extra stress which is applied to the underlying nitride just before final release of moving structures is best prevented by thick sacrificial layers. Examples of observed nitride cracks are depicted in Fig. 3.28.

The proposed process requires the nitride stack to withstand the sacrificial layer patterning, the sacrificial layer etch, and the etching of the seal layer plus three additional HF-dips before LPCVD of insulation nitride, transducer, and metallization. This is only possible if optimized wet-chemical processes of high selectivity towards the nitride are used. These are discussed in Section 2.3.3 and Appendix B.3.

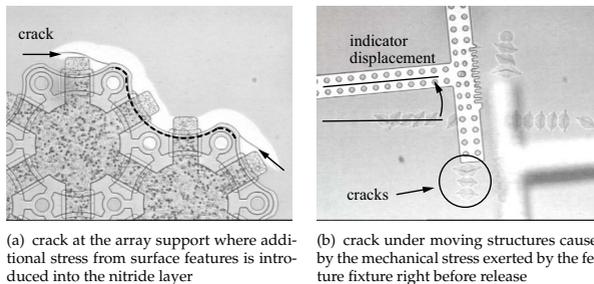


Fig. 3.28: Common examples of wet-chemical substrate protection failures.

The bottom-electrode of the sensor is made of 200 nm PBOR560. This type of layer is suitable because it is fine grained, fully crystalline with a smooth surface, and it

is highly p-doped making good contacts to aluminum. Each cell has six PBOR560 leads creating the offset capacitance of the sensor (see Section 3.4.1). This offset is as reproducible as the undercut of the etch procedure. Therefore, the wider the leads are designed the higher is the sensor offset capacitance but the lower is its susceptibility to process variations. *Design-2* as depicted in Fig. 3.27 has a bottom-electrode track width of $7\ \mu\text{m}$. Etching takes place for 3 min in P-etch (see Section 2.3.3 and Tab. B.16) resulting in an undercut of 330 nm. Already a 10% change of the undercut leads to a sensor offset shift of approximately 1%. From this point of view, the bottom-electrode should be patterned by means of dry etching. However, this is not feasible because of the combined action of the common RIE inhomogeneity and the bad selectivity towards nitride. A RIE process would cause an attack of the underlying protection nitride and a radial thickness inhomogeneity. Any attack of the thin nitride must be prevented for the sake of later bulk protection. A thickness inhomogeneity of the bottom-electrode, due to inhomogeneous dry etch rates, would lead to a change of the sensor topography concentrically distributed over the wafer. 10% thickness deviation of the bottom-electrode causes up to 1% deflection change of the final transducer (see Fig. C.5(d)).

anneal The bottom-electrode layer is asymptotically annealed for 12 h at $800\ \text{°C}$ after patterning. Figure 2.11(b) shows the typical stress of a PBOR560 layer deposited on silicon nitride at such annealing conditions. The applied thermal budget is equal to the highest possible thermal stress of the subsequent process and the anneal guarantees that the bottom-electrode is stable in structure during the subsequent sensor process.

bottom-electrode resistivity Accurate doping and resistivity of the bottom-electrode's is of minor importance. The 25 leads to the counter electrode are switched in parallel each having a resistance of about $2\ \text{k}\Omega$ resulting in an overall series resistance of roughly $80\ \Omega$. This limits the sensors upper cut-off-frequency to about 10 MHz but does not have an effect at the expected operation frequencies below 1 MHz (see also Section 3.4.1).

bottom-electrode contact formation The nitride insulation can be selectively etched with phosphoric acid. It does not attack the underlying poly-silicon and does only marginally etch silicon oxide. Only about 1 nm of as-deposited TEOS masking is removed during the required 100 min etch duration (see Tab. B.17 and Tab. B.18). This makes an extra mask deposition superfluous and either the sacrificial layer oxide or the sealing oxide can be used for masking purpose. It is supposed to do the nitride opening prior to the sacrificial etch, i.e. with the sacrificial layer TEOS as hard mask as depicted in Fig. 3.29. This ensures that any nitride residuals in the contact openings are automatically removed during sacrificial etch.

3.3.2 Sacrificial layer and etch channels

A stack of two TEOS CVD oxide layers form the sensor cavities consisting of a sacrificial layer which is covered by an additional etch channel layer. The sacrificial layer is etched to circular islands in BOE at $20\ \text{°C}$ (see Fig. 3.30). Its thickness can be varied to adjust the required overall gap between counter-electrode and transducer plate. The wet-chemical process time is chosen to produce a $2\ \mu\text{m}$ undercut which is larger than all expected sacrificial layer thicknesses. This measure guarantees constant lat-

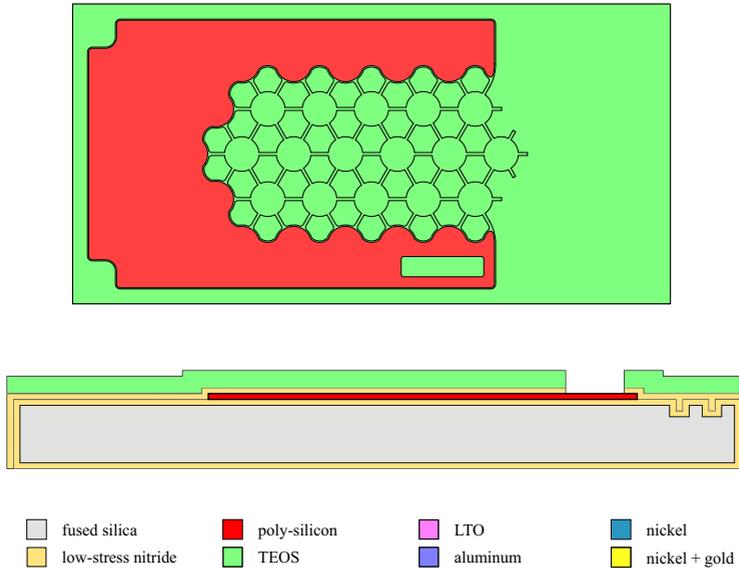


Fig. 3.29: Schematic layout and cross-section of the sensor until insulation nitride patterning. The sacrificial layer CVD oxide is used as hard mask material. As an alternative, the sealing oxide can be used for the same purpose.

eral dimensions of the sacrificial layer islands even if their thickness is altered. A thickness of 675 nm was chosen and no variations were necessary to adjust the sensor's characteristics. The sacrificial layer is deposited in two successive LPCVD runs of approximately the same thickness. In this way, the precise deposition time of the second run can be calculated and the homogeneity can be improved by interchanging the wafer positions in the reactor.

It must be noted, that a sensor's deflection adjustment by means of transducer layer thickness variation is easier than by changing the sacrificial layer thickness instead. This is because larger gaps do not necessarily increase the applicable pressure range as explained in Section 3.1.3 and shown in Fig. C.6(c) and Fig. C.6(d). These figures summarize FEM results of the impact of sacrificial layer thickness deviations. They show that a thicker sacrificial layer increases the deflection by rendering the plate support less rigid. It can be noted, that the effect of thickness variations becomes more severe at high stress levels and high pressure loads (e.g. 10 % thickness variation results in 12 % deflection variation at 1.5 bar and 200 MPa stress).

The sacrificial layer islands are completely covered by a TEOS oxide channel layer which is deposited with a fixed thickness of 350 nm. An additional etch channel layer offers a number of advantages:

impact of thickness variation

benefits of additional etch channel layer

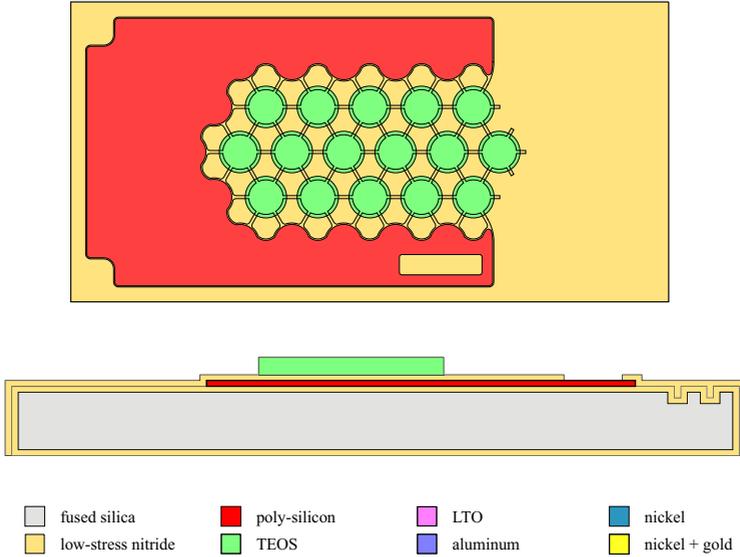


Fig. 3.30: Schematic layout and cross-section of the sensor until sacrificial layer patterning.

- The etch channel geometry becomes independent of the sacrificial layer thickness. Therefore, the channels can be made thinner than the sacrificial layer simplifying their subsequent sealing.
- The sacrificial layer may be annealed and densified if required. This lowers also the sacrificial layer etch rate at the same time. Fast sacrificial layer removal can still be achieved if an un-annealed channel layer covers the whole sacrificial layer. Figure 2.22 shows measured oxide shrinkages for different annealing conditions. About 3% must be expected for a poly-silicon transducer which is anneal 12 h at a temperature between 700 °C and 800 °C.
- The etch channel layer defines the plate diameter which can be processed more accurately by an especially tuned extra etch procedure. A modified BOE solution with a strong buffer is used for etching of the channel layer (see mod. BOE in Tab. B.16). It etches as-deposited TEOS oxide with a low and stable rate of about 100 nm/min (see Tab. B.17).

It is very important to achieve reproducible etch channel geometries because they influence the etch duration of the sacrificial etch and they define the transducer diameter. It should be noted, that the etch channel inlet geometry is defined by the transducer layer mask as given in Fig. 3.32 and is less critical. The inlet cross-section area must only be larger than the overall area of all connected etch channel cross-sections. Otherwise the etchant diffusion into the cavities would be obstructed by

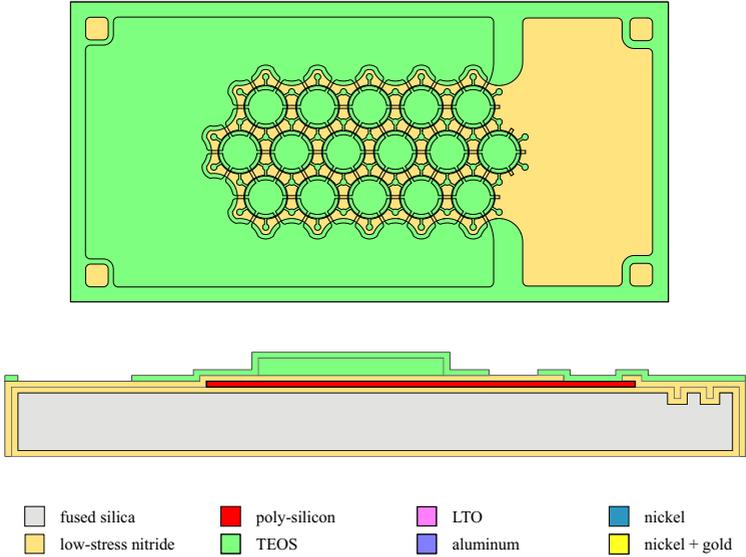


Fig. 3.31: Schematic layout and cross-section of the sensor until etch channel patterning.

the inlet. The area of three etch channel cross-sections is $5.4 \mu\text{m}^2$ for the presented design and inlets with a diameter of $2.7 \mu\text{m}$ (i.e. a cross-section of $5.7 \mu\text{m}^2$) would already be sufficient as confirmed by experiments.

It is crucial to remove all etch channel material at the transducer array support prior to transducer layer deposition. Patterning of the etch channel layer creates openings through which the underlying nitride is exposed. The transducer layer will be attached to the die surface at these openings. Any oxide residuals will cause a liftoff of the plate array during sacrificial etch. A 10 min etch in mod. BOE guarantees a complete removal and leads to a deposition thickness variation insensitive undercut of $1 \mu\text{m}$. A time-adjusted HF-dip before transducer deposition is used to thin-down the channels to precisely 300 nm, to remove any possible oxide residuals or native oxide, and to chamfers all edges.

The etch channel layer's second function is to act as a RIE stop-layer during the transducer layer patterning step. The channel layer covers the wafer surface completely and is only patterned at the location where the transducer layer must be fixed to the underlying substrate. The transducer layer design is done in a way that etch channel oxide is placed below *all* the resulting openings structured during the RIE process. This measure is very important to protect the thin nitride against RIE attack. The selectivity of the poly-silicon reactive ion etch towards oxide is high and renders the transducer layer etch uncritical. However, a $3 \mu\text{m}$ overlap results around every transducer layer feature on the wafer after this etch step causing ad-

transducer layer RIE stop-layer

ditional difficulties (see Section 3.3.5).

3.3.3 Transducer plates

Stress control is a general concern but becomes especially important for the transducer layer. The expected positive action of fused silica on the reproducibility of LPCVD layer stress is discussed in Section 2.1.2. This special feature of the substrate was utilized to adjust the stress of the transducer made out of in situ boron-doped poly-silicon.

PBOR560 is used as plate material for the presented sensor. It is fully crystalline with a very fine grained structure. This renders the material highly compressive on silicon. At the same time and for the same reason, it is under low tensile stress on silica in contrast to other types of poly-silicon as illustrated in Fig. 2.9(b). It is not possible to use crystalline as-deposited poly-silicon as transducer material on silicon because of its compressive stress although its generally more appreciable slow, well defined asymptotical annealing properties (see Fig. 2.24) make it attractive. The same films can be reproducibly annealed to a low-tensile stress on fused silica due to the existing positive thermal stress offset. The asymptotically approached stress levels (see Fig. 2.33) are a function of the annealing temperature. It is found that this function is almost linear in the temperature range between 700 °C and 800 °C. The desired stress of 150 MPa of the transducer layer can be adjusted by:

- parallel deposition of the layer on the process wafers and two additional test wafers,
- anneal of the first test wafer at 700 °C,
- anneal of the second test wafer at 800 °C,
- measurement of the layer stress on both test wafers and calculation of the annealing temperature for the desired stress level as a linear interpolation from both results.

In addition, PBOR560 offers a very fine grained structure and low surface roughness making it robust by increasing its yield stress (see Section 2.3.1). It contains boron in a level which is above the solid solubility and makes good contacts to aluminum. However, it remains the disadvantage of the inherent process inhomogeneity which is related to the boron in the LPCVD reactor. At least $\pm 1.5\%$ deposition rate and about $\pm 1\%$ stress inhomogeneity, given as typical values in Fig. 2.29, must be expected. An uncertainty for the absolute thickness of at least $\pm 5\%$ must be added to the approximation of expected process deviations. This results in a deflection deviation of roughly $\pm 6.5\%$ for a 900 nm plate at 1 bar (see Fig. C.5(b)).

As stated before, it is straightforward to adjust the sensor's sensitivity and pressure range with the plate thickness instead of changing the cavity height or the plate diameter. Thickness changes between 700 nm and 1000 nm lead to a touch-down pressure shift for the presented process from about 0.8 bar to roughly 2 bar. This range is sufficient to adjust the sensor characteristics for atmospheric pressure measurements in normal-mode or for touch-mode operation beyond 1 bar.

The transducer layer mask layout is depicted in Fig. 3.32. It can be observed that the sensor array is made out of one piece of poly-silicon including the later bond

material selection
and stress adjustment

layer thickness

layout considerations

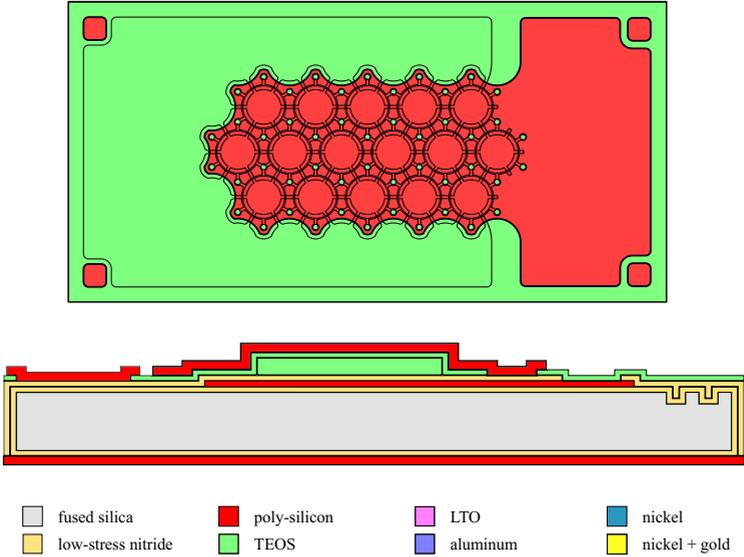


Fig. 3.32: Schematic layout and cross-section of the sensor until transducer layer patterning.

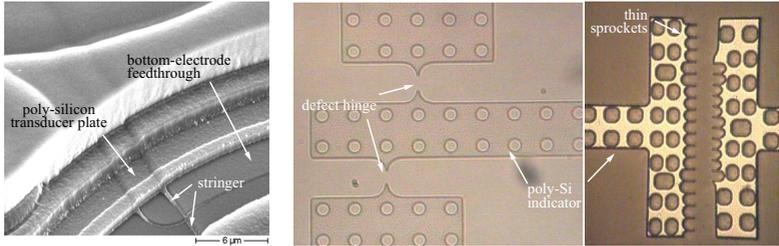
pad area. Such a layout is the most compact but with the disadvantages addressed in Section 3.3.2. The transducer layer is patterned in a RIE process which uses the etch channel oxide as stop layer to ensure that the underlying nitride is not attacked during this process step. Therefore, the poly layer must overlap the channel layer and creates an overlap of $3 \mu\text{m}$ at every transducer layer feature edge, as can be observed in the cross-sectional view of Fig. 3.32 and also in the details of Fig. 3.36. The depth of this recess is defined by the expected mask misalignment of $1 \mu\text{m}$ accounting for the standard alignment error, $1 \mu\text{m}$ for the strained silica substrate, and $1 \mu\text{m}$ for safety purpose. The consequences of these overlaps must be carefully considered:

- If the recesses are not filled in a later process step, they may cause air inclusions during sensor coating leading to reliability issues of the coating.
- If the overlaps are filled with a dielectric, this dielectric material must be very stable. Parasitic capacitances are created by the recesses which are located right over a bottom-electrode lead. Any change of the dielectric, e.g. caused by humidity penetration into the dielectric, causes a sensor offset shift.
- If the metallization should run over such a recess, step-coverage problems will arise as explained in Section 3.3.6.

All remaining layers on the backside of the wafer, i.e. transducer poly-silicon and protection nitride, should be removed prior to annealing. If not, cracks are most

layer stack on wafer back side

likely to occur on the backside. Hydrofluoric acid penetrates through such cracks and forms large cavities during the proceeding sacrificial layer etch. This may lead to particle generation and complicates the dicing procedure by lowering the wafer adhesion on the fissured and textured backside.



(a) transducer-poly stringers shorting top- and bottom-electrode (*Design-1*)

(b) thin indicator hinges due to increased isotropic etch attack of the RIE process on silica

Fig. 3.33: Negative examples of transducer layer RIE process results.

The diameter of the etch channel inlet holes and the geometry of the surface micromachined stress indicators are defined by the transducer layer mask. Especially the lateral dimensions of the indicator hinges are important and require accurate processing. For this reason, it must be noted that the isotropic etch attack of the RIE process is usually more pronounced on silica than on silicon because of the increased surface temperature of this process on the thermally insulating substrate (see also Section 2.3.1). This is influencing the indicator hinge geometry and their accuracy as discussed in Section 2.2.4. However, a positive side effect of the etch stop on the channel layer and the increased isotropic etch attack is that stringers, as depicted in Fig. 3.33, are not present or can be easily avoided by means of etch time extension.

3.3.4 Sacrificial etch

Sacrificial layer removal is one of the most critical process steps. Bulk attack through nitride cracks can cause feature destruction and the sensor's performance is greatly influenced by the magnitude of insulation nitride removal during this procedure. This removal depends on the sacrificial oxide etch rate and the selectivity of the process towards Nit-Z20. Using HF/HCl at 0 °C, as described in Section 2.3.3, increases this selectivity to roughly 1600. Some sacrificial layer etch rate data is presented in Fig. 2.40 corresponding to the geometries of the sensors and the test structures illustrated in Fig. B.10.

The actual etch rates strongly depend on the temperature and temperature gradient within the etch bath. It is found that regular agitation improves the homogeneity and rate of the process. This is in contradiction to literature [Mon94] which states that diffusion within the formed cavities limits the process rate and that agitation

etch process

agitation and process temperature

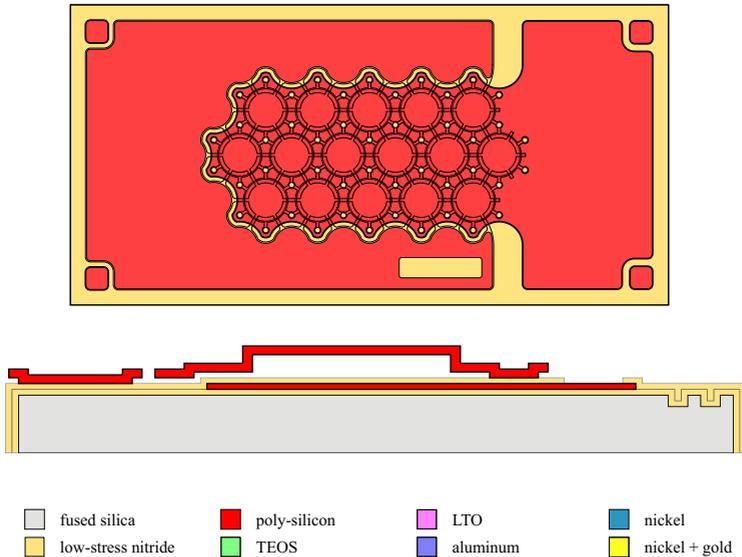


Fig. 3.34: Schematic layout and cross-section of the sensor until sacrificial layer etch.

has no effect. It is assumed that this reported observation still holds but that agitation in the presented case mainly affects the temperature homogeneity within the bath which is of high importance.

Although the selectivity of the conducted sacrificial etch is very high, still 45 nm, i.e. roughly 50 % of the nitride insulation, is removed during the required sacrificial etch of about 90 min. This removal is not indicated in the schematic illustration of Fig. 3.34, but the maximum of its magnitude is found on the exposed wafer surface and the minimum of a couple of nanometers in the center of the sensor's cavity. The sensor's insulation thickness does not greatly influence the normal-mode capacitance. In contrast, the nitride insulator dominates in touch-mode as discussed in Section 3.1.7. The concentrically thinned insulation has a positive action on the sensors linearity. The linearity of the capacitive output increases as well as the operational pressure range because saturation of the output is retarded. This can be observed in Fig. 3.64 which compares measured sensor characteristics to simulation results modeling a constant and a concentrically reduced dielectric thickness.

The mechanical transducer stress is influenced by the sacrificial etch. This can be understood if the high mechanical stress and rigidity of the nitride is considered which is deposited on top of the comparably soft silica. No nitride attack takes place underneath the array support where the poly-silicon is in contact to the nitride and protects it. On the other hand, the nitride on the wafer surface is constantly exposed

impact of selectivity
on sensor output

impact on transducer
layer stress

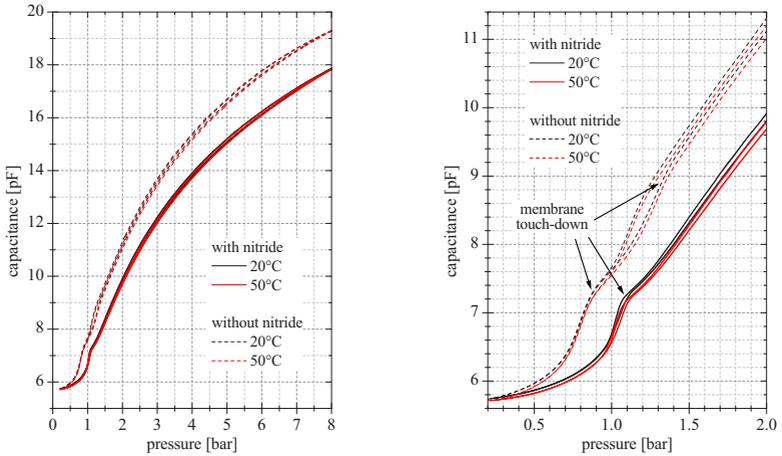


Fig. 3.35: Influence of the nitride thickness on the plate deflection. The figures compare two identically processed sensor cells which differ only in the thickness of the nitride surrounding the transducer array. The nitride of one sample was selectively removed in H_3PO_4 after channel sealing.

to fresh etchant and is therefore etched with the highest rate. This leads to a strong nitride attack around the border of the transducer array, and, in consequence, a different mechanical stress of the plates located next to the array edge in comparison to those in the array center. Different touch-down pressures for the individual transducers result and can be observed in Fig. 3.35. The graph shows capacitance versus pressure plots of two almost identically processed sensor dice. The only process variation was a nitride removal on the wafer surface in H_3PO_4 after cavity sealing (i.e. the nitride remained underneath and within the transducer array cavities). As explained in Section 2.2.5, the overall stress of silicon nitride is dominated by the thermal part and changes in the case of Nit-Z20 on silica with a rate of about 0.5 MPa/K . Therefore, not only the actual transducer stress increases with increased nitride removal, but also the temperature dependency of the transducer stress rises.

It should be noted that no surfactant is required to ensure a good wetting of the surfaces during sacrificial etch in HF/HCl . In addition, also interrupted etch procedures or previously etched wafer, which have been dried, can be re-worked with no appreciable influence on the etch front progression. This is a feature of the sacrificial etch in HF/HCl and is in contrast to etch procedures in BOE [Mon94].

Drying of the processed wafers is accomplished by means of sublimation to prevent stiction of the surface micromachined plates. The wafers are immersed for 20 min in heated tert-butanol ($\text{C}_4\text{H}_{10}\text{O}$) and put into a vacuum chamber afterwards for 30 min. Tert-butanol is solid at a temperature of 20°C (melting point: 25.7°C ; boiling point: 82.4°C) and becomes liquid if slightly heated. It freezes readily

surfactant and rework

wafer drying

when the wafers are put into the vacuum and sublimation starts. Sometimes organic residues may form on the wafer surfaces after this procedure which must be removed in an oxygen plasma.

3.3.5 Cavity vacuum sealing

The implementation of vacuum cavity seals is a critical process issue. The wrong material, process, or design could lead to an adverse impact on the sensor performance. Four issues may arise:

- **The seals are not vacuum tight.** A study with illustrative results on the impact of etch channel number, geometry, and sealant material on the sealing process is given by [Liu99]. It is found that a smaller number of channels increases the probability of complete sealing (unfortunately increasing the sacrificial layer etch duration at the same time). Furthermore, it is concluded that longer channels are advantageous for the case of high-temperature LPCVD sealing procedures, whereas the channel length has no effect on PECVD seals. This can be understood by considering re-emission as main transport mechanism in the channels and the cavity as discussed in Section 2.3.1. That is, the amount of sealant, which enters into the cavity, is defined by the area and aspect ratio of the channel inlet (gas diffusion). Once confined in the channel, the molecules will spread by multiple wall reflections (re-emission). Sealing of openings located straight at the plate edge or in the middle of the plate is most difficult. In these cases, every arriving molecule which has entered the opening is reflected into the sensor cavity. There is no macroscopic wall which may reflect the molecules back in the direction of the opening where a sealant deposition is intended. It is also straightforward that longer channels reduce the deposition thickness within the sensor cavity because more reflections are required to travel them increasing the probability of sealant adsorption in the channel. Similarly, channel geometries which increase the back reflection, i.e. channels with pointed corners, increase the sealant deposition rate next to the inlet and improve the sealing process.

etch channel design

The required minimum sealing layer thickness depends on the chosen material. Poly-silicon or nitride require only a deposition thickness of about half the channel height but CVD oxides and PECVD nitride require four to five times the channel height [Liu99]. It can be additionally suspected that the layer density of the sealant also affects its sealing capabilities.

required sealant thickness

It should be noted that CVD reactor purge cycles usually take place at deposition temperature. The diffusion coefficient depends exponentially on temperature and partial venting of the sealed cavities may take place within the reactor or during unloading. Similarly, the forming gas treatment for an aluminum metallization which is usually conducted at 300 °C–450 °C may also cause gas penetration. Especially atomic hydrogen, which is created during forming, diffuses readily through poly-silicon and crystalline silicon [Ste83].

CVD reactor purge & forming

It is necessary to consider the required transducer layer RIE etch-stop of the presented design (see Section 3.3.3). This oxide stop layer must also be lo-

actual cross-section of hermetic seal

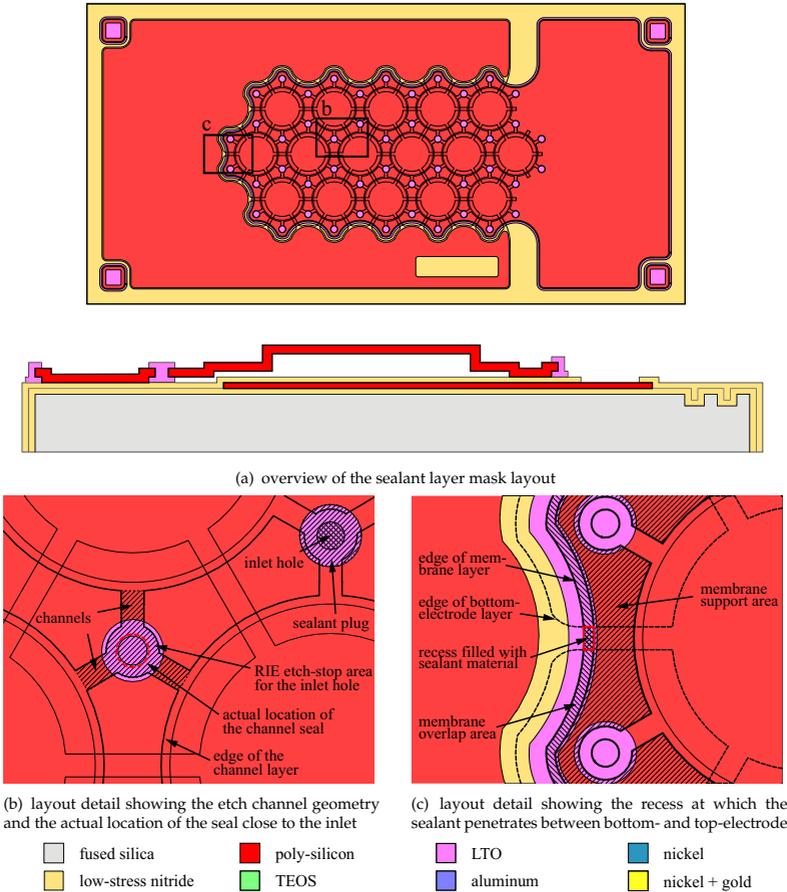


Fig. 3.36: Schematic layout and cross-section of the sensor until etch channel sealing.

cated under the inlet hole of the etch channels creating small cavities below each inlet. The resulting geometry causes the actual sealing to take place close to the edge of the inlet hole and not within the channels (see Fig. 3.36(b) and Fig. 3.39(b)). That is, all sensor cavity volumes are interconnected and puncture of a single cell causes immediate venting of all the others. This consideration is important because possible leakage increases proportional to the cross-section of the actual sealing area. This area is $15 \mu\text{m}^2$ for the presented design

(surface of the cylinder walls below the inlet) and not only the cross-section of the connected channels, i.e. roughly $8 \mu\text{m}^2$ (cross-section of three channels).

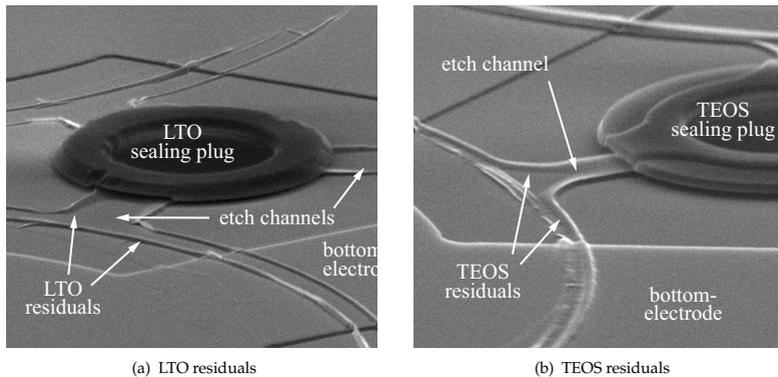


Fig. 3.37: SEM pictures illustrating the penetration of CVD sealant material into the sensor cavities. The pictures are taken from LTO and TEOS sealed sensor cells. The poly-silicon plate material was selectively removed in TMAH after seal deposition and patterning.

- The sealing layer increases the transducer thickness.** The chosen channel geometry of the presented sensor is a compromise. The hexagonal arrangement allows a maximum of three channels per inlet if the cells are closely packed. Small channel cross-sections would improve the sealing process by reducing the sealant transport into the cavities but would also increase the sacrificial etch duration, i.e. increasing the insulation nitride removal at the same time. The chosen channel geometry ($6 \mu\text{m}$ width, 300 nm height, and $11 \mu\text{m}$ length from inlet to cavity edge) guarantees sufficiently fast sacrificial layer removal rates but also leads to a sealant deposition within the cavity which has a strong impact on the sensor performance (see Fig. 3.8). An improvement would be possible if the three channels were designed with an integrated sharp bend. This measure would direct a part of the re-emitted atoms back to the inlet. The extend of sealant transport into the sensor cavities is illustrated by Fig. 3.37. It displays SEM pictures of two sensors which were sealed with LTO and TEOS, respectively. The transducer poly-silicon was removed selectively in TMAH after sealant patterning leaving the oxide sealing plugs on the surface. The transducer layer removal uncovered also oxide residuals which were deposited on the inside of the channels and sensor cavities. The thin oxide deposit in the cavity was partially destroyed during rinsing but can be closer examined in Fig. 3.39 which depicts cross-sectional views of a FIB (FIB: focused ion beam) micromachined sensor cell. The individual locations of these views are indicated in Fig. 3.38. It is found that about 45 nm of LTO is deposited at the remotest location within the sensor cavity (see Fig. 3.39(f)). This thickness is about 5 % of the transducer layer thickness

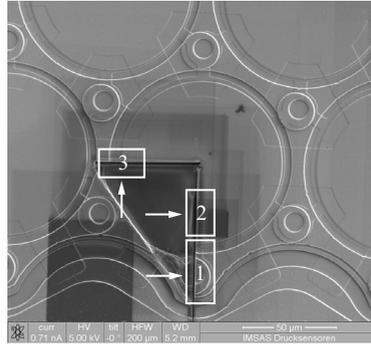


Fig. 3.38: SEM picture showing the top-view of an LTO sealed sensor cell after FIB machining. The enumerated areas correspond to the details presented in Fig. 3.39.

of 900 nm. Besides increasing the transducer thickness, it reduces the gap, exerts a stress on the sensor plate, and increases the insulation thickness.

- **The transducer stress is affected by the seal layer.** The layout of the sealant covered areas on the sensor surface must be considered carefully. The sealant must not overlap the transducer because it would have a serious influence on the stress within the plate. This makes sensor designs with very short etch channels or no channels at all unfavorable. Usually the sealant is deposited as thick as the transducer plate or even thicker. This makes it very rigid and it introduces a lot of stress into its supporting and surrounding material. Moreover, this stress is commonly not very stable because of the often chosen CVD oxides and PECVD materials which change their stress upon humidity uptake or during exposure to high temperatures (see Section 2.2.6). The adverse influence of humidity on the transducer stress was for this reason very pronounced in preceding sensor designs (see [Egg00b] for a picture of the sealant geometry). This observation influenced the sealing layer layout of the presented sensor. Initially in *Design-1*, only small plugs were placed on the inlets which were located at some distance from the sensitive plate on rigid support and no sealant material surrounded the array as can be observed in Fig. 3.21(c) and Fig. 3.23. However, coating during sensor packaging required filling of the etch-stop recess around the transducer array. This was done with the sealant material in *Design-2* (see Fig. 3.36) with the adverse influence on the sensor stability as described in the next paragraph.
- **The instable dielectric properties of the sealant.** The sealant layer overlaps the border of the transducer array in order to close the recess created by the RIE etch-stop. As consequence, also the recess above the bottom-electrode lead is filled with sealant as indicated in Fig. 3.36(c). This causes an increase of the sensor's offset capacitance of about 3.6 fF per lead which sums up to 90 fF for 25 leads. This capacitance is approximately equal to the sensor output change caused by 150 mbar at ambient conditions during normal-mode

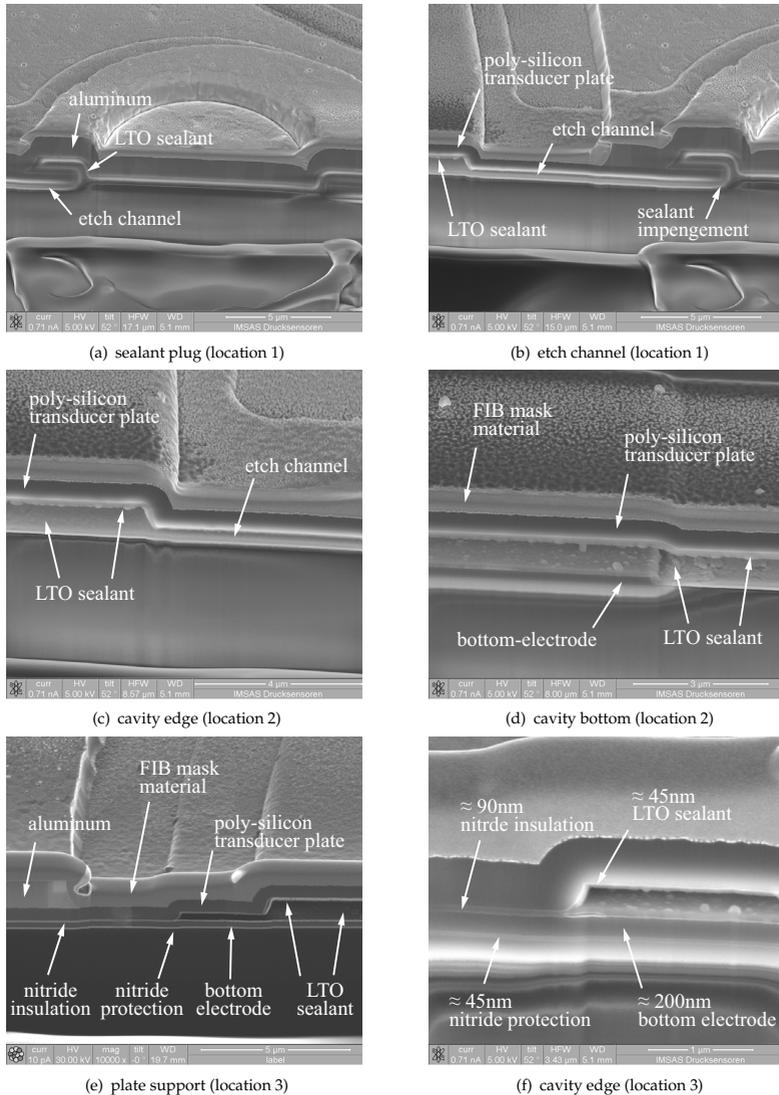


Fig. 3.39: SEM pictures of a pressure sensor cavity which was sealed with LTO. The pictures were taken after partial material removal by means of FIB machining. The top-view of the sensor with the individual locations of the given details is shown in Fig. 3.38.

operation. LPCVD silicon oxide is prone to humidity uptake and the material in the recess can cause a sensor drift in hot and humid atmosphere (see Fig. 2.15 and Fig. 2.16).

- Outgassing of residues change the reference pressure of the sensor.** Outgassing of any material which is present in the sensor's cavities can cause an increase of the reference pressure to a level far higher than the pressure of the LPCVD sealing process. Materials which can cause this high-temperature sensor instability are organic contaminations which may be present from the drying procedure (see Section 3.3.4) or oxide from the sealing procedure. In the latter case, hydrogen from the source gas is incorporated into the deposit and may exit the film during thermal treatments. Serious outgassing was observed in course of this work and the following illustrative calculation is intended to demonstrate the possible magnitude of this effect. Regardless if LTO, TEOS or PECVD oxide is used as sealant, hydrogen will be incorporated into the deposit. It is reasonable to assume a H_2 content of these typical sealant materials of at least 10 at% (already up to 8 at% are incorporated in LPCVD nitride, see Section 2.3.1 and [Ste83]). CVD oxide penetrates into the cavities during the sealing process. The pictures of Fig. 3.37 and Fig. 3.39 indicate that a thickness of about 50 nm – 100 nm can be found within the cavities after completion of the sealing procedure. Taking a film thickness of 50 nm for an approximative calculation, results in a sealant volume of $V^{(seal)} = 6.4 \times 10^{-16} \text{ m}^3$ which is deposited within a cavity volume of $V^{(cavity)} = 7.6 \times 10^{-15} \text{ m}^3$ ($V^{(cavity)} = \pi r^2 h$; $r = 45 \text{ }\mu\text{m}$, $h = 1.2 \text{ }\mu\text{m}$). The molar mass of silicon oxide M_{SiO_2} is taken to be 60.1 g/mol at a density of $\rho_{SiO_2} = 2.2 \text{ g/cm}^3$. The resulting oxide volume is equivalent to an amount of substance of

$$n_{SiO_2} = \frac{\rho_{SiO_2} V^{(seal)}}{M_{SiO_2}} = 2.33 \times 10^{-11} \text{ mol.} \quad (3.92)$$

By assuming only 1 at% to diffuse out of the calculated oxide volume, i.e. an amount of substance of $n_{H_2} = n_{SiO_2}/100$, it is possible to approximate the

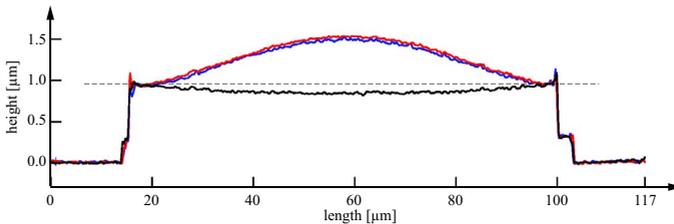


Fig. 3.40: Example surface profiles of a single sensor after PECVD sealant deposition (blue), after sealant patterning (red), and after finally venting the cavity (black). The profiles were taken with a Keyence VK-9700 Series 3D laser scanning microscope.

resulting cavity pressure at ambient temperature of $T = 293$ K

$$p_{\text{cav}} = \frac{n_{\text{H}_2} R^* T}{V_{(\text{cavity})}} = 7.4 \times 10^4 \text{ Pa} = 0.74 \text{ bar} \quad (3.93)$$

where R^* denotes the universal gas constant. Therefore, outgassing of sealant can lead to considerably high reference pressures within the sensor cavities.

Outgassing was observed during sensor development. However, it is unclear which contamination caused the outgassing: CVD oxide or organic residues. Some agglomerates which were found within sensor cavities (see Fig. 3.39(d) and Fig. 3.39(f)) make organic contaminations as gas source more likely than sealant material. The effect of outgassing on the deflection of transducer plate is illustrated by the surface profiles depicted in Fig. 3.40.

3.3.6 Metallization

Aluminum is chosen for the sensor metallization because it guarantees a sufficiently low contact resistance to the in situ boron-doped poly-silicon layers of bottom- and top-electrode by preventing *Schottky* contacts. The metal is sputtered immediately after a HF-dip and a 2 min sputter etch step onto the sensor's surface. Figure 3.41 depicts the chosen layout which intends to keep the sensor's series resistance as low as possible to improve the sensor's Q-factor. The bottom-poly is fully metal covered close to the leads at the transducer array edge. Additionally, the aluminum runs around each individual plate. This metallization of the top-poly may be omitted for the purpose of sensor stability improvement. This measure would rise the sensor's series resistance only marginally.

Five issues related to the metallization arose during sensor development:

- **Insufficient step coverage at the transducer array recess.** In *Design-1*, the transducer poly-silicon did not extend in one piece from sensor array to the top-electrode bond pad. Therefore, the aluminum metallization had to surmount the 300 nm high and 3 μm deep recess caused by the RIE etch-stop at the boundary of the transducer array (see Fig. 3.42). This could not be achieved reliably for metal sputter depositions of 1 μm no matter if the substrate was heated during deposition or not. Figure 3.42 illustrates that the surface mobility, although very low, was sufficiently high to transport the non-conformally deposited metal from the bottom corner into the recess and to impede its closure.
- **Wet chemical etching of an AlSiTi metallization.** The metallization was change from AlSiTi to pure Al during sensor process development. Remaining silicon particles on the surface after wet-chemical patterning of AlSiTi require an additional etch step (see Section 2.3.3) which also attacks the transducer layer un-reproducibly.
- **Partial venting of the seals during aluminum forming.** Usually, a forming gas treatment (see Section 2.3.1) follows the aluminum metallization. This measure improves the contact and bulk properties of the metal. However, there is a risk of partial venting of the sealed cavities which was observed if

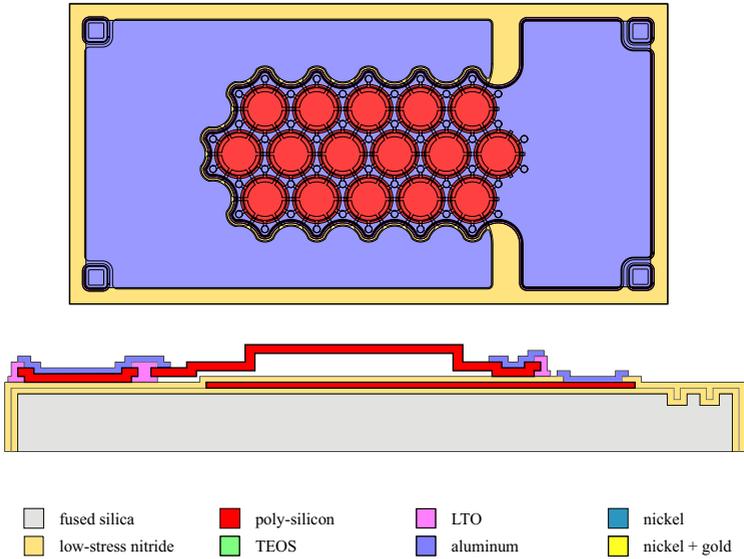


Fig. 3.41: Schematic layout and cross-section of the sensor until metallization.

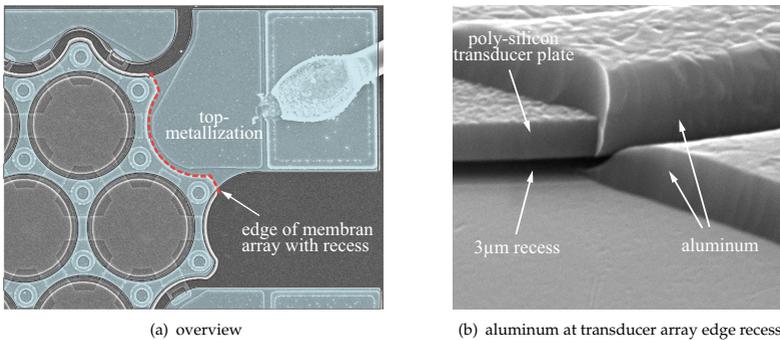


Fig. 3.42: SEM pictures of the *Design-1* top-electrode metallization illustrating the step coverage of aluminum. One micron of sputtered aluminum does not cover the RIE etch-stop recess at the transducer array edge (recess height: 300 nm; depth: 3 μm).

forming was conducted in an atmospheric reactor. Rapid anneal on a hot-plate in vacuum at 300 °C was conducted for 10 min later on and was found to decrease the contact resistance sufficiently to 50 % of the initial value (see

Tab. 2.7).

- **Stress of the aluminum around the individual sensor cells.** The stress of the metallization and its impact on the sensor needs to be considered. For this reason the metallization layout as depicted in Fig. 3.41 is questionable. An aluminum ring running around each cell must be expected to influence the stress of the enclosed transducer. The low temperature, which is required to start morphology changes within the aluminum, is supposed to cause relaxation of the metal stress and to give rise to a sensor drift at high operation temperatures (see Fig. 2.34).

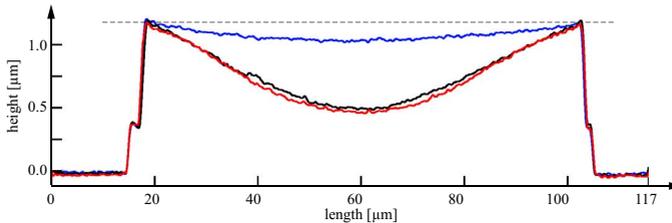


Fig. 3.43: Example surface profiles of a single sensor cell after sacrificial etch (blue), after cavity vacuum sealing (black), and after metallization (red). Sputter etching prior to aluminum deposition increases the plate deflection. The profiles were taken with a *Keyence VK-9700 Series 3D laser scanning microscope*.

- **Attack of sputter etching.** Sputter etching prior to the metal deposition is also a concern because it decreases the thickness of transducer poly-silicon and of the nitride protection layer (see Tab. 2.8 for the measured sputter etch rates). The conducted standard sputter deposition started with a 2 min sputter etch step which removes about 1 % of the transducer layer but, more important, also 18 nm of the nitride around the array. The adverse effect of selective nitride removal around the transducer array was already discussed in Section 3.3.4. It must be considered that the 90 nm of insulation nitride is under a high tensile stress of about 1150 MPa after top-poly anneal. Roughly 35 nm of it is removed during the sacrificial etch. The remaining nitride is additionally sputter etched to almost 40 % of the initial thickness. The effect on the deflection of the outer plates of the array can be observed in Fig. 3.43. This nitride attack also forbids a metallization rework, i.e. wet-chemical removal followed by a second sputter deposition. Such a procedure results in a sensor characteristic as depicted in Fig. 3.35.

3.3.7 Transducer reinforcement (reference cell fabrication)

Basic prove of concept studies have been conducted to evaluate the feasibility of the sensor reference concept described in Section 3.2.2 and illustrated in Fig. 3.22(d). It is the intention to fabricate a sensor reference to atmospheric pressure featuring transducer plates which are reinforced in the already deflected state. This goal is achieved by a reinforcement made out of electroplated metal which covers the whole transducer array of every second sensor on the wafer as depicted in Fig. 3.23. In this way two identically processed sensors can be placed on a single die, one of them acting as reference to the prevailing pressure during the electroplating process.

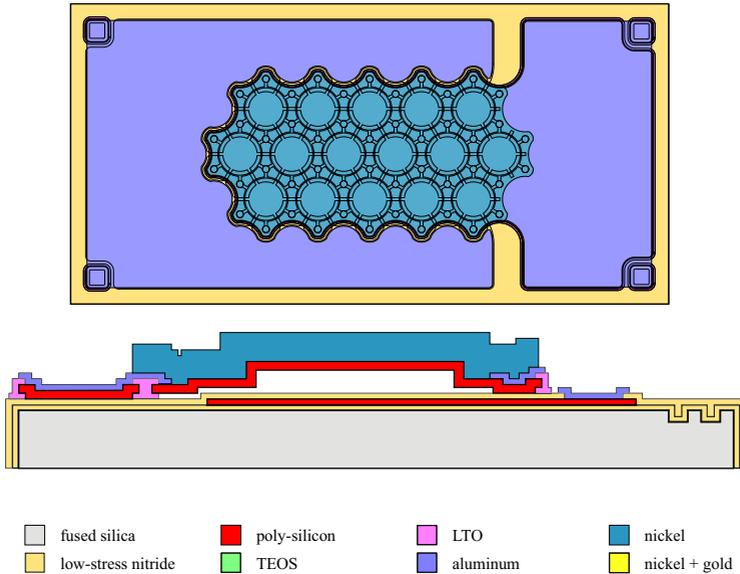
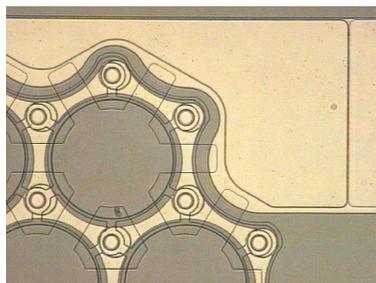


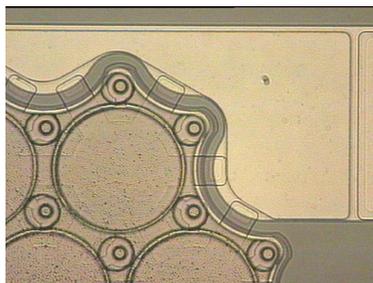
Fig. 3.44: Schematic layout and cross-section of the sensor process until fabrication of a reference cell. The transducer array of every second sensor die is optionally reinforced with an additional layer of electroplated nickel. (SEM pictures illustrating the reference design are presented in Fig. 3.23.)

A thin Cr/Au plating base (10 nm/20 nm) was sputter deposited on the wafer followed by the formation of 3.9 μm deep photoresist micro forms for the plating process (see Fig. 3.44 for the layout). A nickel sulphamate based electrolyte was used to deposit 3 μm of nickel with a non-pulsed DC current density of 5 mA/cm^2 . A homogeneity of $\pm 10\%$ was achieved under steady agitation of the electrolyte bath. A comparison of a sensor prior to and after reinforcement is depicted in Fig. 3.45(a) and Fig. 3.45(b). The mechanical stress of the fine grained layer was measured to be

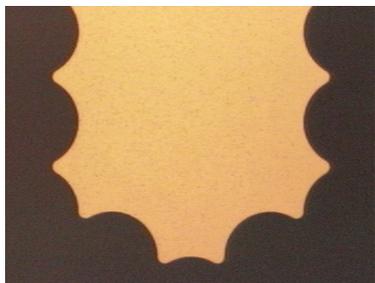
(66 ± 5) MPa with indicators as depicted in Fig. 2.7 (Young's modulus was interpolated and set to 195 GPa from the data presented in [Fri02]).



(a) sensor (*Design-1*) after aluminum metallization before reinforcement



(b) sensor (*Design-1*) after reinforcement with $3 \mu\text{m}$ of electroplated nickel and plating base removal



(c) front side view of a nickel reinforcement fabricated on a blank wafer (photo was taken after plating base removal)



(d) back side view of a nickel reinforcement fabricated on a blank wafer (photo is taken through the transparent substrate after plating base removal)

Fig. 3.45: Example photographs of fabricated transducer reinforcements. High etch rates can result during wet-chemical plating base removal in diluted etchants due to different electrochemical potentials of the metals which are incorporated within the reinforcement layer stack.

Difficulties were related to the removal of the plating base because very large undercuts are likely to occur detaching the reinforcement partly from the outer cells of the sensor array. In addition, the amphoteric aluminum of the buried sensor metallization must not be attacked. The thin layer of chromium which is only intended as adhesion promoter does not protect the aluminum during wet-chemical removal of the gold. For this reason, the Au was physically etched in an Ar plasma (10 min at 20 W and 9°C chuck temperature). Very high ratios of lateral and vertical bulk etch rates were observed during the subsequent wet-chemical Cr removal. The large undercuts may not be observed from the front side of the wafer but pictures taken through transparent test substrates revealed $50 \mu\text{m}$ wide areas of un-attached nickel after removal of the chromium adhesion layer in diluted Cr-etch (see Fig. 3.45(c) and Fig. 3.45(d)). This is caused by the different electrochemical potentials of the metals

which are stacked on the wafer surface.⁶ The undercut could be reduced to roughly $5\ \mu\text{m}$ by using concentrated Cr-etch which reduces the required etch duration to 5 sec.

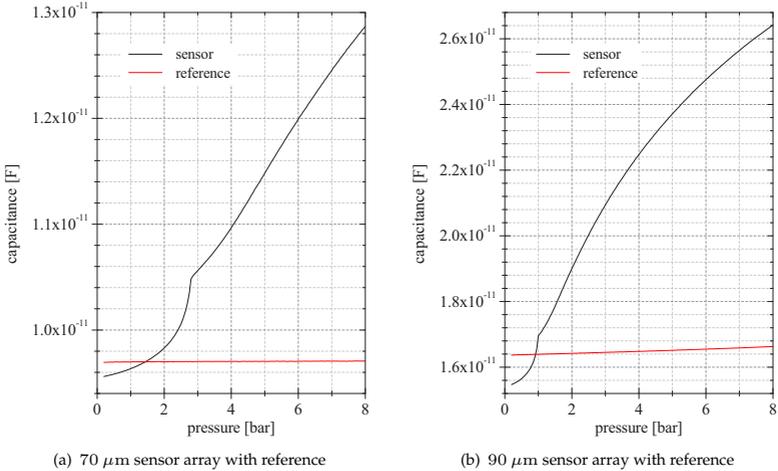
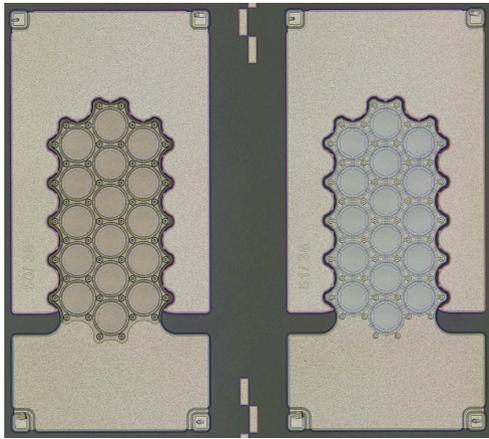


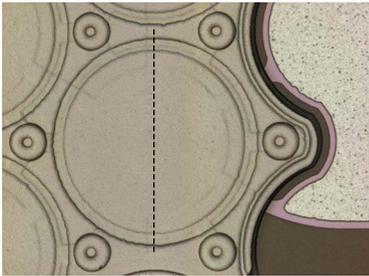
Fig. 3.46: Exemplary measurement results of fabricated sensors (*Design-1*) with atmospheric reference. The $70\ \mu\text{m}$ and $90\ \mu\text{m}$ sensor plates were made out of $815\ \text{nm}$ PBOR560 (stress: $167\ \text{MPa}$). The reference array was reinforced by a $3.35\ \mu\text{m}$ thick layer of electroplated nickel (stress: $66\ \text{MPa}$; *Young's modulus* of nickel: $195\ \text{GPa}$ [Fri02]).

Exemplary measurement results of fabricated sensors of *Design-1* with atmospheric reference are given in Fig. 3.46 (see Section 3.2.1 for a description of the implemented design variations). The array configured with sensor plates of $90\ \mu\text{m}$ diameter showed a sensitivity of $34\ \text{fF}/\text{bar}$ after stiffening with $3.35\ \mu\text{m}$ of electroplated nickel at a deflection very close to the bottom-insulation. The sensitivity of sensor cells with $70\ \mu\text{m}$ plate diameter on the same wafer was reduced to $1.5\ \text{fF}/\text{bar}$. The results are promising in both cases indicating a low impact of the intrinsic stress of the nickel layer on the transducer deflection in the reinforced state ($C_{\text{sensor}} = C_{\text{ref}}$ at $0.9\ \text{bar}$ for the $90\ \mu\text{m}$ -sensor and at $1.4\ \text{bar}$ for the $70\ \mu\text{m}$ -sensor). A *Design-2* sensor with reinforced reference is depicted in Fig. 3.47. The deflection profiles given in Fig. 3.47(d) demonstrate the feasibility of the transducer fixture in the deflected state. Wafer-level test results of sensors with fabricated reference are presented in Fig. 3.69.

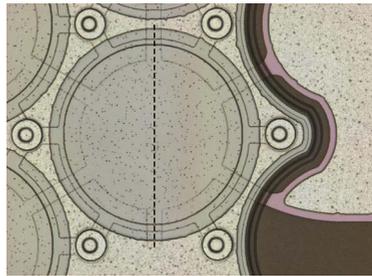
⁶ The electrochemical potential of the involved metals are: Al ($-1.66\ \text{V}$), Cr ($-0.74\ \text{V}$), Ni ($-0.25\ \text{V}$), and Au ($1.50\ \text{V}$).



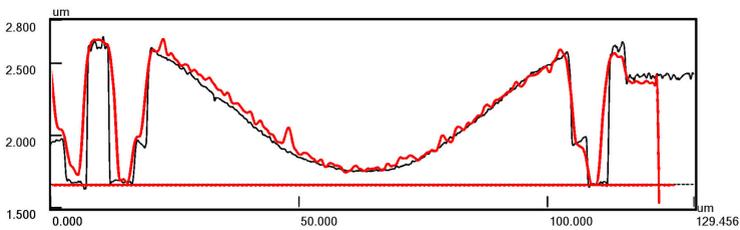
(a) sensor die (*Design-2*) with sensor array (right) and reference array (left)



(b) close-up of a single reference transducer



(c) close-up of a single sensor transducer



(d) sensor plate deflection (black) and reference plate deflection (red) at ambient pressure

Fig. 3.47: Photographs of a reinforced pressure sensor of *Design-2*. The pictures and surface scans were taken by means of optical laser scanning microscopy. Deflections profiles of sensor and reference plates were measured along the dashed lines indicated in Fig. 3.47(b) and Fig. 3.47(c).

3.3.8 Electrical vias

An electrical through substrate via is suggested in Section 3.2.3 which requires bulk micromachining of both wafer sides. A shallow front side via part is manufactured in an early stage of the overall transducer process requiring only small holes which can be sealed with LPCVD deposits. The second backside via part is fabricated in a post-transducer process.

Figure 3.48 depicts cross-sections of two possible approaches. Either a small wet etched or a dry etched front side part can be combined with a large wet etched back side via hole. The back side holes can be reduced in size by thinning the wafer as described in Section 2.4.2 (see Fig. 2.42 for SEM pics of thinned sensors) and by grouping front and back side vias as illustrated in Fig. 3.26.

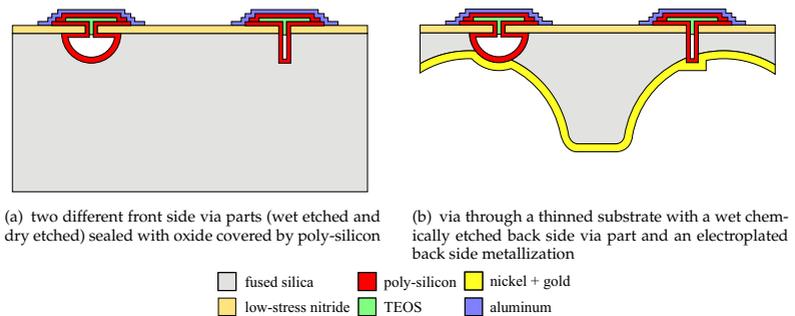


Fig. 3.48: Schematic cross-sections of bulk micromachined electric through substrate vias.

The prove of concept studies aiming at the implementation of through substrate vias have not been completed. Only the required individual process steps were evaluated:

- DRIE etching of silica (Section 2.4.1)
- isotropic etching of silica (Section 2.4.1)
- cavity sealing (Section 3.3.5 and Section 2.3.1)
- thinning of silica substrates (Section 2.4.2).

A consideration of the necessary additional process steps to integrate the via into the transducer process, shows a high risk of wafer damage and high additional costs due to a number of extra LPCVD films and lithography steps for a *wet/wet type via*. The dry/wet via concept requires a DRIE step which is not demanding with respect to depth control. It must only ensure a minimum penetration depth into the bulk material. The dry/wet via concept is favored although it was found difficult to achieve sufficiently high etch rates required for the fabrication of holes with a diameter of $2\ \mu\text{m}$. It is supposed that this would be possible with proper equipment and development time.

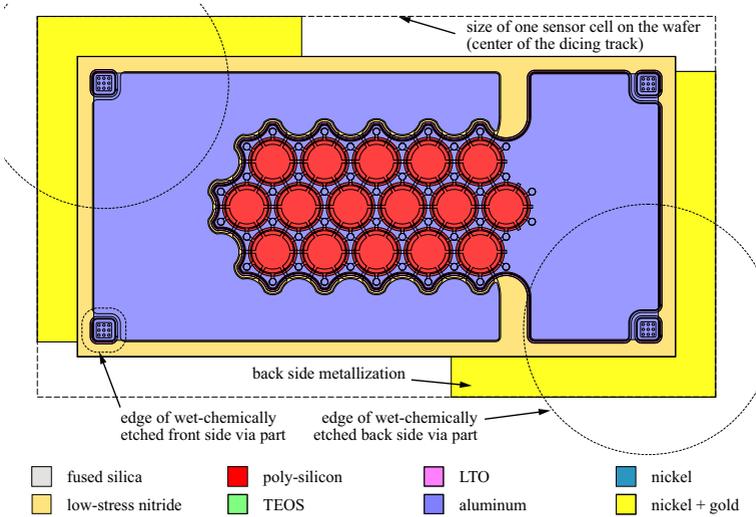
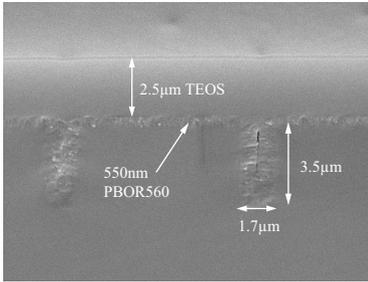


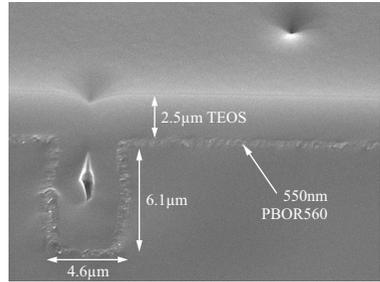
Fig. 3.49: Schematic layout of the sensor process indicating the location of optional through substrate vias. Cross-sections of the suggested vias are given in Fig. 3.48 and Fig. 3.26.

Example SEM pictures of fabricated front side vias are collected in Fig. 3.50. They demonstrate the general feasibility of etching the bulk silica wet-chemically through an inlet which is sufficiently large to coat the inner cavity with a conductive in situ boron-doped poly-silicon film but which is at the same time small enough to be sealed with CVD oxide. An example of a large back side cavity etched into the bulk silica is given in Fig. 2.41(c). The very low sticking coefficient of in situ boron-doped poly-silicon, as discussed in Section 2.3.1, yields a very high conformity of the coating in the cavities with a deposition rate close to the rate at the wafer surface (see Fig. 3.50(e) and Fig. 3.50(f)). Masks made out of a stack of silicon nitride and silicon are rigid and can withstand rinsing and other usual process stresses. The tensile stress of the silicon nitride causes a slightly negative deflection of the sensor plate as can be observed in Fig. 3.50(d) (a cross-section of the whole cavity is given in Fig. 2.41(d)).

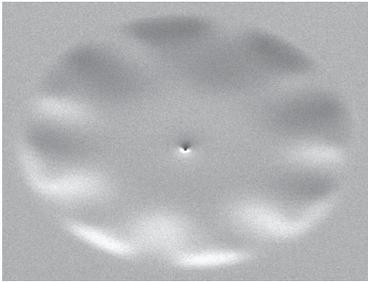
conceptual results



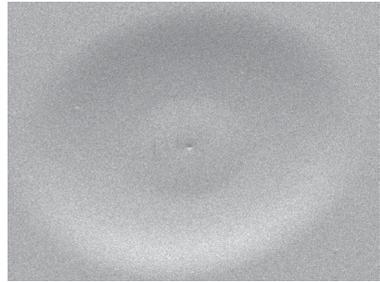
(a) cross-section of two TEOS sealed front side via parts (dry etched, 2 μm hole diameter)



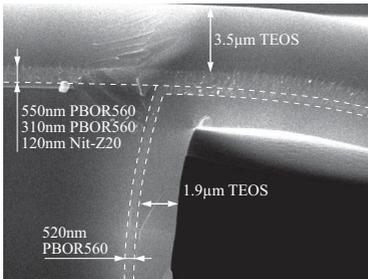
(b) cross-section of a TEOS sealed front side via part (dry etched, 5 μm hole diameter)



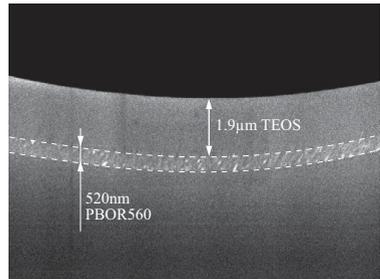
(c) front side via (wet etched, poly-silicon mask, 6 μm inlet diameter) covered with 3.5 μm TEOS



(d) front side via part (wet etched, poly-silicon/nitride mask, 3 μm inlet diameter) sealed with 3.5 μm TEOS



(e) cross-section detail of a wet etched and TEOS sealed front side via part corner (poly-silicon/nitride mask, 3 μm inlet diameter)



(f) cross-section detail of a wet etched and TEOS sealed front side via part bottom (poly-silicon/nitride mask, 3 μm inlet diameter)

Fig. 3.50: Example SEM pictures of bulk micromachined front side via cavities conformally coated with in situ boron-doped poly-silicon (PBOR560) and TEOS (TEOS4Z).

3.4 Sensor modeling and characterization

The electrical output of the presented sensor and its change due to applied pressure load will be modeled in the following section. The modeling procedure starts with a SPICE model which includes all geometry features. It will become obvious from the resulting simulation data that the complex network of electrical components in the full SPICE model of the sensor can be represented with a simplified lumped components equivalent circuit. This equivalent circuit will be discussed and its combination with the results of Section 3.1 finally give an electromechanical sensor model which is compared to the measurement data of sample sensors. The section will conclude with the presentation of measurement results illustrating some special features of the sensor such as temperature dependency, hysteresis, and drift.

3.4.1 Electrical sensor model

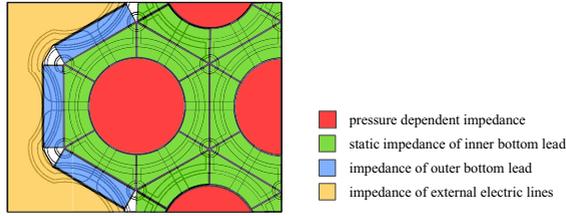
The presented sensor composes of 16 transducer cells which are switched in parallel. A complex geometry results with distinct features that can be represented by interconnected discrete electric components. It is the intention of this section to analyze the resulting circuitry and to verify if the initial goal of an easy sensor readout is achieved. Furthermore, the influence of material and geometry parameters on the sensor is discussed.

The sensor as presented in Section 3.3 can be divided into a number of repeated and interconnected features which represent SPICE model instances. These instances are illustrated by the colored areas in Fig. 3.51(a). It can be noted, that the sensor's impedance composes of contributions from 16 transducer plates, 96 inner transducer lead sections, 25 outer leads around the array, and all the circuitry from the bond pads to the sensor array. Only the red colored areas, i.e. the plate parts right above the circular bottom-electrodes, are pressure sensitive. Their pressure dependent capacitance can be calculated analytically with the formulas summarized in Section 3.1.6 and Section 3.1.7. The cross-sectional view presented in Fig. 3.51(b) indicates that each of the recurring instances again composes of a number of individual resistances and capacitances. These components have been included in an overall model for the sensor array (details are given in [Lud06]). The SPICE instances defined by Fig. 3.51(a) and Fig. 3.51(b) are all two-port networks and can be modeled with the lumped components illustrated in Fig. 3.51(c). These will be used to reduce the complex network to a simplified equivalent circuit for the whole sensor as done in the following section.

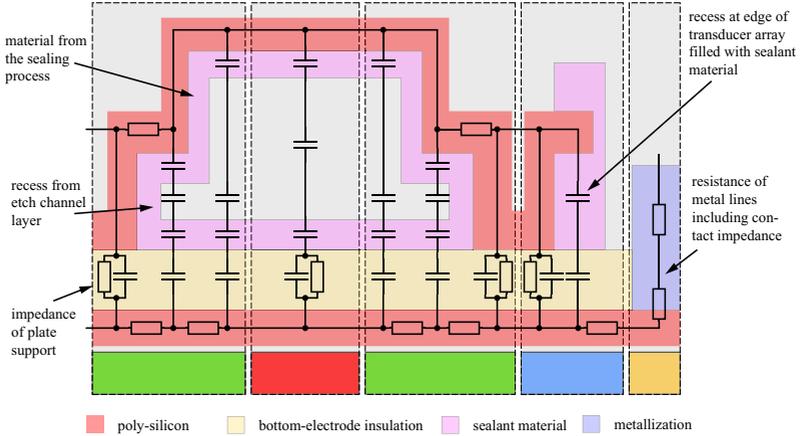
A Bode-plot of the simulated impedance for a typical *Design-2* sensor ($t_i = 90$ nm, Nit-Z20 insulation) at $P = 0$ and $P = 8$ (normalized pressure load, see Section 3.1.1) is presented in Fig. 3.52(a). It can be observed that the impedance drops over the frequency range between 1 Hz and 10 MHz with a slope of $-1/\text{decade}$ indicating that a capacitance dominates the impedance. At frequencies below and beyond this range, resistances dominate the overall impedance as indicated by the rising phase and constant magnitude. The capacitance increases with the applied pressure load. Therefore the impedance drops in the mid-frequency range shifting the curve along the y-axis. The lower impedance limits remain fixed unaffected by the change of

SPICE model including all geometry features

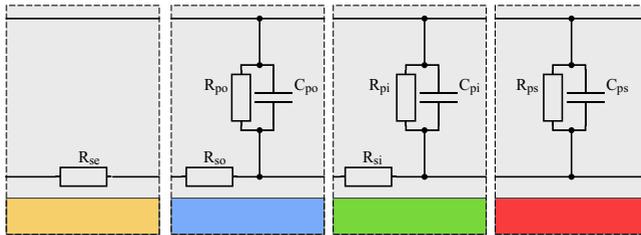
impedance change caused by pressure load



(a) Top-view of a sensor part illustrating the location of SPICE model instances.



(b) Cross-section of a single sensor element showing all included discrete SPICE model components. The colored areas below the picture indicate in which SPICE instance the elements are grouped.



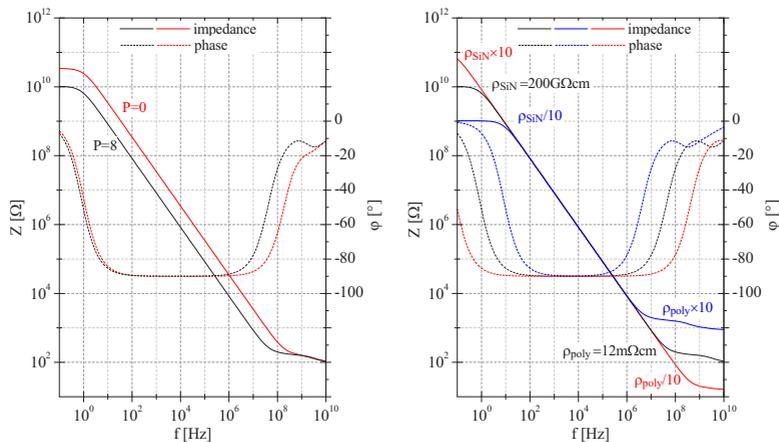
(c) Lumped element representations of the spice instances of the simplified overall sensor equivalent circuit.

Fig. 3.51: Structure of the implemented SPICE sensor model. The overall model consists of a network of 16 transducers (red), 25 outer supports (blue), 96 inner supports (green), and the electrical wiring on the sensor die including the top-electrode resistance (yellow).

capacitance. The decreasing resistance at the low-frequency limit is caused by an increasing touch area and the therefore decreasing insulation resistance.

Decreasing the resistivity of the nitride insulation lowers the asymptotically approached upper impedance limit. On the other hand, variation of the bottom-electrode resistivity (or geometry) alters the impedance at the lower limit (see Fig. 3.52(b)). Therefore, the usable frequency range is generally defined by the nitride insulation properties at low frequency and by the resistance of the poly-silicon at high frequency. However, severe changes of these resistances are required to narrow the operation range reasonably: $1/10^{\text{th}}$ of the original nitride resistivity and a 10 times higher bottom lead resistance narrows the frequency range to about 10 Hz – 1 MHz. One decade shift of either resistance results in a one decade shift of the respective operation frequency limit. This results indicate, that the sensor can be regarded as a real capacitor having a parallel and a series resistance (see circuit C in Fig. 3.60).

impact of nitride and poly-silicon resistivity



(a) effect of pressure load variation on the sensor impedance

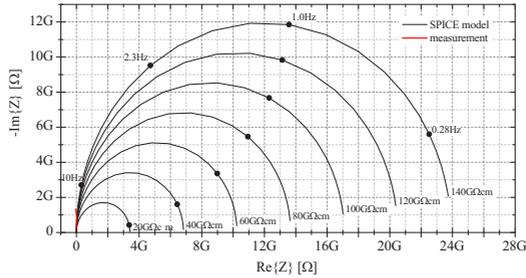
(b) effect of nitride and poly-silicon resistivity variations on the sensor impedance

Fig. 3.52: SPICE simulation results illustrating the impact of pressure and resistivity changes on the sensor output. The given data corresponds to a typical *Design-2* sensor ($t_i = 90$ nm, Nit-Z20 insulation).

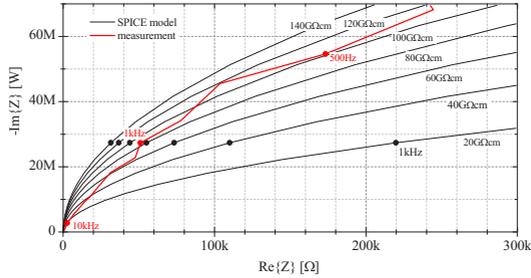
A closer observation of the *Bode*-plots in Fig. 3.52(b) shows that a single RC-network is not sufficient to model the sensor at higher frequencies. After a short saturation at high frequency the impedance drops again indicating the presence of a second time constant. *Nyquist*-plots are a further means to gain information about the internal structure of a circuit by indicating the number of involved RC-networks. A *Nyquist*-plot is obtained if the negative imaginary part of the impedance is plotted against the real part. An RC-network consisting of a single capacitor in parallel to a resistor with a series resistor yields a half circle in the imaginary half space. The diameter of this circle is equal to the parallel resistance and the circle is shifted by the

analysis of electrical structure

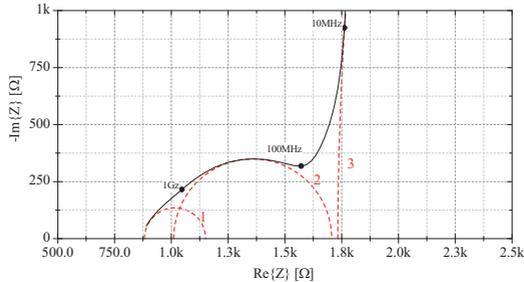
value of the series resistance along the real axis. Multi time constants from nested RC-networks manifest themselves in overlapping half circles.



(a) comparison of measurement and SPICE model for various nitride resistivities at low frequencies



(b) comparison of measurement and SPICE model for various nitride resistivities at intermediate to high frequencies



(c) high frequency detail for a sensor with a 100 times higher poly-silicon resistivity of 1200 mΩcm and a nitride resistivity of 10 MΩcm being 1/100th of the actual value

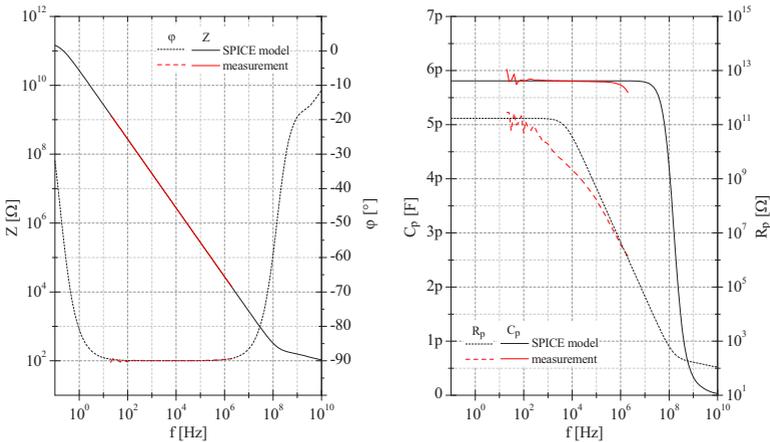
Fig. 3.53: Nyquist-plots of SPICE model and measurement data. The measurement data (full red line) of a typical Design-2 sensor ($t_i = 90$ nm, Nit-Z20 insulation) was taken with an Agilent E4890A Precision LCR Meter.

Nyquist-plots of SPICE simulation results for various nitride resistivities are presented in Fig. 3.53(a). It can be noted that the resistance of the sensor at very low frequencies is directly related to the nitride insulation properties. Actual measurement data taken in a frequency range between 20 Hz and 2 MHz with an *Agilent E4890A Precision LCR Meter* is also given in Fig. 3.53(a) as red full line. The devices are still capacitive at 20 Hz and the LCR meter measurement can not give accurate information about the DC resistivity of the insulation layer. Figure 3.53(b) presents a close-up of Fig. 3.53(a) for the frequency range above 500 Hz. It illustrates that the measurement data can not be fitted accurately with a frequency independent resistivity. This was found to be the major difficulty during low-frequency sensor modeling. Possible reasons will be discussed further below.

extraction of insulation resistivity

The internal electrical structure of the sensor at high frequencies becomes more pronounced if exaggerated resistivity values are used, i.e. a low nitride resistivity of 10 GΩcm and a very high poly-resistivity of 1200 mΩcm. The resulting Nyquist-plot is depicted in Fig. 3.53(c) showing the effect of three RC-networks. Therefore, not more than RC-networks are necessary to accurately model the sensor with an equivalent circuit over the simulated frequency range. The actual model RC-networks and their components is discussed in Section 3.4.2.

electrical high-frequency sensor structure



(a) comparison of modeled and measured impedance (magnitude and phase) (b) comparison of model and measurement data converted to a C_p/R_p parallel equivalent circuit

Fig. 3.54: Comparison of SPICE model simulation and measurement data. The measurement data was acquired with an *Agilent E4980A Precision LCR meter*. The SPICE model parameters correspond to a *Design-2* sensor at $P = 0.97$. Insulation resistivity was set to 1000 GΩcm and the resistivities of top- and bottom-electrode have been measured and set to 12 mΩcm and 9 mΩcm, respectively.

The best possible fit of SPICE model and measurement data is presented in Fig. 3.54. It is given for a *Design-2* sensor at $P = 0.97$ with a nitride resistivity of $\rho_{SiN} = 1000 \text{ G}\Omega\text{cm}$

comparison of model an measurement data

and the measured resistivities of bottom- and top-electrode: 12 mΩcm and 9 mΩcm.⁷ The fit of SPICE model to impedance phase measurement data is very good as can be observed in Fig. 3.54(a), however, deviations become more obvious if magnitude and phase of measurement and simulation data is converted with

$$C_p = \frac{1}{\omega Z} \frac{\tan \varphi}{\sqrt{1 + (\tan \varphi)^2}} \quad (3.94)$$

$$R_p = Z \sqrt{1 + (\tan \varphi)^2}.$$

The resulting curves are depicted in Fig. 3.54(b).

Equation (3.94) neglects the presence of any series resistance and simply converts the magnitude and phase into an parallel capacitance and parallel resistance equivalent circuit which should be a good approximation over a wide frequency range. A perfect capacitor with no series resistance R_s would yield a constant C_p and R_p . The capacitance and resistance drops as soon as a series resistance influences the impedance, i.e model R_p starts to drop at about 1 kHz and model C_p at 10 MHz.⁸

The drop of R_p and C_p in the SPICE model data depicted in Fig. 3.54(b) must be expected from the preceding argumentation. But the actual R_p data does not follow the model- R_p in a range between 100 Hz and 100 kHz. Also the model- C_p deviates from the measurement beyond about 1 MHz. It is supposed that this deviation is only a different aspect of the same problem as already illustrated in Fig. 3.53(b). Improvement of the fit quality could not be achieved by means of material parameter as well as structural model variation. For this reason it is concluded that an effect influences the electrical sensor output which has not been incorporated in the model so far. The following influences may be present:

- **measurement setup**

The presented measurement data was acquired on wafer-level with the setup described in Section 3.4.5. It is supposed that the measurement equipment introduced an error and tests were run to determine its magnitude.

Figure C.8(a) and Fig. C.8(b) present impedance readings of the setup with open terminals. It is concluded that the impedance meter can accurately measure high quality capacitances with an R_p up to $10^9 \Omega$ over the full frequency range (and up to $10^{11} \Omega$ at the lower frequency limit). However, the high impedance of open terminals cause a high spread of the data below 10 kHz. A high series resistance is not present in the setup which might be responsible for the drop of R_p and C_p of the sensor. The setup has a series resistance smaller than 20 Ω. It must be noted that the high-frequency drop of C_p in Fig. C.8(b) is of very small magnitude and that an additional short compensation does not have a notable effect on the results as illustrated in Fig. C.8(d).

A measurement system analysis of type 1 (MSA1) in accordance to the recom-

⁷ It can be noted that the fitted dc resistivity of the Nit-Z20 insulation layer of 1000 GΩcm is above the expected value of roughly 130 GΩcm given in Section 2.3.1 (see Fig. 2.21(a)). The limit of the measurement set-up is approached if frequencies drop below 100 Hz (see also Fig. C.8) and the actual dc resistivity might even be higher.

⁸ The C_p and R_p results can be corrected if the magnitude of R_s is known (see Appendix. C.4.3).

impact of series resistance on C_p and R_p

deviation of model and measurement data

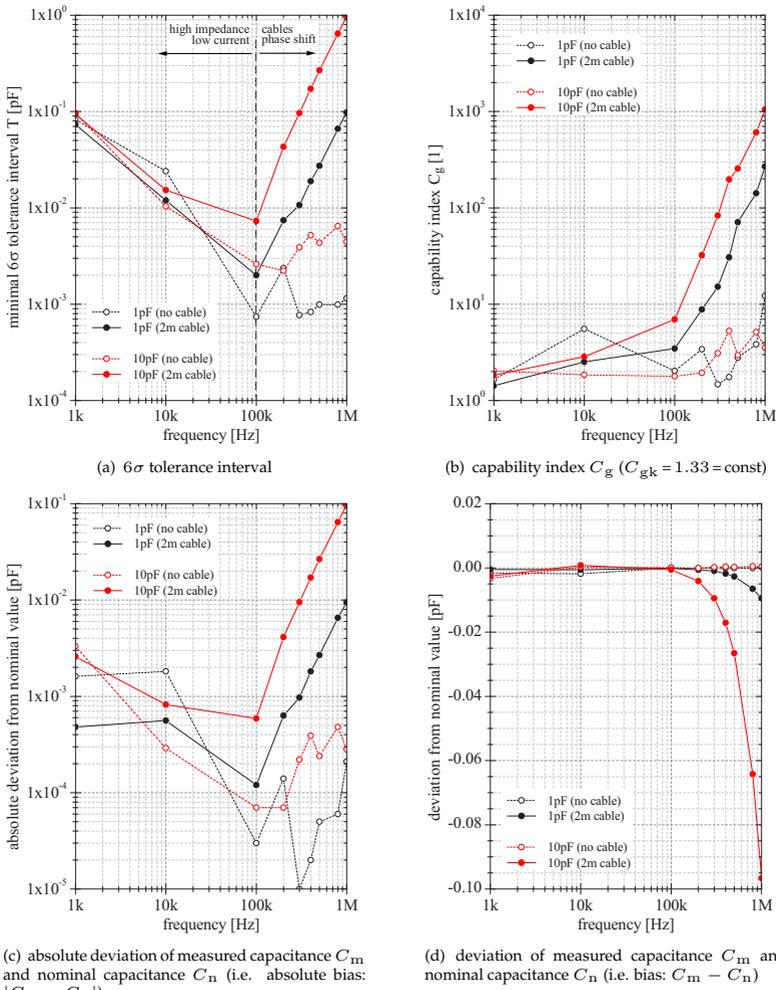


Fig. 3.55: Measurement system analysis type 1 (MSA-1) results for the wafer level test set-up according to recommendations of the *Automotive Industry Action Group (AIAG)* [Aut08]. Two *Agilent* air capacitors (nominal capacitance values: 1 pF and 10 pF) were used as standards. The MSA-1 was conducted with the standards attached to the input terminals of the *Agilent E4980A* and attached to the end of 2 m coaxial cables (meter settings: $V_{ac} = 0.5$ V, medium integration, $1 \times$ averaging, open compensation). Capability index C_{gk} was fixed to 1.33 for the calculation of the 6σ tolerance interval and capability index C_g . Deviation and absolute deviation, i.e. bias and absolute bias, were calculated from the mean value of 50 readings.

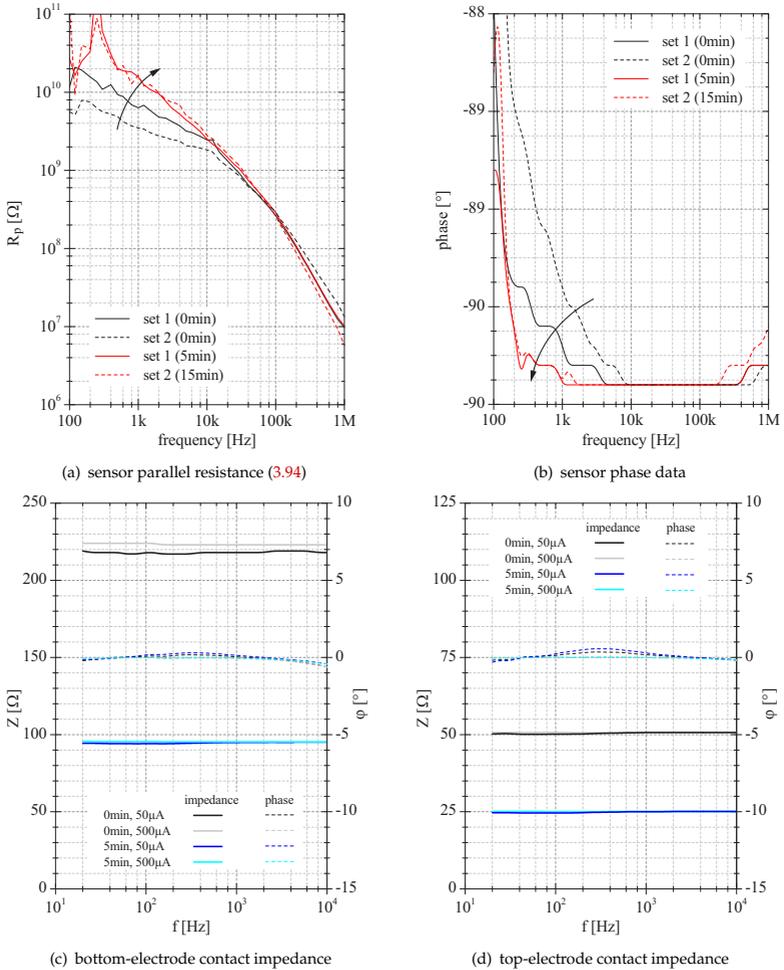


Fig. 3.56: Effect of the Al/Si contact interface on the sensor characteristics. Depicted are the mean characteristics of two sample sets (one set: 10 sensors) selected from two different wafers. Annealing was conducted at 300 °C for the indicated time in ambient atmosphere. The contact impedances were measured with *Kelvin* test structures for 50 μA and 500 μA signal level.

mendation of the *Automotive Industry Action Group (AIAG)* [Aut08] was conducted to assess the accuracy of the used wafer-level test setup. The results are summarized in Fig. 3.55 and indicate that the observed high-frequency drop of the sensor C_p can be in first place attributed to the cabling of the setup (see Fig. 3.55(d)). It can be noted that the 6σ tolerance interval increases below 100 kHz exponentially due to the low measurement currents (capability index C_g is small at these frequencies)⁹ and increases again exponentially above 100 kHz due to the used 2 m coaxial cables. The cables introduce a phase shift which can not be corrected by open and short compensation. This phase shift depends on the magnitude of the measured impedance but the maximum error does not exceed < 100 fF within the measurement range below 10 pF (see Fig. 3.55(d)). Therefore, the setup's error can not be the only reason for the drop of about 200 fF which can be observed in Fig. 3.54 or Fig. C.8(d).

- **metal/poly-silicon interface**

Annealing experiments were conducted to test the influence of the metallization on the sensor impedance. A high series resistance due to non-ohmic metal/poly-silicon contact interfaces could be suspected to cause the observed deviations between model and measurement data.

Measured contact resistance data is summarized in Fig. 2.36 and Tab. 2.7. It can be noted that the contacts of aluminum to the implemented in situ boron-doped poly-silicon (PBOR560) layers are ohmic after annealing for 5 min at 300 °C. The contact resistance drops from roughly $25 \text{ k}\Omega\mu\text{m}^2$ to $8 \text{ k}\Omega\mu\text{m}^2$ during anneal resulting in a very low dc resistance of the bottom- and top-electrode contact pads ($8 \text{ k}\Omega\mu\text{m}^2 / (500 \mu\text{m} \times 250 \mu\text{m}) < 1 \Omega$).

It can be speculated that the ac resistance of the metal/poly-silicon interface might be of high magnitude or frequency dependent. For this reason the ac contact resistance was measured with *Kelvin* structures with the results depicted in Fig. 3.56(c) and Fig. 3.56(d). It can be observed that the ac contact resistance does not depend on frequency but only changes in magnitude during anneal.

However, the metal anneal lead to a drop of the sensor's phase and an increase of R_p (see Fig. 3.56(b) and Fig. 3.56(a)). Additionally, the differing parallel resistances of the two sample groups (selected from two different wafers) resemble each other after anneal and the measurement results become more reproducible.¹⁰

The action of the metal interface on the sensor characteristics is unclear. It may influence the impedance at low-frequency but does not provide an explanation for the drops of R_p and C_p at high-frequency.

- **dielectric insulation**

It must be noted that the discussion in Section 2.3.1 on the insulation properties of low-stress silicon nitride focused solely on the *dc properties* of these films. These theoretical results are in good agreement with the observations

⁹ Information on the MSA-1 procedure and the derived quantities of tolerance interval, capability indexes and bias can e.g. be found in [Six08].

¹⁰ $1/f$ noise and the related resistivity change of the poly-silicon itself may be considered as explanation [Mic98].

(high R_p for f approaching 0 Hz). No experiments on the low- and medium-frequency resistivity of dielectrics have been conducted and discussed in this work.¹¹ A frequency dependency of the Nit-Z20 low-stress silicon nitride below 2 MHz should be expected. Reports on experiments with RF sputtered¹² SiN_x show a decreasing permittivity and an increasing ac conductivity for an increasing frequency below 20 kHz [Gou03]. Such a behavior could explain the observed drop of C_p and R_p . Measurements of capacitive test structures having two metal electrodes and a PECVD oxide dielectric show a distinct frequency dependency. Metal electrodes were implemented to eliminate any possible influences of semiconductor/metal or semiconductor/dielectric interfaces on the measurement result. The obtained impedance data presented in Fig. C.9 is in agreement with [Gou03] showing a decline of the permittivity with increasing frequency. Similar test capacitors with metal electrodes could not be fabricated with an LPCVD SiN_x insulation because of the required high deposition temperature but a similar trend for the permittivity can be suspected. Therefore, it is concluded that the dielectric bulk properties of the implemented Nit-Z20 insulation will have an effect on the frequency characteristic of the sensor with, however, uncertain magnitude.

- **poly-silicon/insulator interface**

Interface trapped charges influence the bias and frequency response of metal oxide semiconductor (MOS) capacitors [Sze81, p. 380] [Nic82, p. 176]. A high number of interface traps are commonly present at silicon/ SiN_x interfaces (see Section 2.3.1). These traps are distributed over the whole band gap. They are continuously charged and discharged during application of an ac voltage across the MOS device. These traps can have time constants of several seconds and generally cause energy dissipation when charges exit traps tardy and transfer their excess energy to the crystal lattice. Such an interface related dissipation is commonly modeled as a frequency dependent resistance in MOS capacitors [Nic82, p. 201].

The effect of the silicon/insulator interface on the CV characteristics of metal

Table 3.4: Summary of CV plot fit parameters for low-stress silicon nitride and thermally grown dry oxide (see Fig. 3.57 and Fig. 3.4 for the CV plots).

dielectric	ϵ [1]	V_{ms} [V]	N_A [m ⁻³]	N_Q [m ⁻²]
$\text{SiN}_{1.04}$	7.4	-0.98	4×10^{22}	3.4×10^{16}
SiO_2	4.05	-0.97	2.3×10^{22}	9.4×10^{15}

insulator semiconductor (MIS) structures have been analyzed in course of this

¹¹ The high-frequency properties were measured by means of spectroscopic ellipsometry. The dispersion of the two important dielectric layers, i.e. Nit-Z20 (insulation) and LTO (sealant), are depicted in Fig. C.7. These can be well modeled with a Lorentz oscillator (see Section C.4.1). A pronounced high dissipation must be noted for low-stress silicon nitride if compared to the imaginary part of the LTO permittivity.

¹² RF sputtered silicon nitride exhibits similar insulation properties like LPCVD nitride.

work [Her06] [Wic08]. Low-stress nitride, TEOS, LTO, and thermal dry oxide were deposited on $0.5 \Omega\text{cm} - 1 \Omega\text{cm}$ p-type substrates. All samples had an aluminum top-electrode and a back side metallization. A *Keithley 590 CV Analyzer* was used to acquire CV data at an ac level of 15 mV at 100 kHz and 1 MHz. The bias voltage was swept in all cases from -20 V to $+20 \text{ V}$ and back with various delay times between each 0.5 V voltage step. In addition, the influence of a infra-red illumination on the CV curve was tested. Exemplary results are summarized in Fig. 3.57 and Fig. 3.58 for Nit-Z20 and thermal dry oxide, respectively. The CV data for dry oxide is presented for the purpose of comparison. It can be noted that in this case sweep speed variations as well as frequency variations do not affect the onset of depletion, i.e. do not shift the CV curve. Deep depletion can be observed during the positive bias sweep and equilibrium is only attained during the reverse sweep. This changes if the samples are exposed to infra-red illumination increasing the minority carrier generation. The data for thermal dry oxide can be closely fitted to the CV curve of an ideal MOS capacitor as shown in Fig. 3.58(d) with the formulas summarized in Section C.5 and the fit parameters given in Tab. 3.4. In contrast, the CV plots of low-stress nitride (Nit-Z20, $\text{SiN}_{1.04}$) presented in Fig. 3.57 show a distinct dependency on the sweep speed. The higher the delays are chosen between the bias steps the narrower becomes the hysteresis between up and down sweep. This excludes dielectric charging as cause for curve shifts but indicates interface trap time constants of several seconds. Furthermore, curve shape and onset of depletion shifts with frequency. This stretch-out is characteristic for the influence of interface traps [Sze81, p. 382].

The CV data obtained at the lowest sweep speed is closest to the ideal characteristic and was used for parameter extraction. The fit depicted in Fig. 3.4 corresponds to the data given in Tab. 3.4 with a trap density of $3.4 \times 10^{16} \text{ m}^{-2}$. It is in good agreement with literature data stating trap densities of $(3 - 5) \times 10^{16} \text{ m}^{-2}$ [Hu66] [Dea68] (see also the discussion on the dielectric properties of low-stress nitride in Section 2.3.1).

The dielectric/silicon interface causes dissipation and influences the magnitude of the measured capacitance of a MIS device. Therefore, it is concluded that the insulation/*poly-silicon* interface similarly influences the sensor characteristics. The number of interface traps and their energy dissipation should be at least of the same order. However, more work is required to determine the frequency and temperature dependency of the $\text{SiN}_{1.04}$ /poly-silicon interface.

- **depletion of bottom-electrode leads**

The observed influence of interface traps, frequency, and illumination is most pronounced when the semiconductor is depleted. The transducer layer poly-silicon overlaps the bottom-electrode leads at the plate support resulting in a structure very similar to a thin film transistor. Depletion of the p-type bottom-lead could be suspected if the top-electrode is positively biased. It may act as gate electrode on top of the 200 nm bottom-poly lead. Surprisingly, biasing does not change the capacitive sensor reading significantly. Cause is most probably the sensor's tolerance towards series resistance. (A $10 \times$ higher lead resistance may not be noted in C_p as shown in Tab. 3.6.)

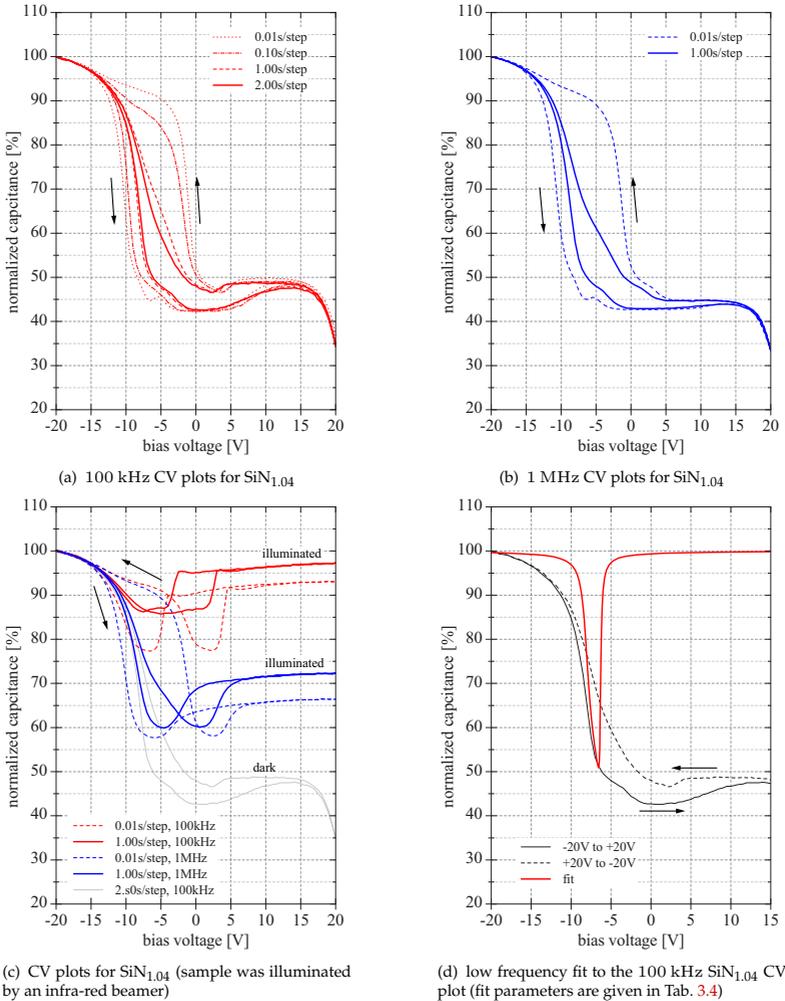


Fig. 3.57: CV measurement data of a MIS capacitor with 91.8 nm $\text{SiN}_{1.04}$ dielectric. The indicated step times denote the delay after each 0.5 V bias step (bias was swept in both directions starting from -20 V). All samples had a aluminum top electrode and back side metallization. p-type substrates with a resistivity of $0.5 \Omega\text{cm} - 1 \Omega\text{cm}$ were used. The data was acquired with a *Keithley 590 CV Analyzer* at an ac voltage level of 15 mV.

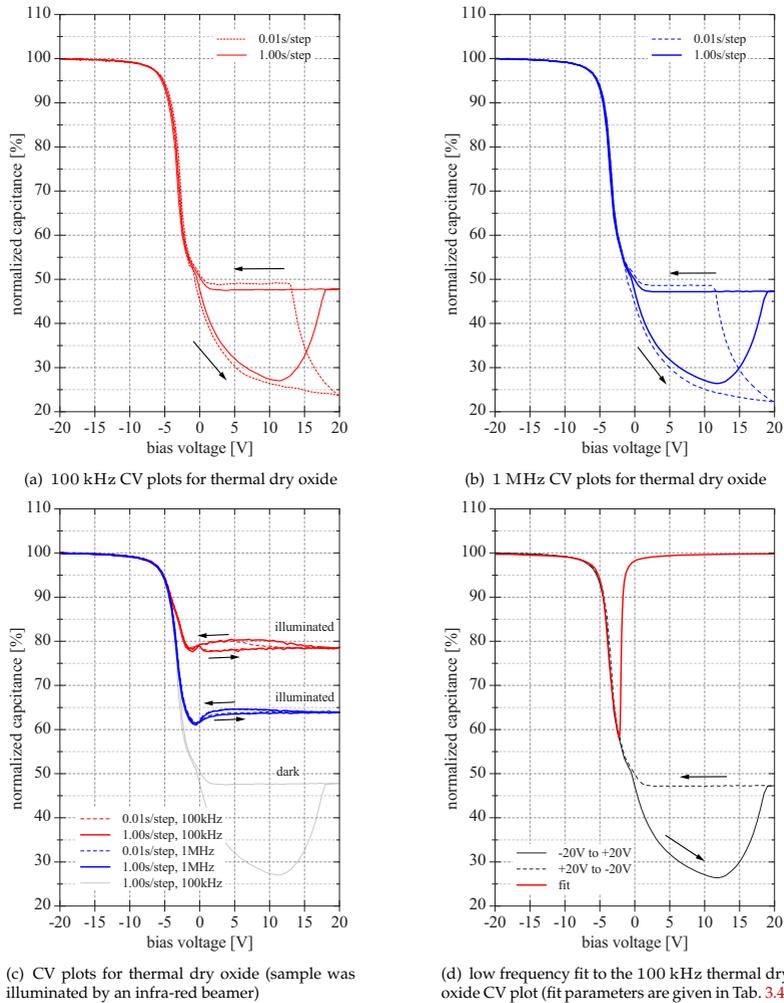


Fig. 3.58: CV measurement data of a MOS capacitor with a 87 nm thermal oxide dielectric. The indicated step times denote the delay after each 0.5 V bias step (bias was swept in both directions starting from -20 V). All samples had a aluminum top electrode and back side metallization. p-type substrates with a resistivity of $0.5 \Omega\text{cm} - 1 \Omega\text{cm}$ were used. The data was acquired with a *Keithley 590 CV Analyzer* at an ac voltage level of 15 mV.

summary of
conclusions

The conclusions of the preceding discussion on the fit of a structural equivalent SPICE model to the sensor measurement data can be summarized as follows:

- The overall sensor characteristic is very similar to a two terminal capacitor with parasitic resistances.
- The insulation resistivity determines the parasitic parallel (dc) resistance and limits the operation range at low-frequency.
- The poly-silicon resistance of top- and bottom-electrode determine the parasitic series resistance and limits the operation range at high-frequency.
- The overall sensor can be represented by a network of not more than three RC-circuits.
- A single C_p , R_p , R_s circuit can be expected to be a sufficiently accurate equivalent circuit over a wide frequency range (and even the series resistance might be neglected below 1 MHz).
- Additional effects influence the sensor impedance being either related to the dielectric, the poly-silicon/insulator interface, or the poly-silicon/metal interface.

The general structure of the equivalent circuit is derived but the actual values of the required components must still be calculated from the sensor geometry and material data. This is done in the preceding section.

3.4.2 Equivalent circuit

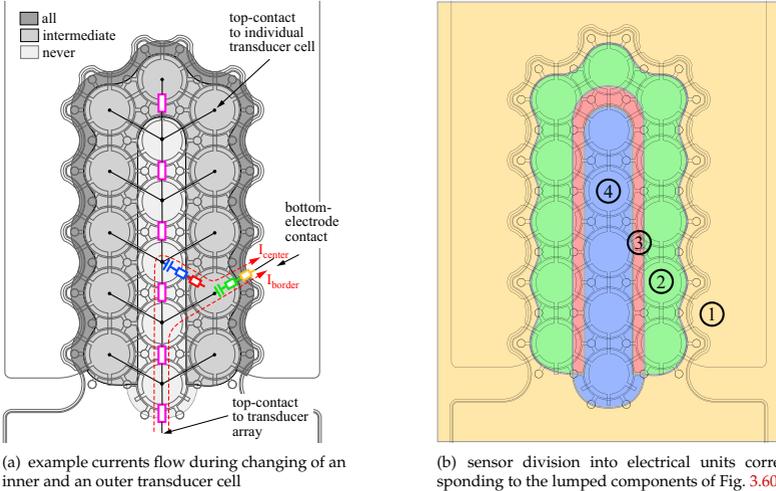
A SPICE model consisting of a complex network of individual discrete components reflecting all geometric features of the presented sensor was discussed in the preceding section. It was found that this model, here referred to as the *full model*, can be approximated with three interconnected RC-networks. This section will identify which individual components must be grouped to form the lumped components of such a simplified equivalent circuit.

grouping of elements for the
equivalent circuit

The equivalent circuit structure is found by following the current flow through the sensor. No matter if it charges a center cell or a cell at the border, it must exit the sensor through 25 bottom leads at the circumference of the array. It can be noted that the series resistances decreases concentrically for all capacitive elements which are charged during sensor operation. This is illustrated by $I^{(center)}$ and $I^{(border)}$ in Fig. 3.59(a). Therefore, a concentric grouping of the individual discrete spice elements is necessary as indicated by the colored areas in Fig. 3.59(b). This results in a circuit structure **A** with lumped components as depicted in Fig. 3.60 (the area numbers correspond to the numbers in the component's subscripts of the equivalent circuits). The boundaries on these areas are located where the bottom-electrode geometry causes a high series resistance. It can be observed that four interconnected RC low-pass filters result.

calculation of
lumped components

All sensor capacitances are charged by a current which enters the transducer array top-electrode at the contact pad. It passes three transducer cells at a time on its way to the last cell at the array tip (see Fig. 3.59(a)). The average top-electrode resistance is denoted by R_{s1t} . It can be neglected in the case if a metallization runs around each transducer cell as illustrated in Fig. 3.41. R_{s1t} is in series connected to the rest of the



(a) example currents flow during changing of an inner and an outer transducer cell
 (b) sensor division into electrical units corresponding to the lumped components of Fig. 3.60

Fig. 3.59: Division of the complex sensor geometry into electrical units for a lumped components equivalent circuit. These units are determined by high resistance legs of the bottom lead resulting in the discrete components groups indicated by the colored areas in Fig. 3.59(b). A concentrically increasing series resistance is present as illustrated in Fig. 3.59(a). (The frequency range at which the sensor output is affected by the series resistance of the individual group is indicated by the grey shaded area.)

equivalent circuit (see Fig. 3.60). The lumped components are defined in Fig. 3.51(c) having subscripts with the general meanings of: **t**op, **b**ottom, **s**eries, **p**arallel, **i**nnner support, **o**uter support, and **e**xternal wiring including contact resistance. Their values can be calculated with the formulas summarized in Appendix C.4.4.

The components of circuit **A** form four RC-networks interconnected in a low-pass filter structure. Therefore, the series resistance R_{s3} and R_{s4} of the inner bottom-leads can only influence the output at low-frequency but are under these conditions much smaller than the respective R_{p3} and R_{p4} . These series resistances are omitted in simplified circuit **B** with no appreciable effect on the impedance (see Fig. 3.61). The sensor becomes resistive at approximately 10 MHz as can be observed in the example presented in Fig. 3.61(a).¹³ The reason is that the large inner capacitance ($C_{p2} + C_{p3} + C_{p4}$) shorts its parasitic parallel resistance at this frequency. Therefore R_{s2} is in parallel to C_{p1} shorting it. If frequency further increases the impedance of C_{p1} drops below the impedance of R_{s2} and the overall impedance again decreases and the phase drops slightly. The sensor's series resistance of bottom- and top-electrode dominate the output at frequencies beyond roughly 1 GHz. A comparison of actual measurement data to the impedance of the equivalent circuits **B** and **C**, including the results from the full model, are depicted in Fig. 3.62. No significant de-

successive equivalent circuit simplification

comparison of lumped and full model

¹³ Exaggerated resistance values have been used to make the features of the Bode-plot more distinct.

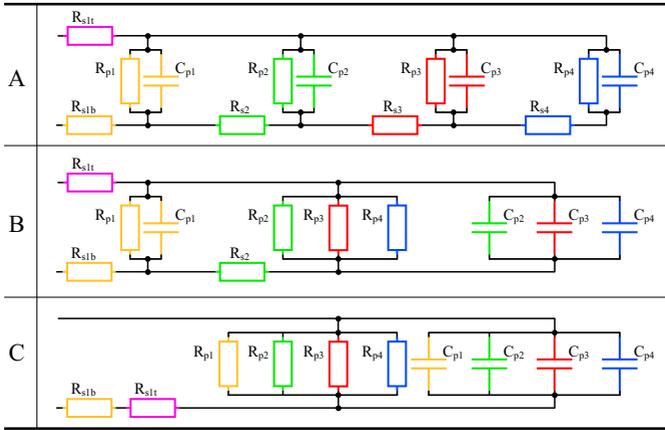


Fig. 3.60: Simplified lumped components sensor equivalent circuits. The subscripts correspond to the electrical units defined in Fig. 3.59(b). Fig. 3.51 indicates which individual components, i.e. geometric features, are condensed in the lumped components of circuits A to C.

viation between the equivalent circuits can be noted within the measured frequency range. Again the discrepancy in the R_p data can be observed as already discussed in the preceding section.

The following conclusions can be drawn from the discussion of the sensor equivalent circuit:

1. The sensor can be well approximated in the relevant frequency range below 1 MHz with the simplified equivalent circuit C depicted in Fig. 3.60 which can be condensed to the circuit given in Fig. 3.63. The components of this equivalent circuit can be calculated with

$$\begin{aligned}
 C_{\text{sensor}} &= 16C_{\text{ps}} \\
 C_{\text{offset}} &= 96C_{\text{pi}} + 30C_{\text{po}} \\
 R_p &= \left(\frac{1}{16}R_{\text{ps}} + \frac{1}{96}R_{\text{pi}} + \frac{1}{30}R_{\text{po}} \right)^{-1} \\
 R_s &= \frac{1}{25}R_{\text{so}} + R_{\text{s1t}}.
 \end{aligned} \tag{3.95}$$

2. The time constant of R_{s2} and C_{p1} determines the upper operation frequency limit. It is the RC network formed by the inner leads to the bottom-electrodes of cells located at the array border and the overall capacitance outer array support.
3. The time constant of the overall parasitic parallel insulation resistance and the overall capacitance determines the lower operation frequency limit.

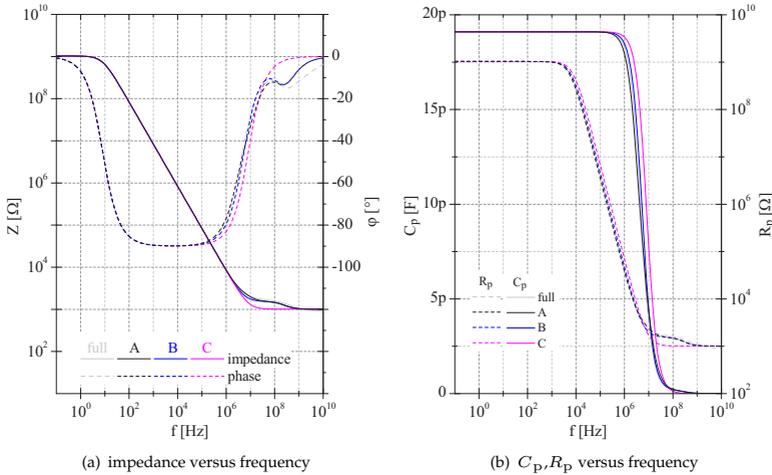


Fig. 3.61: Comparison of the *full model* SPICE simulation result to the impedances of simplified equivalent circuits **A** to **C** presented in Fig. 3.60. The data corresponds to a typical *Design-2* sensor ($t_i = 90$ nm, NiT-Z20 insulation). The resistance of the top- and bottom-poly was set to $1/10^{\text{th}}$ and $10\times$ the actual value, respectively, for the sake of illustration. C_p , R_p values were calculated with (3.94).

4. The series resistance of the inner bottom leads have no significant effect. They may be designed with a smaller width to lower the sensor's capacitive offset.
5. The width of the outer bottom-electrodes can be reduced to approximately one tenth with no significant effect on the impedance below the frequency of 1 MHz. This measure would lower the sensor offset capacitance.
6. The top-electrode metallization around each sensor cell can be omitted with no effect on the impedance below 1 MHz.

3.4.3 Electromechanical model

The structure of the electromechanical sensor model is given by Fig. 3.63, where C_{sensor} sums up the 16 pressure dependent capacitances C_{ps} of the individual transducer cells. C_{ps} can be calculated with the analytic formulas of Section 3.1.7 and the static offset impedance is defined by (3.95) and (C.4.4). Effort was spent to simplify the electrical and electromechanical sensor model but it was found that many parameters strongly influence the actual sensor characteristics. A summary of these quantities is given in Tab. 3.5. Of course, the exact sensor geometry must be known, i.e. lateral dimension and also layer thicknesses. In addition, the electrical properties such as resistivity, contact resistivity, and permittivity are required. More difficult to determine are the mechanical moduli and stresses. The moduli do not change

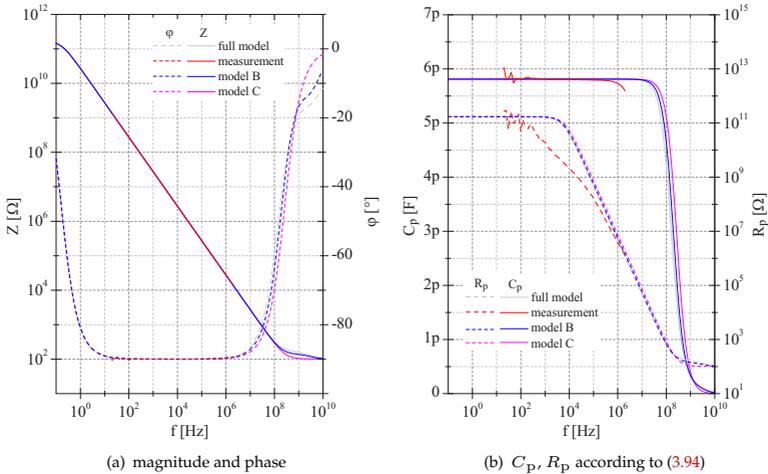


Fig. 3.62: Comparison of measurement data to the impedance of simplified equivalent circuits. Measurement data was acquired with an *Agilent E4890A Precision LCR meter* from a *Design-2* sensor at $P = 0.97$.

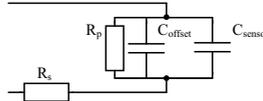


Fig. 3.63: Sensor equivalent circuit for operation below 1 MHz. The components can be calculated with (3.95).

significantly and could be measured by the procedure described in Section 2.2.3 but the determination of the actual stress in the individual transducer plate is difficult. This stress differs even between the plates within a single array, as has already been mentioned in Section 3.3.4. It is affected by all deposits in the vicinity of the individual transducer (see also Section 3.4.5). Parameters such as sealant thickness, surface roughness, and wet-chemical attack of the nitride insulation within the vacuum cavities of the sensor have significant impact on the characteristics in touch-mode and are difficult to measure. Finally, the approximative analytical approach for the mechanical sensor model followed in Section 3.1 is an additional origin for deviations between model and measurement data.

It must be expected that the overall error of a model with so many parameters is very high. However, general trends can be predicted and the importance of individual features and parameters can be tested. An example fit is presented in Fig. 3.64. The strong influence of the bottom-electrode insulation surface properties would not have been recognized without the application of the electromechanical model. A far

insulation surface
roughness & thickness

Table 3.5: Summary of electromechanical sensor model parameters.

group	parameters
lateral geometry	bottom electrode: lead lengths, radius; sacrificial layer radius; channel layer: radius, recess depth at array border; transducer support geometry (insulated overlap area of transducer and bottom-electrode poly); contact areas: top electrode, bottom electrode
etch rates	under cuts: bottom-electrode, channel layer, sacrificial layer; insulation layer etch rate during sacrificial etch (+sacrificial layer etch duration)
layer thicknesses	bottom t_b ; insulation t_i ; sacrificial t_{ss} (including shrinkage); channel t_c ; transducer h ; seal in cavity t_s ; surface roughness in cavity t_r
electrical properties	permeabilities: insulation ε_i , sealant ε_s ; resistivities: insulation ρ_{SiN} , bottom-poly ρ_b , top-poly ρ_t (or sheet resistance $R_{\square top}$); contact resistivities: bottom R_{cb} , top R_{ct}
mechanical properties	transducer layer Young's modulus E , Poisson number ν ; transducer layer stress σ_{top} ; deflection at 0 bar w_{min} , deflection w + angle at support ϑ at $P < 1$

more sensitive touch-mode device would result without consideration of surface roughness. A roughness of $t_r = 20$ nm (t_r represents the total thickness of the two contact interfaces, see Fig. 3.13) was necessary to achieve reasonable fit results. In addition, the effect of the concentric insulation attack during sacrificial etch became obvious during model development. It can be noted in Fig. 3.64 that the touch-mode model data is linearized and approximates more closely the measurement data if a concentrically decreasing dielectric thickness is incorporated. This is because saturation of the mechanical transducer deflection is partly balanced by a concentrically decreasing β as defined by (3.65) (in this example: $\beta_{center} = 0.036$, $\beta_{edge} = 0.023$).

During model development was realized that no adequate agreement of model data and measurement result could be achieved until a compliant plate support, an initial deflection, a layer stress, and large deflections are incorporated in the analytical model. These influences have been discussed in Section 3.1.6 and each have a significant impact on the result. For the presented example, a support compliance of $\gamma = 0.11$ was measured with (3.27) leading to a $K^{(elastic)}$ of 0.725 and therefore lowering the touch-down pressure more than 25 % from $p_t = 0.96$ bar to 0.7 bar. On the other hand, the present layer stress of 200 MPa and large deflections cause a $K^{(large)}$ of 2.05 approximately doubling the value of the actual touch-down pressure being finally 1.45 bar. This value is, almost surprisingly, very close to the measured p_t of 1.4 bar.

Individual parameters greatly influence the sensor and model performance and it must be supposed that these can not be measured with sufficient accuracy. There-

support compliance,
stress, & large deflec-
tion

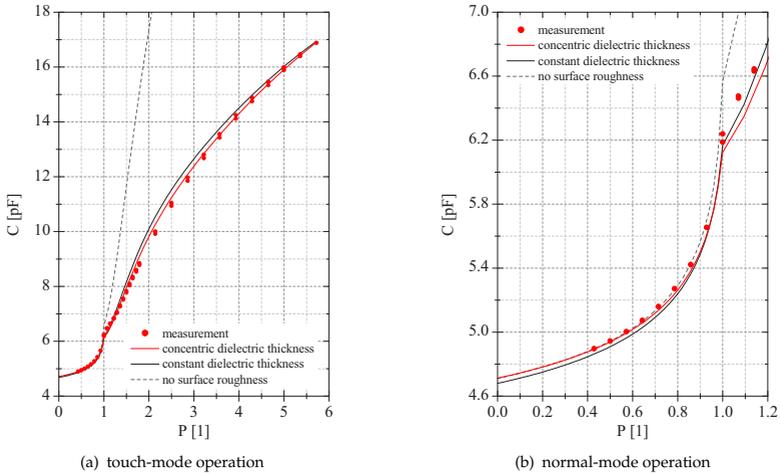


Fig. 3.64: Comparison of measured and electromechanically modeled sensor characteristics. The touch-mode capacitance was calculated using (3.80) and (3.88) for a constant and a concentric insulation layer thickness, respectively.

fore, the approximative model may not be used to predict the sensor characteristics of a new design but to forecast the effect of changes due to process variations. This is done for the presented prototype model in the next section.

3.4.4 Design and process variations

Table 3.6 summarizes the lumped component's values for the discussed typical *Design-2* sensor of the preceding sections. Values of individual model parameters have been varied (red colored) to demonstrate their influence. The presented examples highlight:

- the direct relation of insulation resistivity ρ_{SiN} and R_p .
- the direct relation of poly-resistivity ρ_{poly} and R_s .
- the impact of the top-electrode resistivity if metal is omitted (+ 100 Ω).
- the effect of undercut variations during the bottom-electrode etch procedure. The wet-etching process is developed to result in an undercut of 0.5 μm and an overall lead width of $w_b = 6 \mu m$. Increasing the undercut to 0.8 μm reduces the lead width by 10 % to 5.4 μm and decreases the offset capacitance by 10 %. At the same time the overall series resistance of the sensor increases by only 3 Ω .
- the effect of insulation layer thickness variations. A 10 % thinner dielectric increases the offset capacitance by 11 %. At the same time, the sensor capacitance in touch-mode increases by only 4 %. This can

be understood by considering the influence of sealant and surface roughness within the sensor cavity as discussed in Section 3.1.7 ($t_r = 30$ nm, $t_s = 1$ nm, $\varepsilon_i = 7.5$, $\varepsilon_{\text{eff}} = 2.18$). A 10% thinner dielectric increases C_{sensor} during normal operation at $P = 0.97$ by only 14 fF, i.e. 0.8%.

Table 3.6: Calculated values for the lumped components of the simplified equivalent circuit as depicted in Fig. 3.95. The presented data corresponds to a typical *Design-2* sensor. t_i and w_b denote the Nit-Z20 insulation layer thickness and bottom lead width, respectively.

P	[1]	0	0.97	8.00	0.97	0.97	0.97	8.00	0.97
ρ_{SiN}	[TΩcm]	1	1	1	0.1	10	1	1	1
ρ_{poly}	[mΩcm]	12	12	12	120	1.2	12	12	12
t_i	[nm]	90	90	90	90	90	90	81	90
w_b	[μm]	6.0	6.0	6.0	6.0	6.0	6.0	6.0	5.4
top-metal		no	no	no	no	no	yes	no	no
R_s	[Ω]	150	150	150	1500	15	48	150	153
R_p	[GΩ]	171	171	52	17.1	1708	171	46	189
C_{offset}	[pF]	4.06	4.06	4.06	4.06	4.06	4.06	4.51	3.67
C_{sensor}	[pF]	0.62	1.79	15.00	1.79	1.79	1.79	15.63	1.78

3.4.5 Sensor characterization

This section summarizes typical characterization results either acquired on wafer level or sampled from packaged dice. The homogeneity of offset capacitance and sensitivity has been tested on wafer level to evaluate the impact of process variations and their influence on the achievable yield. Known good dice were selected afterwards and stress tests were run to access the sensor's stability under the common qualification conditions as listed in Tab. 3.3 and Tab. C.1. These package level testing results are demonstrating the influence of temperature, pressure cycling, humidity, and bias voltage stress on the sensor characteristics.

Test setup: wafer level

It was the aim of this work to address the demand of low fabrication costs by implementation of a new surface-micromachining process which guarantees high homogeneities and consequently high yields. Therefore, the prototypes were 100 % mapped on wafer level to assess if this goal was met. Testing was performed on a *Süss MicroTec AP200 BlueRay* equipped with a *Süss MicroTec Pressure Probe Module (PPM)* [Sus08]. The PPM is basically a small nozzle which is placed above each device during probing (see Fig. 3.65(a) and Fig. 3.65(c)). It supplies a controlled flow of nitrogen which exerts a relative pressure on the tested device. The actual flows for the individual pressure load steps are calibrated once prior to testing. This is done by placing the nozzle over a reference sensor inlet hole in the prober chuck. The accuracy of the PPM is specified to be $\pm 0.7\%$ full scale, i.e. ± 49 mbar for a full scale pressure of 7 bar (relative pressure). Calibration is done for a fixed gap between device under test and nozzle. The recommended nominal gap is $40\ \mu\text{m}$ which was increased to $200\ \mu\text{m}$ to make the setup less sensitive to contact height variations. These are expected to have a magnitude of $\pm 20\ \mu\text{m}$ with an effect on the accuracy of the applied pressure as illustrated in Fig. 3.66. The impact of gap deviations decreases for increasing nominal gap values. Therefore, the largest nominal gap should be chosen still enabling the application of the highest required pressure load step, which is limited by the selected gap and the maximum nitrogen supply pressure of 10 bar. It can be noted from Fig. 3.66(d) that the overall error is below ± 65 mbar (including the probe module error of ± 49 mbar and the separation error) for the chosen gap of $200\ \mu\text{m}$.

The impedance data was acquired with an *Agilent E4980A Precision LCR meter* and the electrical cabling as given in Fig. 3.65(b). A discussion on the accuracy of the test setup was presented before in Section 3.4.1 and is summarized in Fig. 3.55. It illustrates that the setup's accuracy is best at 100 kHz (6σ tolerance interval: 2 fF for a 1 pF load and 7 fF for a 10 pF load). As consequence, wafer level testing was conducted at a test frequency of 100 kHz.

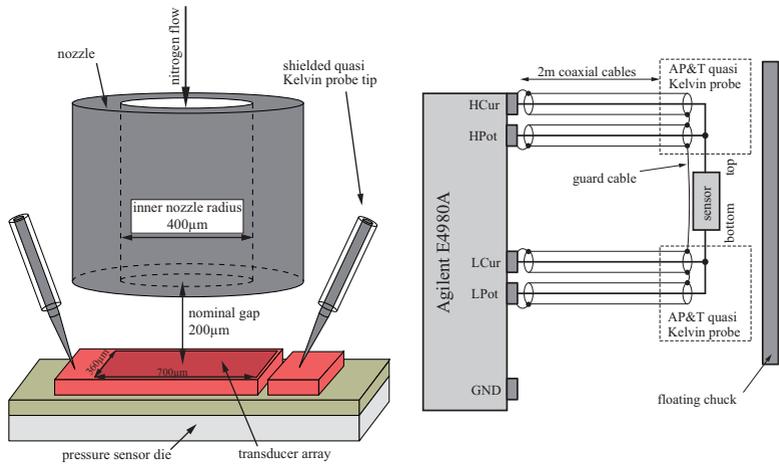
A settling time of 0.8 sec per pressure step was used which resulted in an overall wafer level test time of 3.6 sec per die. This includes electrical data acquisition and the index step summing up to 300 min overall test time per 10 cm wafer with 5000 dice.

wafer level
pressure application

pressure accuracy

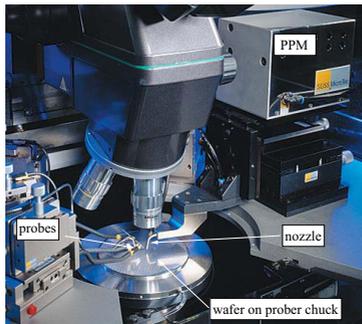
electrical accuracy

testing time



(a) schematic drawing of a wafer level test setup with a *Siiss MicroTec Pressure Probe Module*

(b) electrical design of the implemented wafer level test setup



(c) photograph of a *Siiss MicroTec Pressure Probe Module* mounted on a wafer prober [Sus08]

Fig. 3.65: Functional principle and electrical design of the implemented wafer level test setup.

Results: yield, offset capacitance, sensitivity

Exemplary wafer level test results are presented in Fig. 3.67 and Fig. 3.68 showing histograms of the measured capacitances and sensitivities for sensors operating in normal- and touch-mode. It can be observed that the process yields an offset capacitance spread of ± 150 fF in normal operation, i.e. $\pm 3.5\%$ of the nominal value of 4.4 pF at 1.0 bar. The offset spread of $\pm 3.5\%$ corresponds to an insulation thickness variation of approximately ± 3.15 nm or a bottom-electrode undercut variation

normal-mode
results

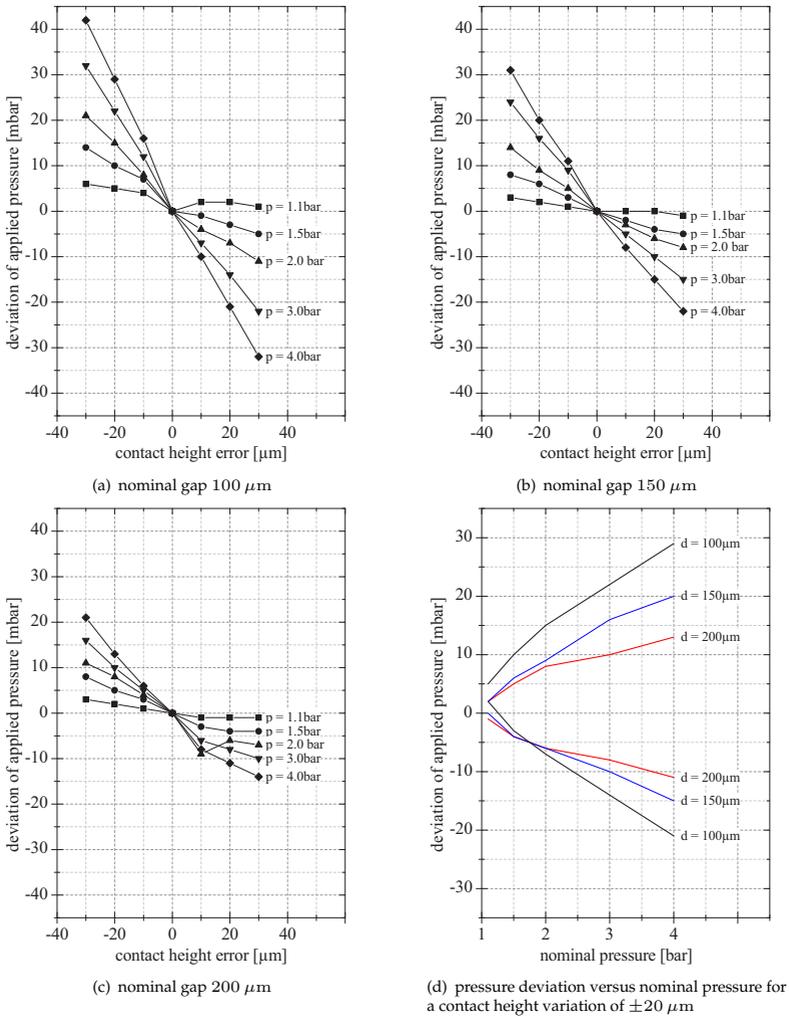


Fig. 3.66: Error of applied pressure as function of contact height variations for a wafer level test setup using a *Stüss MicroTec Pressure Probe Module*. The error is given for three nominal nozzle to wafer surface gaps (100 μm , 150 μm , 200 μm) as function of contact height variation which alters the actual gap between nozzle and surface.

of ± 210 nm (see Tab. 3.6). The sensitivity spread is about 12.5 % at a mean value of $300 \text{ fF}/\text{bar}$. These results include 90 % of the 5000 sensor dice on a 10 cm substrate. The small offset spread in normal operation is indicative for the homogeneity of the bottom-electrode wet-etch procedure and the homogeneity of the nitride insulation thickness. The sensitivity distribution reflects in first place the reproducibility of the transducer geometry and stress. Besides this, possible errors of the test setup caused by the PPM have the highest impact during normal-mode characterization at low relative overpressures. Such load errors introduce an additional scattering into the results.

The presented touch-mode example of Fig. 3.68 shows a spread of $\pm 350 \text{ fF}$ ($\hat{=} \pm 4.5 \%$) of the 8 pF offset-capacitance at 2 bar and a sensitivity of $1800 \text{ fF}/\text{bar} \pm 85 \text{ fF}/\text{bar}$ ($\hat{=} \pm 4.7 \%$) measured at 3.5 bar. These results include 95 % of the sensor dice on the wafer. A narrow distribution of the offset capacitance in touch-mode demonstrates both a homogeneous transducer layer stress and a reproducible fabrication of all feature dimensions. The touch-mode sensitivity is primarily related to the bottom-electrode insulation layer thickness and surface properties including surface roughness, unintentionally deposited sealant, and all other contaminations within the sensor cavity.

The presented normal- and touch-mode results are promising and good yields of up to 95 % were realized in the prototype fabrication runs. The observed defects, in order of their occurrence, were: broken cavity seals, contaminations within the sensor cavity, pattern transfer defects (mask defects, particles, scratches), and sticking.

A new reference concept was suggested in Section 3.2.2 and further discussed in Section 3.3.7. Every second sensor on the wafer is reinforced at ambient pressure with an additional electroplated metal layer. This yields a reference to atmospheric pressure which can compensate fabrication related offset capacitance shifts of touch-mode transducers. Example wafer level test results of this concept are presented in Fig. 3.69. Distinct two peaks in the capacitance histogram can be noted for each pressure step, one for the reference cells and one for the actual sensors. Similarly, two peaks can be observed in the sensitivity histogram. Again the results represent approximately 95 % of the dice on the wafer. These results demonstrate the general feasibility of the suggested approach but show that the reference cells are still sensitive to the applied pressure. Their sensitivity of $200 \text{ fF}/\text{bar}$ is roughly 88 % lower compared to the mean sensor's sensitivity of $1700 \text{ fF}/\text{bar}$. However, the $3 \mu\text{m}$ electroplated nickel reinforcement may need to be designed thicker to further decrease their sensitivity.

touch-mode
results

yield & defects

sensors with atmo-
spheric reference

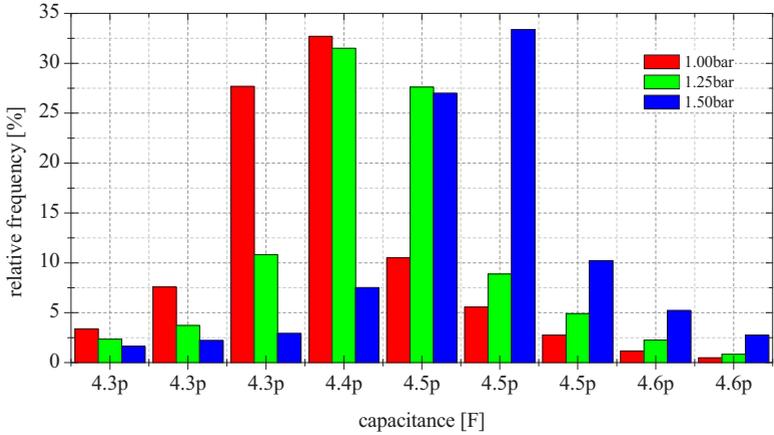
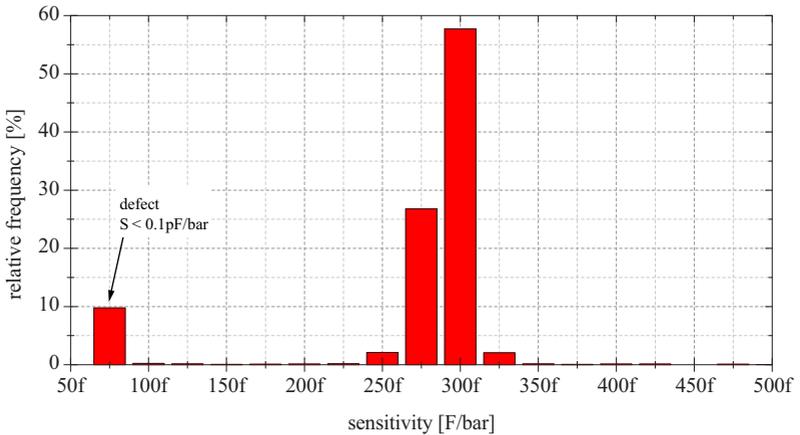
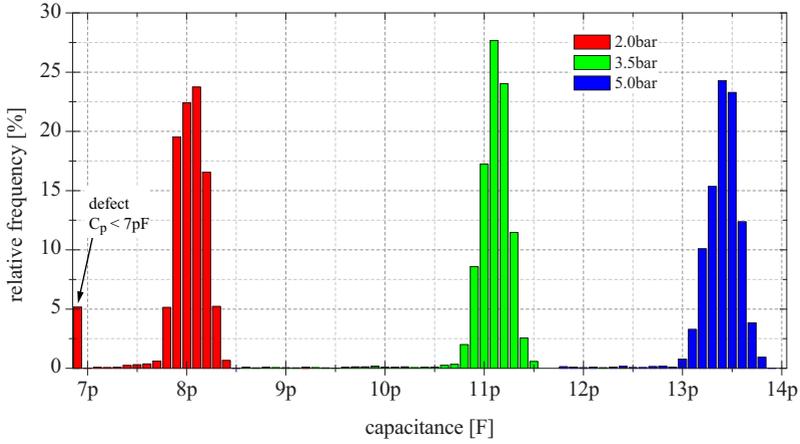
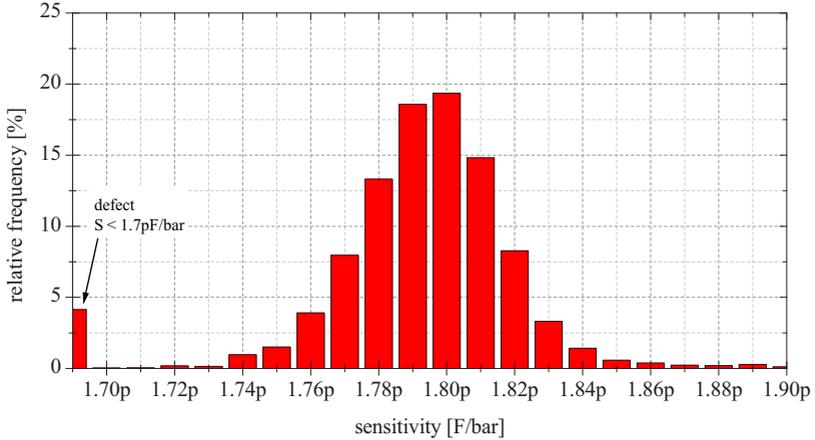
(a) capacitance at three pressure loads (± 25 fF interval width per category)(b) sensitivity at 1.5 bar (± 12.5 fF interval width per category)

Fig. 3.67: Histograms of normal-mode capacitance and sensitivity. 100 % testing was conducted on wafer-level using a *Süss MicroTec AP200 BlueRay* equipped with a *Süss MicroTec Pressure Probe Module*. The capacitance data was acquired with an *Agilent E4980A Precision LCR meter*.



(a) capacitance at three pressure loads (± 50 fF interval width per category)



(b) sensitivity at 3.5 bar (± 5 fF interval width per category)

Fig. 3.68: Histograms of touch-mode capacitance and sensitivity. 100 % testing was conducted on wafer-level using a *Siiss MicroTec AP200 BlueRay* equipped with a *Siiss MicroTec Pressure Probe Module*. The capacitance data was acquired with an *Agilent E4980A Precision LCR meter*.

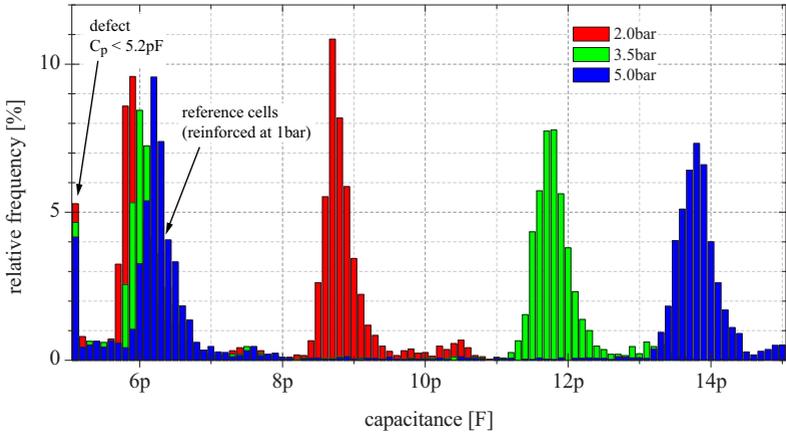
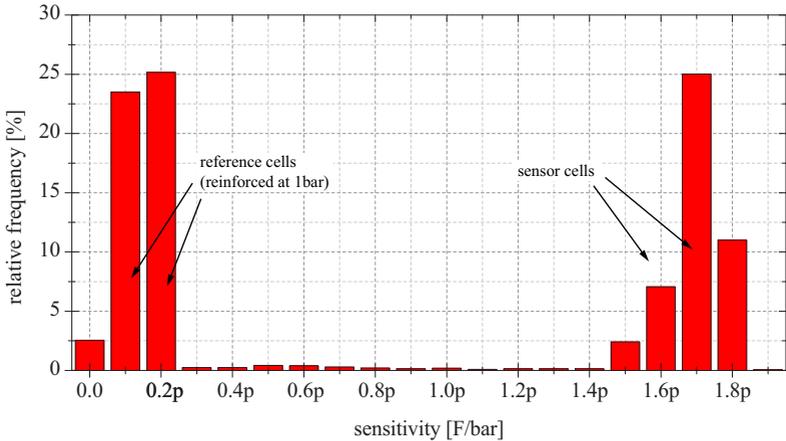
(a) capacitance at three pressure loads (± 50 fF interval width per category)(b) sensitivity at 3.5 bar (± 50 fF interval width per category)

Fig. 3.69: Histograms of touch-mode capacitance and sensitivity of sensors with reference cell. 100 % testing was conducted on wafer-level using a *Süss MicroTec AP200 BlueRay* equipped with a *Süss MicroTec Pressure Probe Module* (50 % sensor and 50 % reference cells). The actual capacitance data was acquired with an *Agilent E4980A Precision LCR meter*. The sensors operated in touch-mode within the applied pressure range.

Test setup: package level

Wafer level testing was followed by a dicing procedure as described in Section 2.4.3 and picking of known good dice. The selected dice were mounted in ceramic packages as depicted in Fig. 3.70(a) and measured in a test setup capable to apply a pressure and temperature load. Testing took place before and after application of environmental and electrical stresses. Un-attached samples were used for testing in cases where humidity or temperature may change the mechanical stress exerted by the package on the die (see Section 3.2.3 for further information on sensor packaging).

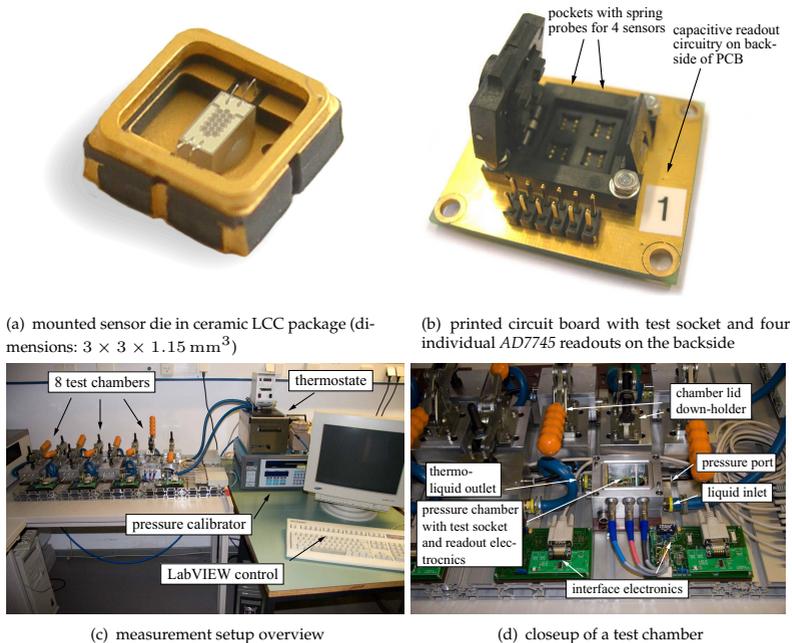


Fig. 3.70: Photographs of the implemented system level test setup.

A measurement setup has been developed to test 32 packaged dice simultaneously. It composes of 8 individual chambers. Each pressure chamber is equipped with a printed circuit board carrying a burn-in socket (see Fig. 3.70(b)). Four individual sensors can be fitted in such a socket, each sensor connected to an individual AD7745 read-out chip located on the back side of the printed circuit board. The wiring of the PCB, including the vias, was done carefully in order to keep the tracks between readout and sensor as short as possible with the goal to render the offset capacitance low and stable. Photographs of the whole setup are presented

test-setup
packaged sensors

in Fig. 3.70(c) and Fig. 3.70(d). Pressure is supplied by a DRUCK DPI510 with an accuracy of $\pm 0.04\%$ of the reading¹⁴ and temperature is controlled by a HAAKE DC10/K15. Each chamber contains a Sensirion SHT15 for the purpose of temperature monitoring with an accuracy of $\pm 1.5^\circ\text{C}$. The developed setup is capable to apply pressure loads between 0.5 bar and 8.0 bar at a temperature ranging between 5°C and 90°C . No measurement system analysis of type 1 (MSA1) [Aut08] was conducted to access the overall accuracy of the whole setup. Such an analysis was solely done for the electrical wafer level setup with the results already presented in Section 3.4.1. However, the setup's offset capacitance was compensated (set to zero) at the beginning of each characterization run and was stable within $\pm 1\text{ fF}$ during the measurement cycle.¹⁵ The accuracy of the AD7745 is specified to $\pm 4\text{ fF}$ [Ana05].

Results: temperature dependency

It will be noted that the sensor characteristics are influenced by temperature in a complex way. Therefore, only qualitative correlations can be given. A number of observations are made when the sensor is operated in **normal-mode** and **temperature T increases** (see Fig. 3.72 and Fig. 3.73(a)):

1. the normal-mode capacitance C_n drops at low pressure ($p \rightarrow 0\text{ bar}$)
2. the touch-down pressure p_t decreases
3. the normal-mode capacitance C_n increases at high pressure ($p \rightarrow p_t$)
4. the sensitivity increases
5. the maximum normal-mode capacitance $C_n^{(\text{max})}$ decreases.

These observations may be caused by either thermally induced changes of the insulation properties or by thermally induced changes of the mechanical transducer layer stress. Both influences will be discussed in the following paragraphs.

Thermally induced dielectric property changes of the implemented $\text{SiN}_{1.04}$ silicon nitride insulation were measured with test structures. These were located on every wafer and are, compared to the sensor, identically processed and have an almost identical layout. They differ only slightly in their geometry having an omitted transducer plate center (see Fig. 3.71(b)). These test structures solely measure the sensor's offset capacitance caused by the membrane support. A capacitance versus temperature plot acquired with such a test structure is presented in Fig. 3.71. It is showing an almost linearly increasing capacitance. This change of low magnitude can be modeled by a relative permittivity of nitride ϵ_{Nit} :

$$\epsilon_{\text{Nit}} = \epsilon_{\text{Nit}_0} [1 + \alpha_\epsilon (T - 20^\circ\text{C})], \quad (3.96)$$

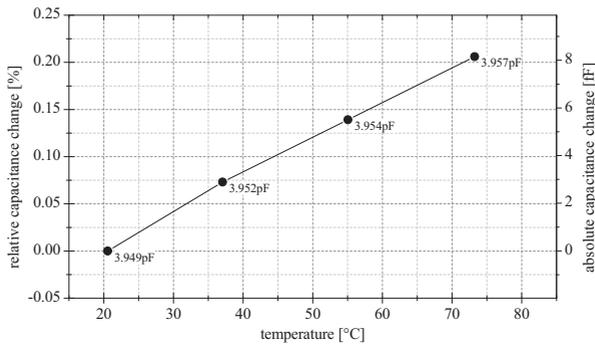
where α_ϵ denotes a temperature coefficient of magnitude $33.76 \times 10^{-6} \text{ 1/K}$ ($\epsilon_{\text{Nit}_0} = 7.4$ for $\text{SiN}_{1.04}$, see Section 3.4.1). The capacitance data was acquired from packaged test

¹⁴ $\pm 0.04\%$ of the reading from 20%–100% full scale and $\pm 0.01\%$ of the full scale value from 0%–20% full scale. This is equivalent to an absolute error of $\pm 3.2\text{ mbar}$ at $p = 8.0\text{ bar}$ and $\pm 0.2\text{ mbar}$ at $p < 2.0\text{ bar}$ (range: 10 bar full scale).

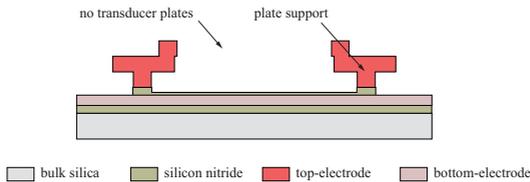
¹⁵ Experiments with different printed circuit board layouts have been run to access their stability [Beh07]. Maximum humidity error: $\pm 0.7\text{ fF}$ at 20°C ; maximum temperature error: $\pm 0.2\text{ fF}$ within the range of 20°C – 85°C ; drift: $< 0.2\text{ fF per day}$; noise: $< \pm 0.5\text{ fF}$.

structures in the setup described above using an *AD7745* circuit. Therefore, it can not be distinguished whether the observed temperature characteristic is caused by an increasing permittivity or by an actually *decreasing resistivity*. Temperature has a twofold action on the insulation resistivity (see Section 2.3.1): firstly the prevailing hopping conduction increases with temperature, secondly the stress within the nitride layer decreases by 0.5 MPa/K increasing in turn the conduction caused by field-enhanced thermal excitation.

No matter which effect caused the dielectric's temperature dependency, its impact on the sensor characteristic is low (approx. $0.15 \text{ fF/}^\circ\text{C}$) and it can be concluded that the sensor is primarily influenced by the thermally induced stress changes within the transducer layer.



(a) relative and absolute capacitance change of the sensor's offset capacitance (sum of the contributions of 16 individual elements)



(b) schematic cross-section of a single array element of the measured test-structure

Fig. 3.71: Temperature dependency of the sensor's offset capacitance. The characteristics were measured with a test-structure having the same geometry as the actual sensor cell. Circular openings in the transducer plate center of the test-structure, as depicted in Fig. 3.71(b), cancel out the transducer plate capacitance and the impact of thermally induced plate deflection.

The decreasing C_n at low pressure and increasing C_n at higher pressures close to p_t (see Fig. 3.72 and Fig. 3.73(a)) can be understood by considering the simulation results presented in Section 3.1.6. It was demonstrated that plates with topography deflect under mechanical stress even if no external pressure load is applied. This initial transducer deflection w_{\min} is proportional to the in-plane membrane stress σ_m

(see Fig. 3.9(a)). It was further discussed, that according to (3.52) p_t decreases if σ_m decreases. Consequently, the plate deflection at a fixed pressure close to p_t increases if σ_m decreases (see Fig. 3.9(b)) rising the transducer's mean sensitivity $\bar{S}^{(\text{normal})}$ as defined by (3.90) at the same time. These effects of in-plane stress on the transducer's deflection are illustrated in Fig. 3.10(d) by comparing the deflection versus pressure curves of a plate with topography at different levels of σ_m . Therefore, the temperature dependent observations one through four given in the itemization at the beginning of this section can be explained by an in-plane stress change caused by temperature:

$$T \uparrow \longrightarrow \sigma_m \downarrow$$

$$\sigma_m \downarrow \longrightarrow C_n \downarrow \Big|_{p=0 \text{ bar}}, p_t \downarrow, C_n \uparrow \Big|_{0 \text{ bar} \ll p < p_t} \longrightarrow \bar{S}^{(\text{normal})} \uparrow.$$

The observed increase of $C_n^{(\text{max})}$, the maximal normal mode capacitance, can not be concluded from the simplified theoretical approach presented in Section 3.1 assuming identical deflection surfaces for plates with and without in-plane stress.¹⁶ Therefore, the touch-down capacitance at $P = 1$, when the plate center just touches the counter electrode insulation, is identical for all stress levels and independent of the actual magnitude of p_t . In reality, the in-plane stress causes an initial deflection and a non zero angle ϑ at the elastic support at $P = 0$. Therefore, the plate surface around the touched center gets closer to the counter electrode with rising in-plane stress and increases the actual magnitude of $C_n^{(\text{max})}$.

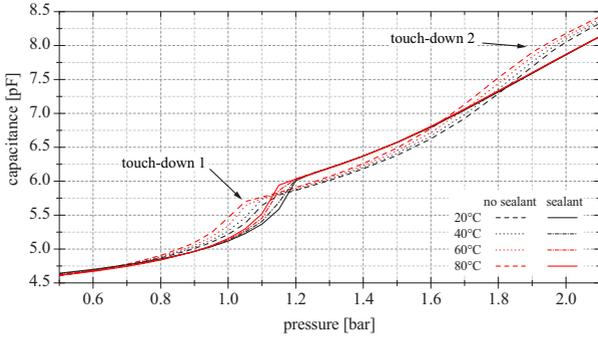
Figure 3.72(b) indicates that the touch-mode characteristics are less affected by temperature changes. This is in agreement with the theoretical finding that the plate deflection in touch-mode is generally less affected by any kind of stress changes. It was demonstrated that the plate deflection in touch-mode is primarily determined by the bending moments (see Section 3.1.8 and Fig. 3.18). This highlights a touch-mode sensor advantage: the robustness to stress deviations either originating from process deviations, packaging influences, or being thermally induced during operation.

Still unknown, the cause for the decrease of in-plane stress at rising temperature although a comparison of two fabricated sensor types provides additional information. These types are fabricated on the same wafer (multi design mask) only differing in their individual sealant layer layout: a standard sensor with a *sealant ring* around the array edge and another having *no sealant* material around the transducer array (see schematic given in Fig. 3.72(c)). The sealant ring covers, if present, the etch-stop recess at the array edge and reinforces mechanically the area around the whole array. Characterization results for both sensor types are presented in Fig. 3.72 and Fig. 3.73. However very similar in their general features, the sensor characteristics and temperature dependencies are greatly influenced by the layout variation at the array edge.¹⁷ The omitted sealant around the array lowers p_t , decreases $C_n^{(\text{max})}$,

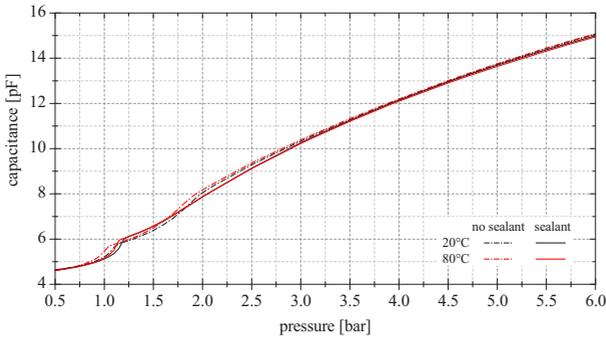
origin of
stress changes

¹⁶ The increase of $C_n^{(\text{max})}$ can not be caused by a change of permittivity ϵ . A larger ϵ would have also increased the touch-mode sensitivity which is not the case (see Fig. 3.72(b)).

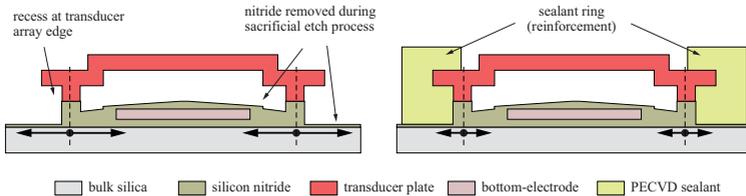
¹⁷ The importance of the area around the transducer array was pointed out before in Section 3.3.4 where the effect of insulation nitride *removal* around the array edge was illustrated in Fig. 3.35.



(a) sensor characteristics (low pressure detail)



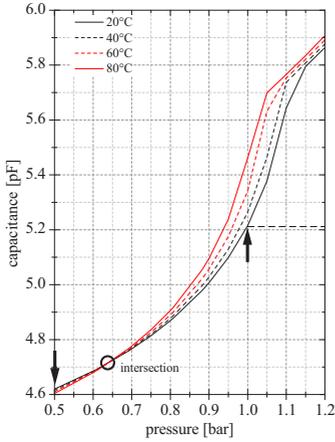
(b) sensor characteristics (full pressure range)



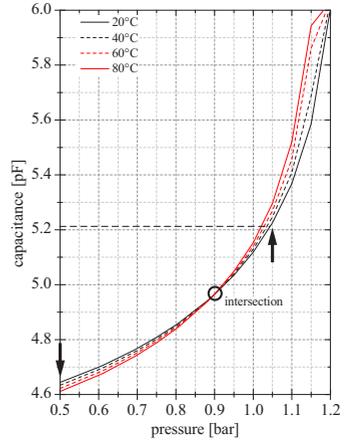
(c) Schematic geometry of the sealant ring around the transducer array. The arrows indicate the support displacement direction and magnitude induced by temperature changes.

Fig. 3.72: Comparison of the sensor's temperature dependent characteristics with and without sealant filled recess around the transducer array. The sealant does not overlap the transducer plates having a geometry as illustrated in Fig. 3.72(c) (see also Fig. 3.36). More details of plot 3.72(a) are presented in Fig. 3.73.

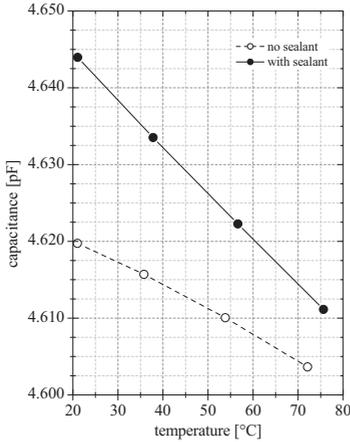
causes a second touch-down, *and* increases the impact of temperature on the sensor.



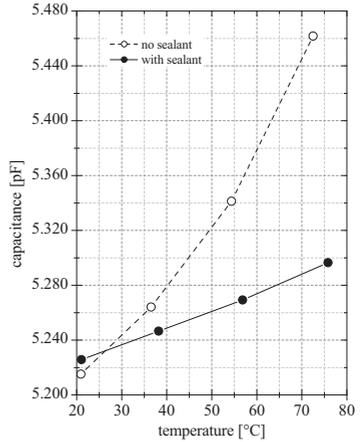
(a) normal operation characteristics without sealant ring around the transducer array



(b) normal operation characteristics with sealant ring around the transducer array



(c) temperature dependency at 0.5 bar



(d) temperature dependency at 1.0 bar (without sealant ring) and 1.05 bar (with sealant ring)

Fig. 3.73: Temperature dependency during normal operation (detail of plot 3.72(a)). The combined action of an offset shift and sensitivity change causes an intersection of the presented characteristics indicated by a black circle in Fig. 3.73(a) and Fig. 3.73(b). The influence of the sealant ring around the transducer array can be noted by comparison. Capacitance versus temperature plots at the locations indicated by the black arrows are presented in Fig. 3.73(c) and Fig. 3.73(d).

It can be concluded that thermally induced stress changes are responsible for the temperature dependency of the sensor which have the highest impact in normal-operation at pressure levels just below p_c . Plates located at the array edge contribute to this change significantly. They show the strongest temperature dependency (they touch at touch-down pressure 1, see Fig. 3.72(a)) because their support is less rigid and larger displacements due to thermal expansion occur. Therefore, the seal ring geometry, material, and stress affects the mechanical homogeneity of the array and the sensor's temperature characteristic. It defines the location of the intersection of the CP-plots (see Fig. 3.73(a) and Fig. 3.73(b)). The higher the stress level within the seal ring the further shifts the intersection towards higher pressures.¹⁸ The negative sign of the thermally induced stress is due to the sum of the individual thermal expansions of the silica bulk, the nitride insulation, and the transducer poly-silicon.

Results: long-term stability

Long-term stability is the biggest concern of sensors acquiring absolute magnitudes of physical quantities. A long-term test was run to obtain information on the stability of the developed sensor. The implemented setup comprises of a sensor sample placed in a ceramic package as depicted in Fig. 3.70(a) (not die-attached) which was mounted on a PCB and interconnected to an AD7745 readout. The ambient pressure was monitored for 100 days and compared to local data provided by the meteorological service DWD [Deu08]. The results are presented in Fig. 3.74.

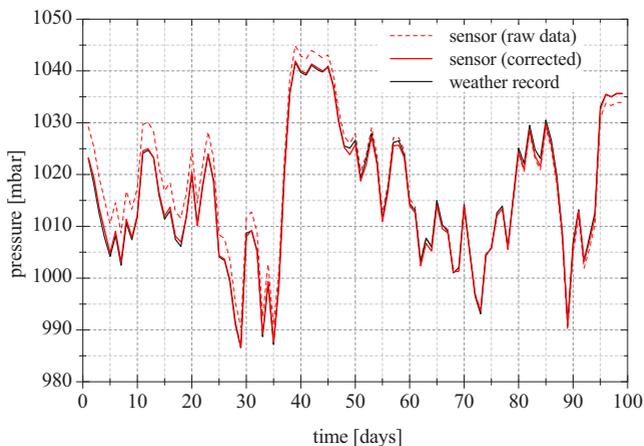


Fig. 3.74: Ambient pressure readings compared to weather service data provided by the DWD [Deu08]. Sensor raw data is only compensated for temperature. The corrected sensor data graph accounts for a constant drift of $-79 \mu\text{bar}/\text{day}$.

¹⁸ The seal ring of the presented two sensors types was made out of a $2.7 \mu\text{m}$ PECVD layer stack having a stress of 81 MPa on fused silica.

A negative drift of the sensor signal must be noted (see sensor raw data in Fig. 3.74). The normal-mode sensor readings fit the official weather record data closely if they are corrected for a drift of $-79 \mu\text{bar}/\text{day}$ or the equivalent of $-54 \text{ aF}/\text{day}$ (at 1 bar and 20°C ambient temperature). The observed drift may either be caused by venting of the sensor cavities, mechanical stress changes due to humidity or creep, dielectric charging, or change of the dielectric insulation properties. The following sections will discuss the characteristics of sensors exerted to different kinds of environmental stresses and will therefore give more information on the probable causes for the observed instability.

Results: hysteresis, pressure cycling

The occurrence of a hysteresis is a major concern of touch-mode pressure sensors (see Section 3.1.8). It is attributed to *Van-der-Waals* forces and is therefore related to the surface properties of the mating faces. Furthermore, surface roughness greatly influences the touch-mode capacitance (see Section 3.1.7 and Fig. 3.19(b)). This section will provide information on the stability of hysteresis and touch-mode capacitance during operation and demonstrates the influence of the sealant material choice.

tested
samples

Sensors from the same fabrication run with identical layouts were either sealed with a LPCVD TEOS layer or a PECVD layer stack. These seal options were chosen because they lead to different mating faces during touch-mode operation. LPCVD sealing causes a deposition of approximately 50 nm oxide on all inner cavity walls (see Section 3.3.5 and Fig. 3.37 through Fig. 3.39) and therefore oxide is in contact to oxide. The PECVD sealant does not penetrate noticeable into the cavities because of the much higher sticking coefficients of the precursors (see Tab. 2.9). Therefore, the poly-silicon transducer plate is in contact to the silicon nitride insulation in touch mode if the cavities are PECVD sealed.

test
conditions

Samples of each sensor type were mounted and characterized in ceramic packages as depicted in Fig. 3.70(a). The operational wear was simulated in a cycling chamber which allowed load alterations from 1 bar to 6 bar and back to 1 bar within 4 sec. This pressure cycling was conducted at ambient temperature with no voltage applied to the devices under test. The resulting hysteresis and touch-mode capacitance change after one to three days of continuous cycling are summarized in Fig. 3.75.

effect on
capacitance

The touch-mode capacitance increases for both sealant materials as can be observed in Fig. 3.75(a). This effect is more pronounced for the LPCVD sealant but saturation occurs for both sealant types. These results can be explained by surface roughness reduction which is either caused by abrasive wear or by surface leveling through plastic deformation of exposed hillocks. The reduced surface roughness in turn increases the capacitance of the interface as defined by (3.63) in both tested cases and raises therefore the touch-mode capacitance.

effect on
hysteresis

The hysteresis of the tested samples developed differently as can be observed in Fig. 3.75(b). The given maximum hysteresis $H^{(\text{max})}$ is the maximum of the hystere-

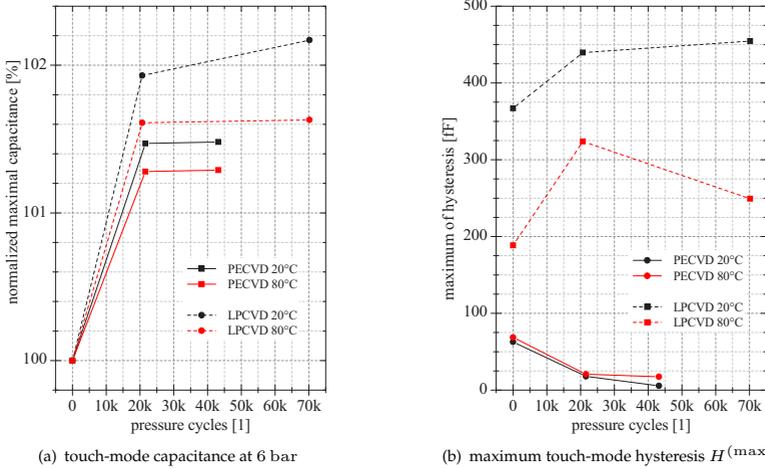


Fig. 3.75: Influence of pressure cycling on sensor hysteresis and touch-mode capacitance. The samples were cycled at ambient temperature between 1 bar and 6 bar (one cycle = 4 sec). The given hysteresis value $H^{(max)}$ is the maximum of H (3.97) within the range of 0 bar–6 bar.

sis

$$H = \left| \frac{C^{(up)} - C^{(down)}}{2} \right| \tag{3.97}$$

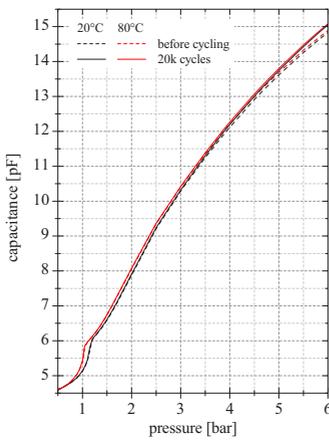
measured within the applied pressure range. Equation (3.97) defines H as the absolute deviation from the mean capacitance reading $C^{(mean)}$

$$C^{(mean)} = \frac{C^{(up)} + C^{(down)}}{2} \tag{3.98}$$

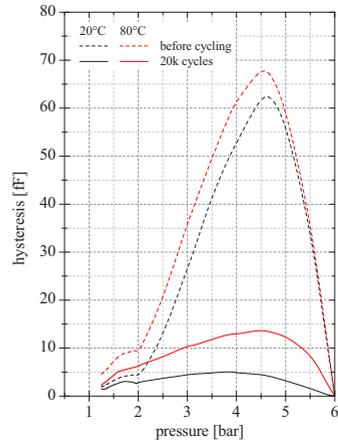
acquired during up- and down-sweep measurements at each tested pressure load. LPCVD sealed sensors show an increasing hysteresis while PECVD sealed samples show the opposite trend. Saturation is clearly observable for the PECVD material but is ambiguous for the case of TEOS. In addition, the magnitude and temperature dependency of the hysteresis is much higher in case of a TEOS seal. These observations may be explained by the softer structure of the TEOS surface ($E=70$ GPa) which might deform plastically. Different the situation in case of PECVD seals, where the more brittle surface of PBOR560 and Nit-Z20 are in contact having *Young's* moduli of 163 GPa and 239 GPa, respectively. Abrasive wear is likely to occur in this case.

More information on operational wear and hysteresis is given in Fig. 3.76. It summarizes characterization results of a PECVD sealed sample with no sealant ring

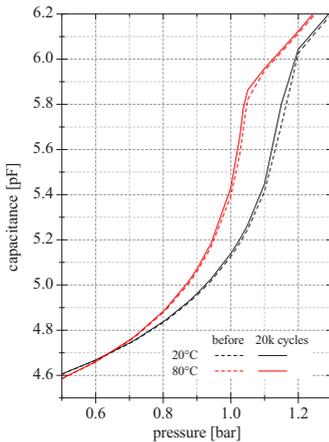
origin of drift



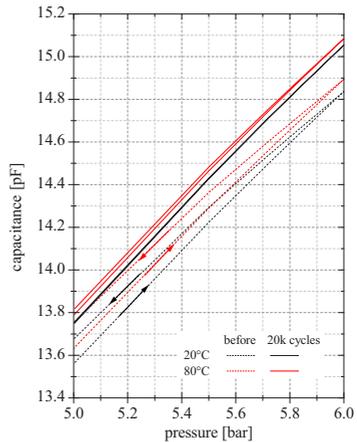
(a) capacitance $C^{(\text{mean})}$ (3.98) before and after pressure cycling



(b) hysteresis H (3.97) before and after pressure cycling



(c) normal-mode capacitance (up **and** down sweep) versus pressure before and after pressure cycling



(d) touch-mode capacitance (up **and** down sweep) versus pressure before and after pressure cycling

Fig. 3.76: Influence of operational wear in touch-mode operation. Depicted are the characteristics of a PECVD sealed sample before and after 24 h of pressure cycling. The applied load was altered at ambient temperature between 1 bar and 6 bar during each pressure cycle.

around the transducer array. It can be noted that the sensor capacitance decreases

immediately after pressure reduction (see Fig. 3.76(d)) but with a down-sweep capacitance $C^{(\text{down})}$ which is always higher than the up-sweep value $C^{(\text{up})}$. This finding, the fact that the magnitude of H is independent on the sweep speed, and the occurrence of a return pressure independent location of $H^{(\text{max})}$ supports the interpretation of *Van-der-Waals* forces as cause for the hysteresis. The down-sweep capacitance is always higher because bonded surface atoms around the circumference of the touched area must be broken with energy provided by bending moments acting in the transducer plate. A hysteresis maximum must exist because the required release work is a function of the length $2\pi r_t$, which is proportional to touch-radius while the bending moments depend non-linearly on r_t .¹⁹

Figure 3.76(c) indicates that the surface roughness change due to sensor wear also has a minor effect on the magnitude of the normal-mode capacitance as discussed in Section 3.1.8 ($C_n^{(\text{max})}$ increases). However, no hysteresis can be observed after return from touch-down within the measurement error of the setup (up- and down-sweep are both depicted in Fig. 3.76(c)).

Results: humidity, high temperature stress

The influence of high temperature and humidity on the sensor stability was tested. The stress conditions were chosen on the basis of the two most general reliability tests (see Tab. 3.3), i.e. high temperature storage life and steady state temperature humidity bias life. No die-attach was implemented to cancel out the possible influence of packaging stress changes during environmental stress application. Sensors with and sensor without sealant ring, were packaged in ceramic housings and measured before and after stress application.

Characterization results demonstrating the influence of 4 h at 150 °C are summarized in Fig. 3.77. Results illustrating the impact of 168 h at 85 °C/85 %RH are given in Fig. 3.78. The following procedure was maintained during all characterization runs:

- low-temperature stabilization at 20 °C
- data acquisition during pressure up- and down-sweep
- high-temperature stabilization at 80 °C
- data acquisition during pressure up- and down-sweep.

Depicted are $C^{(\text{up})}$ versus pressure plots before and after stress application and the respective deviation of pressure up- and down-sweep. The down-sweep deviation gives information on the *stability of the measured shift*.

Consistent results are obtained for thermal stressing. Both sensor types show a positive and stable capacitance shift indicative for a stress relieve within the transducer layer (see Fig. 3.77). The positive capacitance shift cancels out sensor cavity venting as cause for the drift. Distinct peaks can be observed in vicinity of the touch-down pressures at 1 bar and 2 bar where the sensor has its maximum sensitivity. The stability under thermal stress can be improved notably by omitting the PECVD

test
conditions

thermal
stress

¹⁹ The local minima at approx. 2 bar in Fig. 3.76(b) is caused by the second touch-down of the inner transducer plates of the PECVD sealed sample with no sealant ring around the transducer array (first touch-down at approximately 1 bar, see explanation in previous section and Fig. 3.72(a)).

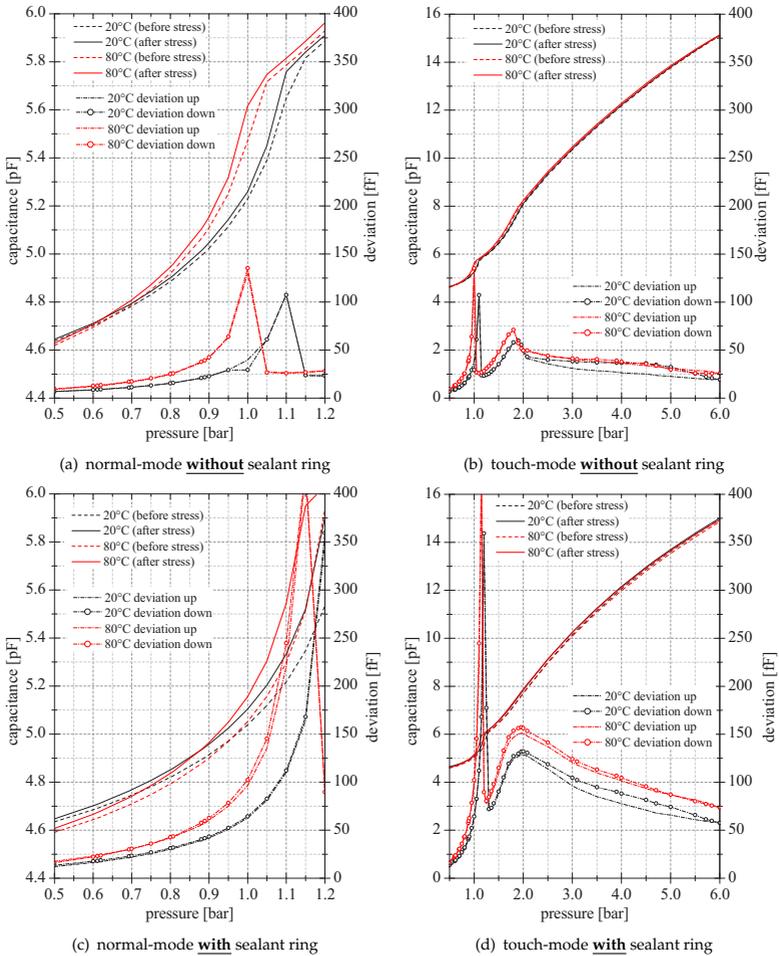


Fig. 3.77: Influence of steady state high temperature stress on the sensor characteristics. The data compares the sensor output of dice with and without sealant ring around the transducer array before and after application of a 150 °C stress for 4 h.

material at the array edge. However, the sample without sealant still drifts with unknown cause.²⁰ From the measurements can be concluded that thermal stressing at

²⁰ The measurement setup, including electronics and pressure controller, did not introduce an error. Their

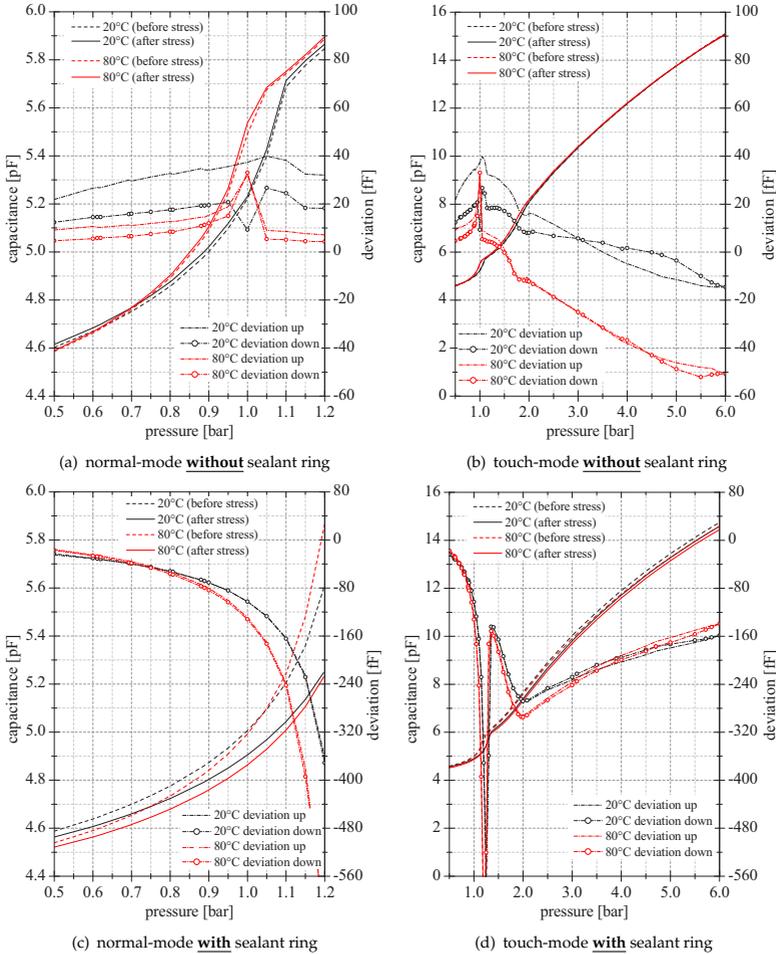


Fig. 3.78: Influence of steady state temperature and humidity stress on the sensor characteristics. The data compares the sensor output of dice with and without sealant ring around the transducer array before and after application of a 85 °C/85 %RH stress for 168 h.

150 °C leads to a relieve of the transducer’s in-plane stress σ_m .

The measurement results depicted in Fig. 3.78, though from a single samples, rep-

stability was monitored by unstressed reference sensors which were measured in parallel.

humidity
stress

resent the typical influence of humidity on the sensor characteristics. Again, the samples with PECVD sealant around the array shift stronger than the samples without. The observed drift of the sealant sample has a negative sign, opposite to the shift caused by thermal stressing (compare Fig. 3.77(d) and Fig. 3.78(d)). This suggests humidity diffusion as cause of mechanical stress changes. Such an explanation is probable for the case of a present PECVD seal ring. However, the results obtained from samples without sealant ring cast some doubt on this simple interpretation because a positive shift results for normal and a negative for touch operation. Additional effects may influence the readings such as humidity in the etch stop recess or parasitic surface conduction.²¹ These explanation approaches would be in agreement with the constantly decreasing normal-mode shift during the characterization run starting with a 20 °C up- and ending with a 80 °C down-sweep (see Fig. 3.78(a)). However, the high-temperature touch-mode shift is stable and negative. Therefore, the conclusion of humidity increasing the mechanical in-plane stress is likely.

origin
of drift

Which part of the transducer changes its mechanical properties is unsure and must be further investigated. The area close to the array edge is shown to be very important and all kind of sealant around the array increases the risk of drift (see Section 2.2.6). But only LPCVD silicon nitride, poly-silicon, and aluminum remains on the surface of the sealant ring less sample. Amongst these materials just aluminum can be expected to show morphology changes at temperatures below 200 °C (see Fig. 2.34). Creep of the stressed silicon nitride or of the fused silica bulk may take place. However, this is according to the discussion presented in Section 2.2.2 not expected because the stress level of the nitride insulation layer is roughly $\sigma = 1.2$ GPa, a magnitude of about 17 % of its fracture strength (>6.7 GPa, $\text{SiN}_{1.04}$ [Chu04]) and the magnitude of stress within the silica bulk is small (<1 MPa see Section B.1.4 and Section 2.2.2). Humidity or oxygen may penetrate the transducer material and change its intrinsic stress. In the other hand, wafer-level bow measurements of PBOR560 layers prior to and after humidity stress did not reveal a stress change. Finally, humidity uptake by the silica bulk itself and subsequent deformation could take place but was not evaluated.

Results: bias voltage stress

Drift due to dielectric charging is, besides hysteresis and wear, a potential threat during touch-mode operation. This short section gives for this reason CP-plots demonstrating the influence of electrical stress. A 3 V bias was applied for 168 h at ambient temperature and a pressure of 6 bar to the device under test (positive terminal connected to the top-electrode). Already about 50 % of the bottom-electrode is in contact to the transducer plate at this pressure level (see Fig. 3.16). PECVD sealed samples were selected for testing to ensure that the poly-silicon transducer is in direct contact to the low-stress silicon nitride insulated counter-electrode with no additional sealant material between the mating faces. The chosen voltage level stresses the insulation of the sample with an electric field of $38 \text{ MV/m} - 55 \text{ MV/m}$ (variation from

²¹ Parasitic conduction increases the capacitance reading acquired with an AD7745. Already a parasitic parallel resistance R_p of $225 \text{ G}\Omega$ introduces a measurement error of $+40 \text{ fF}$ magnitude ($\Delta C = 9 \text{ mF}/\Omega$, can be concluded from [Ana05, p. 9]).

touch-area center to the circumference), a magnitude well below the critical level of 170 MV/m calculated in Section 2.3.1. Therefore, thermally excited hopping conduction according to (2.32) is expected to dominate the charge transport within the nitride insulation.

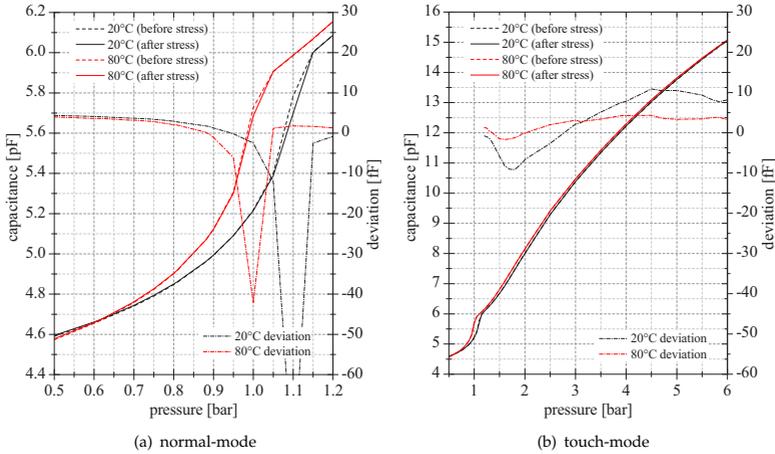


Fig. 3.79: Influence of continuous bias voltage stress on the sensor characteristics. The given readings compare the sensor output before and after application of a 3 V bias for 168 h at ambient temperature.

Fig. 3.79 compares $C^{(\text{mean})}$ data acquired before and after bias voltage stress application. The measurement cycle started at 0.5 bar and 20 °C and ended at the same pressure level at 80 °C. The touch-mode capacitance is expected to be most significantly influenced by the stress. This is not the case and distinct deviations can only be observed in vicinity of the touch-points at 1 bar and 2 bar. The deviation changes its sign and makes therefore other influences more likely than dielectric charging. The presented results are based on two measurements which were conducted within the time of 20 days. Therefore, considering the results given in Fig. 3.74, a drift of approximately -1 fF must be expected during 20 days at 1 bar which is close to the -2 fF observable in Fig. 3.79 after bias stress. Especially, the touch-mode deviation of the 80 °C characteristic at the end of the characterization run is within the expected error of the setup. Moreover, the offset capacitance at 0.5 bar, which is caused by the nitride insulation at the transducer plate support, deviates only within the setup’s error. Therefore it can be concluded that the implemented $\text{SiN}_{1.04}$ insulation with a thickness of 90 nm after deposition and between 85 nm – 50 nm after sacrificial etch (variation from bottom-electrode center to the electrode edge) is at least suitable for operation voltages up to 3 V.

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*You certainly usually find something if you look,
but it is not always quite the something you were after.*

J.R.R. Tolkien

4

Summary and Conclusion

AUTOMOTIVE sensor applications were the MEMS promoters of the early years. Today, still the largest number of sensors are fabricated for the automotive and industrial market. In future, consumer electronics are expected to become the driver of many new applications. The number of required MEMS components will increase enormously approaching hundreds of millions or even billions of devices. The prospect of very large component counts and a high turnover is motivation for many companies to adopt existing technologies or develop completely new approaches to meet the demands of the consumer electronics markets: small size and low-costs. Successful commercial examples can already be found, most of them incorporate inertial sensors:

market
demands

- Tilt (acceleration) sensors are employed to adjust a display image according to the actual device orientation.
- Acceleration sensors are incorporated in hard disc drives, laptops, or camcorders to detect the event of free fall and prevent data loss.
- Six-axis inertial measurement units are integrated in gesture based user interfaces. The *Wii* playstation from *Nintendo* e.g. incorporates MEMS accelerometers and angular rate sensors.
- Accelerometers and gyroscopes are used for image stabilization in camcorders and digital cameras.
- The demand for location based services is expected to grow requiring inertial sensors in cell phones, PDAs, or navigation devices. Accelerometers and gyroscopes are used as pedometer, are incorporated to improve the dead-reckoning capabilities, or to enable pinpointing with the navigation device.

In addition, there are also non-inertial MEMS sensors for high volume products:

- Capacitive microphones are already incorporated in cell phones and will continue to replace electret microphones.
- Absolute pressure sensors will add functionality to cell phones. They provide either barometric pressure data for an integrated weather station or height data for location based services.

- MEMS pressure sensors will also keep on spreading into a variety of household appliances and sports equipment.
- The market of highly miniaturized pressure sensors for tire pressure monitoring systems is expected to keep on growing over the next years.

objectives
of this work

The presented work focused on the development of a micromachined pressure sensor. It was the objective to address the future key requirements, die size and system cost, by a new micromachining process on fused silica. Surface micromachining reduces in first place the die dimension and costs. Moreover, the small surface micromachined dice with miniaturized transducer structures on a rigid bulk simplify the packaging, require smaller and thinner housings, and reduce the system integration costs. The special substrate material was chosen to improve the difficult stress control of the transducer layer which is generally associated with the surface micromachining approach. An improved stress control raises the fabrication yield and reduces again the device costs. The high purity of the silica substrate material increases its softening point to 1600 °C enabling the integration of high temperature LPCVD film formations into transducer processes. These depositions are required to achieve high homogeneities which are mandatory to raise the die yield. Additionally, the non-conductive substrate reduces the sensor offset capacitance and therefore increases the sensor's relative sensitivity with a positive impact on the readout design. The suggested process results in small pressure sensitive devices with two floating terminals which can be integrated into a circuitry like any other non-polar capacitor.

4.1 Processing on fused silica

selection of
fused silica

This work demonstrated successfully the feasibility of a surface micromachining technology on non-conductive fused silica substrates. The special material choice was motivated in Section 2.1. In contrast to *Pyrex*[®], fused silica is stable at process temperatures up to 800 °C and its low TEC of $0.5 \times 10^{-6} \text{ K}^{-1}$, well below the silicon TEC of $2.6 \times 10^{-6} \text{ K}^{-1}$, raises the stress of many LPCVD deposits to tensile levels. Other non-conductive substrate alternatives, like mono-crystalline quartz or sapphire, were excluded for their high TECs rendering most LPCVD layers compressive (see Tab. 2.2 for a summary of substrate material properties).

thin-film
deposition

Thin-film deposition is a key technology for surface micromachining process flows and was discussed in Section 2.3.1 for the relevant layers such as silicon oxides, silicon nitrides, and un-doped as well as in situ boron-doped poly-silicon. Measurement of mechanical film properties such as stress and modulus was addressed. A useful and simple means to determine the biaxial modulus of thin-films by means of co-deposition and curvature measurements on silicon and fused silica was presented in Section 2.2.3 together with the actual moduli of all relevant films for this work.

stress and moduli
measurement

Silica substrates cause a general increase of the thermal stress component of all commonly used LPCVD films. As benefit, well controllable asymptotic annealing of fully crystalline as-deposited poly-silicon layers to low tensile stress levels becomes feasible as discussed in Section 2.2.5. This section presented a comprehensive

stress on
fused silica

comparison of film stress on silica to the stress on silicon. It was found that the total stress of SiN_x increases by roughly 800 MPa and that poly-silicon becomes about 350 MPa more tensile. The generally high stress levels on fused silica were shown to pose strong demands on the overall process flow: layer thicknesses are limited, low-stress silicon nitrides must be adopted instead of stoichiometric Si_3N_4 , wet-chemical patterning is mandatory in most cases, and lithography is rendered more demanding because of stress induced alignment key shifts.

Fused silica substrates were suggested for high temperature processes. The amorphous structure of this material makes a discussion of viscous deformation necessary which was given in Section 2.2.2. It was shown that long-term processes up to 12 h at 800 °C reduce e.g. the stress of $\text{SiN}_{1.04}$ low-stress nitride by about 1 % due to viscous relaxation of the substrate. For the same reason, the stress of in situ boron-doped poly-silicon, the transducer layer material PBOR560, increased by roughly 5 %. It was concluded that 800 °C is the upper thermal process limit for the suggested fused silica substrate. On the other hand, fused silica was demonstrated to be thermally stable under normal operation conditions below 200 °C. The presented calculation of the viscous time constant for fused silica indicated an increase of 30 orders of magnitude for a temperature drop from 800 °C to 200 °C (see Tab. 2.3 and Tab. 2.4).

Low-stress silicon nitride and in situ boron-doped poly-silicon were the two most important structural layers of the presented sensor. These films were therefore in depth discussed in Section 2.3.1. It was concluded that the increased mechanical stress on silica renders the dc insulation properties of the low-stress silicon nitride comparable to the quality of stoichiometric nitride deposited on silicon. The deposition of in situ boron-doped poly was discussed and demonstrated to be difficult to control. It was concluded that the resulting deposition rate and layer structure is very susceptible to the boron and hydrogen concentration within the reactor. This special poly-silicon was chosen as material for both electrodes of the presented sensor because of its very fine grained structure being thermally and mechanically very stable. It was demonstrated that these fully crystalline as-deposited films can be asymptotically annealed in well controllable long-term processes to the target stress level by means of temperature adjustment.

The high selectivities of wet-chemical processes put them in focus of Section 2.3.3. A special low-temperature etch-process was presented to overcome the challenge of removing a LPCVD oxide sacrificial layer on top of an oxide substrate which is only protected by a very thin silicon nitride layer. The developed process offers a selectivity of 1.6×10^3 for as-deposited TEOS on a $\text{SiN}_{1.04}$ passivation. The selectivity was shown to increase above 1.1×10^4 for $\text{SiN}_{0.61}$. Tight etch rate control of the wet-chemical processes were a concern because these processes were used to define the transducer's geometry. Special etch-mixtures to pattern deposited oxides and poly-silicon were developed guaranteeing reproducible and well controllable low etch rates. The importance of wet-etching is stressed by the fact that 3/4 of the layers in the presented pressure sensor process are patterned in wet-chemical batch processes leading to low overall processing costs.

Bulk micromachining of fused silica was only briefly addressed in Section 2.4. General aspects of etching the silica bulk by means of DRIE and hydrofluoric acid

thermal stability
of fused silica

low-stress nitride

in situ boron-
doped poly

wet-etching

selectivity

wet bulk etching

dry bulk etching

wafer thinning

were discussed highlighting the challenge to implement proper masks for the required long etch processes. 200 μm cavities were wet-etched by means of hydrofluoric acid with poly-silicon as well as nitride masks. A nickel mask was tested for DRIE of narrow openings but only small rates were achieved and mask material re-deposition was observed causing rough sidewalls. Wet-chemical and mechanical wafer thinning was evaluated demonstrating the feasibility of grinding and polishing the silica wafers after the final transducer fabrication step. Wet-chemical thinning was tested but was found to be time consuming and not applicable in most cases.

4.2 Theoretical sensor design

dimensionless analytical model

topography & stress

touch-radius vs pressure

normal- & touch-mode capacitance

dielectric & counter-electrode radius

general transducer properties

A mechanical and electrical model of a capacitive pressure transducer with a circular plate was presented in Section 3.1. The well known formulas were normalized and presented in a dimensionless form specially adapted for surface micromachined plates. It was shown in Section 3.1.6 that an analytic approximation for these type of MEMS transducers must incorporate the influence of topography, fabrication related stress, and membrane stress due to large deflections in order to be meaningful. The presented approach incorporated these influences analytically by simply re-scaling the dimensionless load. Two approximations for the normal operation deflection were presented: the first, keeping the linear relation of deflection and applied pressure from small-deflection theory but being accurate at plate touch-down, the second, non-linear and exact at plate touch-down.

A new and general way to calculate the touch-down radius of the transducer plate as function of applied load was presented in Section 3.1.4. The given approximation of this relation was found by normalization and is general for all circular plates under uniform pressure load. It was used in this work to calculate the bending moments, maximum pressure, sensitivity, and capacitance in touch-mode operation.

The normal- and touch-mode capacitance was calculated in Section 3.1.7 based on the derived analytic approximations for the transducer plate deflection. The influence of a counter-electrode insulation consisting of a dielectric layer stack was incorporated in a general form. It was observed during prototype fabrication, that not only the insulation material covering the counter-electrode, but also unintentionally deposited sealant material had a non-negligible impact on the touch-mode capacitance. Furthermore, it was found impossible to fit the characterization results to the theoretical model unless surface roughness was incorporated in the formulas which appeared to have a strong influence on the resulting touch-mode capacitance. In addition, the commonly smaller diameter of the counter-electrode, and a concentrically varying insulation thickness were integrated in the presented formulas. This concentrical insulation thickness variation, caused by wet-chemical attack during sacrificial layer removal, lead to linearization of the touch-mode characteristics.

All analytic results were summarized in Fig. 3.15. It is a general capacitance versus pressure plot for circular plate type pressure sensors relating the marked operation points: minimum-, touch-down-, and maximum capacitance, to the design parameters: transducer plate dimension, dielectric insulation, and counter-electrode radius. The distinct features of normal- and touch-mode operation of capacitive pressure

sensors were summarized in Section 3.1.8. The discussion highlighted that normal-mode sensors are greatly influenced by mechanical stress either caused by the transducer fabrication, the package, or by large deflections. This was demonstrated to be not the case for touch-mode sensors where stress changes mainly cause offset shifts. Instead, their properties depend critically on the implemented insulation. It was illustrated that touch-mode sensors have the potential to be highly sensitive over a wide pressure range, but it was shown that optimization of this unique touch-mode feature implies the implementation of thin dielectric insulations being prone to parasitic conduction and rendering the process challenging. Additionally, wear of the insulation and a hysteresis due to surface forces were identified as general concern of touch-mode transducers.

normal- vs
touch-mode

4.3 Prototype fabrication and modeling

A highly miniaturized surface micromachined capacitive pressure sensor was presented. General design aspects were discussed in Section 3.2.1 focusing on the arrangement of individual transducer cells, on the package and interconnection concept, as well as on reference cell concepts. It was concluded that the aggregation of individual transducers plates in a continuous mechanical array down-sizes the transducer dimensions but leads to differing mechanical properties of these plates. Some readout concepts require a reference capacitor. Possible implementations were discussed in Section 3.2.2. A new approach for a reference cell with transducer plates reinforced by means of electroplating was suggested and prototypes fabricated (see Section 3.3.7). These cells were shown to provide a reference to ambient pressure (the pressure at which the electroplating process was run). The proposed reference cells are identically processed as the actual sensor cells having the same geometry and dielectric. The special concept was intended for touch-mode sensors allowing the fabrication of a reference at a pressure load beyond plate touch-down. Reinforced in touch-down, the references account for all sensor process deviations commonly leading to a shift of the touch-down pressure. Furthermore, they incorporate the actual dielectric insulation stack of the sensor after sacrificial etching and hermetic sealing, including partially removed dielectric, unintentionally deposited sealant, and surface roughness.

concept

array geometry

reference cells

The conceptual design was concluded with a brief discussion on the pressure sensor system integration given in Section 3.2.3. A standard packaging procedure using a back side die-attach and wire bonds was favored as it provides the best reliability and stress insulation of the sensor die. Through substrate vias were motivated potentially lowering the overall package height which is considered to become increasingly important in future. Concepts for a via through fused silica were presented as well as the technological basis for their fabrication (see Section 3.3.8).

system
integration

through
substrate via

Surface micromachining on fused silica was proven to be feasible by implementation of a capacitive pressure sensor process which was described in Section 3.3. As could be expected from the discussion of Section 2.2.5, the commonly high stress levels of deposits on this special substrate are a general challenge. These lead to the consequence of film thickness limits and to the requirement of highly selective etch procedures. Sealant material choice and deposition was found to be critical. It

pressure sensor
process

penetrated the sensor cavities, changed the mechanical transducer properties, influenced the touch-mode capacitance, and affected the hysteresis of the sensor greatly. In addition, sealant material and the metallization are the final layers in the process sequence and can lead to sensor instability if these are not insensitive to humidity and temperature stress (see Section 3.4.5).

The fabricated prototypes were characterized on wafer and package level. Reproducible and precise asymptotic transducer layer stress adjustment, as demonstrated in Fig. 2.33, has been achieved utilizing the high thermal offset stress on silica. This was proven by means of 100 % wafer level sensor mapping under pressure load application with the results presented in Section 3.4.5. These demonstrate a high fabrication yield and a low spread of sensitivity and offset capacitance in normal- and touch-mode operation (see Fig. 3.67 and Fig. 3.68). In addition the feasibility of the suggested reference cell concept based on transducers arrays reinforced by means of electro plating was demonstrated (see Fig. 3.69).

The goal to develop a pressure sensor which could be treated as a two terminal floating capacitance during system design was met. A discrete measurement system consisting of a commercially available AD7745 and a pressure sensor in a ceramic housing mounted on PCB was sufficiently sensitive to monitor the atmospheric pressure (see Fig. 3.74). However, the accuracy of the system is generally limited by drift and by hysteresis in touch-mode operation. A test setup for simultaneous testing of packaged dice within the range of 0.5 bar – 8 bar and 5 °C – 90 °C was implemented to further investigate the cause of instability and hysteresis. Package level testing presented in Section 3.4.5 revealed a high temperature coefficient of the sensor. Mechanical stress changes were demonstrated to be related to the sensor's temperature characteristic. Implemented design variations with differing sealant layer layouts indicated that the area around the transducer array had a critical action. It was influencing the sensor's temperature coefficients, the overall shape of the CP-curve and its stability under environmental stress. As discussed above, the stress of un-patterned transducer layers can be adjusted precisely during sensor fabrication, but observations indicated that the actual stress of a local individual transducer plate is affected by the stress of all layers in its vicinity. The distance over which a local structure under stress influences surrounding features is determined by the rigidity of the bulk. The shear modulus of silicon is about 2.5 times the modulus of silica. Therefore, it can be concluded that stress of local structures on silica affects neighboring features stronger and over greater distances. The implications for the presented sensor are threefold and supported by the measurement data summarized in Section 3.4.5:

- The relative softness of the substrate increases the effect of any mechanical stress changes due to environmental stress. Layers exposed to the environment are of special concern and need to be tested for their stability under the expected operation conditions. Geometry and location of patterned structures must be carefully considered.
- Center cells of the transducer array do not deflect as their neighbor plates at the array edge. The more rigid the layer stack around the transducer array is designed the more homogeneous become the individual plates of the array in their mechanical characteristic.

transducer layer
stress adjustment

wafer level
testing

package level
testing

temperature
sensitivity

softness of
silica

- Packaging stress introduced from the back side of the die extends further into the bulk. Experiments and simulations with different die-attaches indicated that the influence of a back side die-attach is, however low in magnitude, higher than on silicon [Her07].

Package level testing indicated that the presented sensor can be operated at 3 V in touch-mode without drift due to dielectric charging but temperature stress and combined temperature/humidity load lead to drift of the output signal.

The hysteresis as general problem of touch-mode sensing could be greatly reduced by sealant material choice as discussed in Section 3.4.5. It was demonstrated that a hysteresis smaller 10 mbar within a pressure range up to 6 bar can be achieved with poly-silicon and silicon nitride as mating faces. The observations indicated that *Van-der-Waals* forces are cause for the hysteresis.

dielectric
charging

hysteresis

4.4 Challenges and outlook

Special applications can necessitate the choice of fused silica as substrate material if the bulk's special electrical, optical, or thermal properties can be utilized very beneficially. These features can justify the additional work caused by substrate related process developments as for the present case. A complex surface micromachining process has been demonstrated to be feasible on silica. The initial objectives summarized in Tab. 1.5 were successfully addressed but it became apparent that the actual challenge is the achievement of a high sensor stability. It was noted that the relative softness of the silica in comparison to silicon must be taken into consideration as it promotes stability issues. A high thermal stress level of deposits combined with the bulk's softness and amorphous structure generally increases the risk of drift for mechanical transducers. This general substrate related concern must be expected to require engineering work.

The presented thesis provides the means for a theoretical and practical pressure sensor development on silica. It shows the benefits and limitations of the less common touch-mode operation which is expected to be less sensitive to packaging influences. This feature still needs to be demonstrated and further challenges may be identified by the development of a package for the presented element. Initial tests indicated that protective coatings have a positive action on the sensor's stability. Therefore proper packaging may reduce the observed drifts. However, more thoroughly testing of the mechanical long-term stability of all implemented layers including the insulation and its interface to the poly-silicon must be conducted. Clarification of the root cause of the observed instability is required which may be either stress relaxation or diffusion of vapor and other gases. A possible contribution of the transducer or bulk material itself to the sensor drift could not be ruled out in the present work.

One of the most critical steps in the presented process flow is the deposition of the in situ boron-doped transducer layer. Its stress can be adjusted with the suggested procedure but thickness reproducibility and homogeneity over the reactor load remains an issue. As discussed in this work, better process stability is expected if the precursor gas mixture is changed from B_2H_6/SiH_4 to B_2H_6/H_2 . A positive

impact on the sensor characteristics could have a silicide covered bottom electrode. Initial tests showed that stress control will be an issue for such layers on fused silica but the sensitivity of the element towards the readout frequency can be expected to decrease.

References

- [Her07] T. Hertzberg: *Numerische Untersuchungen und Experimente zur Beurteilung thermo-mechanischer Einflüsse der Sensor/Gehäuse-Verbindung auf das Verhalten eines oberflächen-mikromechanischen kapazitiven Drucksensors*; Student research project report; University of Bremen; 2007.
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*There is nothing more deceptive
than an obvious fact.*

Sir Arthur Conan Doyle



Introduction

A.1 Physical constants

Table A.1: Summary of physical constants.

symbol	value	unit	quantity
g	9.82	m/s^2	acceleration of gravity
R^*	8.31433	$\text{J}/(\text{K mol})$	universal gas constant
N_A	$6.02214179 \times 10^{23}$	$1/\text{mol}$	<i>Avogadro</i> constant
q	1.60218×10^{-19}	$\text{C} = \text{A s}$	elementary charge
eV	1.60218×10^{-19}	J	electron volt
k	1.38066×10^{-23}	$\text{J}/\text{K} = \text{Ws}/\text{K} = \text{VA s}/\text{K}$	<i>Boltzmann's</i> constant
m_0	9.1095×10^{-31}	kg	electron rest mass
ϵ_0	8.85418×10^{-12}	$\text{F}/\text{m} = \text{C}/(\text{V m})$	permittivity of free space
ϵ_{cSi}	11.9	1	permittivity of silicon

A.2 The barometric formula

The following section will give a hydrostatic derivation of the barometric formula¹ that relates pressure to altitude. The formula is sometimes also called *Laplace's formula* because he was the first to give it explicitly for an isothermal atmosphere. The assumption of a homogenous temperature holds reasonably well (with an error less than 5 % for altitudes up to 6 km). A linear temperature gradient can be integrated in the formula with little more effort and is done below in Section A.2.1. The obtained expression is a good approximation of the troposphere and together with average

¹ A good summary on the history of the barometric formula together with alternative kinetic and stochastic derivations can be found in [BS97].

values for ground pressure, temperature and temperature gradient it is used as a standard model since 1976 (see Tab. A.2).

Consider a small cylindrical volume with the base A containing the mass dm of air. The equilibrium of forces gives

$$Ap - g dm = Ap + A dp$$

with p and g denoting pressure and acceleration of gravity. The weight of the enclosed air is supported by a small change in pressure dp . Due to symmetry, the force acting on the lateral area can be omitted. Expressing the mass of the entrapped air in terms of density $dm = A\rho_{\text{air}} dh$ and geometry yields

$$\frac{dp}{dh} = -\rho_{\text{air}} g.$$

The perfect gas law (1.1) provides an approximative expression for the air density in dependence of temperature T and pressure

$$\rho_{\text{air}} = \frac{pM}{R^*T}$$

which can be pasted in (R^* , M are the universal gas constant and the molar mass of air, respectively). By separation of the variables, an integrable differential equation is found local pressure in a gas column exposed to gravitation and temperature:

$$\frac{dp}{p} = -\frac{Mg}{R^*T} dh. \quad (\text{A.1})$$

An integration yields the barometric formula as given by *René de Laplace*:

$$p(h) = p_0 \exp \left[-\frac{Mgh}{R^*T} \right]$$

or with molecular mass m_u and *Boltzmann* constant k

$$p(h) = p_0 \exp \left[-\frac{m_u gh}{kT} \right].$$

A.2.1 Atmosphere with a linear temperature gradient

The troposphere extending up to 11 km can be well modeled by assuming a linear vertical temperature gradient: $T(h) = T_0 + T_{,h}(h - h_0)$ where $T_{,h}$ denotes a partial derivative of T with respect to h . The declining temperature with rising altitude is due to the fact that air is heated by the surface of the earth. Nevertheless, the temperature gradient is smaller than it may be expected. This is because convection occurs and warm surface air is transported upwards. Local weather phenomena

like inversion layers and cold or warm fronts² do also change the mean gradient of $T_{,h} = -0.65 \text{ K}/100 \text{ m}$.

The differential equation A.1 can be integrated by neglecting small changes in g due to altitude

$$\int_{p_0}^p \frac{dp}{p} = -\frac{Mg}{R^*} \int_{h_0}^h \frac{dh}{T_0 + T_{,h}(h - h_0)}$$

yielding the barometric formula for the pressure of an atmosphere with a linear temperature gradient dependent

$$p(h) = p_0 \left[1 + \frac{T_{,h}(h - h_0)}{T_0} \right]^{-\frac{Mg}{R^* T_{,h}}}. \quad (\text{A.2})$$

Solving for the altitude gives the height as a function of pressure (with $h_0 = 0$ at sea level)

$$h(p) = -\frac{T_0}{T_{,h}} \left[1 - \left(\frac{p}{p_0} \right)^{-\frac{R^* T_{,h}}{Mg}} \right]. \quad (\text{A.3})$$

A.2.2 The Standard Atmosphere

The *Standard Atmosphere* is a hypothetical vertical distribution of atmospheric properties. It is, by international agreement, an approximate representative of year-round, mid-latitude conditions. The model was established by the work of the U.S. Committee on Extension to the *Standard Atmosphere* (COESA) for the first time in 1953 and the current version later in 1976. The *Standard Atmosphere* consists of seven atmospheric layers from sea level to 1000 km and gives the atmospheric properties according to rocket and satellite data by applying the perfect gas law and a different lapse rate for each layer (see Tab. A.2 for the values that apply for the atmosphere from sea level to 11 km). Below 32 km the *Standard Atmosphere* is identical with the standard from the *International Civil Aviation Organization* (ICAO).

The relation of pressure and altitude of the *Standard Atmosphere* is based on the derivation presented in Section A.2 and Section A.2.1. Local changes in gravitational acceleration are neglected. Therefore, the altitude h is a geopotential altitude rather than geometric altitude. Pasting the constants of Tab. A.2 into (A.2) and (A.3) yields

$$p(h) = 101325 \text{ Pa} \left[1 - \frac{h}{44.331 \times 10^3 \text{ m}} \right]^{5.263} \quad (\text{A.4})$$

² The true local gradient varies from $-0.3 \text{ K}/100 \text{ m}$, in case of warm air gliding up onto cold air, up to $-0.8 \text{ K}/100 \text{ m}$, when cold air sets in.

Table A.2: Atmosphere model Constants according to the 1976 U.S. Standard Atmosphere.

Symbol	Value	Unit	Description
T_z	-273.15	°C	absolute zero
$r_{(\text{earth})}$	6356.766	km	effective earth radius
g_0	9.80665	m/s ²	gravitational acceleration at 45° latitude
R^*	8.31432	J/(mole K)	universal gas constant
M_{air}	28.9644×10^{-3}	kg/mol	mean molar mass of air
ρ_{air_0}	1.225	kg/m ³	air density at sea level
p_0	1013.25	Pa	mean pressure at sea level (= 760 mmHg)
T_0	288.15	K	mean temperature at sea level (= 15 °C)
T_h	-6.5	K/km	mean lapse rate (altitude < 11 km)
R_{air}	287.053	m ² /s ² K	gas constant for dry air ($R = R^*/M$)

$$h(p) = -44.331 \times 10^3 \text{ m} \left[1 - \left(\frac{p}{101325 \text{ Pa}} \right)^{0.19} \right]. \quad (\text{A.5})$$

These formulas apply very well and the typical error is below 1 % increasing to 3 % under extreme circumstances. The error is mainly due to the assumption of dry air, i.e. humidity is neglected (the molecular mass of water is smaller than the mass of air causing an error in M).

A.3 Pressure units definition and conversion

Table A.3: Pressure units and conversion factors.

	Pascal [Pa]	Bar [bar]	technical Atmosphere [at]	Torr [Torr]	Pounds per Square Inch [psi]
1 Pa	[N/m ²]	1	10 μ	$\approx 7.5\text{m}$	$\approx 145\mu$
1 bar	[Mdyne/cm ²]	100k	1	≈ 750	≈ 14.504
1 at	[kp/cm ²]	$\approx 98.1\text{k}$	≈ 0.981	≈ 736	≈ 14.22
1 Torr	[mmHg]	≈ 133.3	$\approx 1.33\text{m}$	1	19.34m
1 psi	[lbf/in ²]	$\approx 6.9\text{k}$	$\approx 69\text{m}$	51.71	1

References

- [BS97] M. N. Berberan-Santos, E. N. Bodunov and L. Pogliani: *On The barometric formula*; American Journal of Physics; 1997; 65(5): pp. 404–412.

*Do not go where the path may lead;
instead, go where there is no path
and leave a trail.*

Ralph Waldo Emerson

B

Micromachining on Fused Silica

B.1 Material properties of thin-films

Table B.1: Literature data for *Young's* modulus and *Poisson's* ratio of silicon and fused silica. The biaxial modulus remains constant in silicon for all directions in the {100} plane [Bra73]. *Young's* modulus, *Poisson's* ratio, and consequently biaxial modulus are invariant for all directions in the {111} plane [Bra73]. (Explicit numeric data for additional crystallographic directions is calculated and graphically presented in [Wor65].)

layer	<i>Young's</i> modulus [GPa]	<i>Poisson's</i> ratio [1]	biaxial modulus [GPa]	shear modulus [GPa]	comment	source
silicon {111}, arb. dir.	168.9	0.262	228.9	90.7	all mech. prop. invariant	[Bra73]
silicon {100}, <001>	130.2	0.279	180.6	70.6	biaxial mod. invariant	[Bra73]
silicon {100}, <011>	168.9	0.064	180.6	84.8	biaxial mod. invariant	[Bra73]
silicon {110}, <001>	130.2	0.279	180.6	70.6		[Bra73]
silicon {110}, <111>	187.5	0.182	229.2	97.0		[Bra73]
fused silica	72.0	0.170	86.7	30.8		[Sch07]

B.1.1 Thermal expansion of fused silica and silicon

The thermal expansion of silicon wafers over the temperature range of 300 K – 1500 K can be calculated with [Oka84]

$$\alpha = 3.725 \times 10^{-6} / \text{K} \left(1 - \exp[-5.88 \times 10^{-3} / \text{K}(T - 124)] \right) + 5.548 \times 10^{-10} / \text{K}^2 T \quad (\text{B.1})$$

Table B.2: Coefficients for the calculation of the thermal strain of silicon (fit according to [Oka84] and (2.6)) and fused silica. The coefficients represent the interpolation of elongation data given in [Tou77] and thermal expansion coefficients given in [Sch07].

coefficient	unit	fused silica	silicon
ε_0	1	$+1.3875 \times 10^{-5}$	-5.7191×10^{-5}
ε_1	$^{\circ}\text{C}^{-1}$	$+6.9957 \times 10^{-7}$	$+2.8275 \times 10^{-6}$
ε_2	$^{\circ}\text{C}^{-2}$	-2.9101×10^{-10}	$+1.6114 \times 10^{-9}$
ε_3	$^{\circ}\text{C}^{-3}$	$+1.6768 \times 10^{-14}$	-4.8926×10^{-13}

Table B.3: Coefficients for the calculation of the thermal expansion coefficients of silicon (fit according to data given in [Oka84] with approximation (2.6)) and fused silica (interpolation of elongation data given in [Tou77] and thermal expansion coefficients given in [Sch07]).

coefficient	unit	fused silica	silicon
α_0	$^{\circ}\text{C}^{-1}$	$+6.9957 \times 10^{-7}$	$+2.8275 \times 10^{-6}$
α_1	$^{\circ}\text{C}^{-2}$	-5.8202×10^{-10}	$+3.2228 \times 10^{-9}$
α_3	$^{\circ}\text{C}^{-3}$	$+5.0304 \times 10^{-14}$	-1.4678×10^{-12}

B.1.2 Wafer curvature measurement procedure

Wafer curvature measurements were conducted in course of this work. In most cases these measurements took place simultaneous on silicon and fused silica substrates to allow for a direct comparison of the resulting stress values. The wafers were prepared in the following manner to ensure similar deposition conditions:

1. deposition of 100 nm in-situ boron-doped poly
2. anneal 12 h at a temperature above or equal all later anneal steps (i.e. 800 °C)
3. deposition of 100 nm low-stress nitride (Nit-D20) (this step was omitted for nitride layers under test)
4. deposition of the film under test → 1. curvature measurement
5. back side strip of film under test → 2. curvature measurement
6. 12 h anneal @ 800 °C in N₂ → 3. curvature measurement

Table B.4: Measurement data for the thermal strain of fused silica and silicon in comparison to results obtained with approximation (2.6) and the coefficients summarized in Tab. B.2.

temperature [K] [°C]		fused silica			silicon	
		[Sch07] [10 ⁻⁴]	[Tou77] [10 ⁻⁴]	interpol. [10 ⁻⁴]	[Oka84] [10 ⁻⁴]	interpol. [10 ⁻⁴]
293	20	0	0	0	0	0
350	77	—	0.38	0.38	1.57	1.7
373	100	0.37	—	0.53	2.27	2.41
400	127	—	0.69	0.70	3.13	3.27
473	200	0.94	—	1.15	5.61	5.69
500	227	—	1.29	1.30	6.58	6.62
573	300	1.52	—	1.70	9.29	9.23
600	327	—	1.84	1.84	10.33	10.23
700	427	—	2.33	2.33	14.27	14.06
800	527	—	2.77	2.76	18.35	18.09
873	600	2.56	—	3.05	21.39	21.14
900	627	—	3.13	3.14	22.52	22.29
1000	727	—	3.46	3.47	26.78	26.62
1073	800	—	—	3.68	29.92	29.86
1100	827	—	3.74	3.75	31.10	31.07
1200	927	—	3.97	3.98	35.48	35.59

It must be noted that the actual stress of a layer under test may deviate considerably if deposited on silicon nitride but this procedure was chosen to maintain comparability. The results for the biaxial-moduli given in Tab. B.9 and Section 2.2 were obtained by application of the latter procedure. More details on wafer curvature measurement can be found in Section 2.2.1.

B.1.3 Improved version of Stoney's equation

Stoney's equation is frequently used to predict the stress of thin films (see Section 2.2 for an explanation of the symbols):

$$\sigma_F = \frac{E_S' t_S^2}{6 t_F} \left(\frac{1}{r_0} - \frac{1}{r} \right) \quad \text{with} \quad E_S' = \frac{E_S}{1 - \nu_S}$$

The approximation becomes more accurate for thinner films and thicker substrates. The error can be calculated with [Kle00]

$$\epsilon_{St} = \delta \frac{1 - \xi \delta^2}{1 + \xi \delta^3}.$$

Stoney's equation was modified by Atkinson to lower the magnitude of ϵ_{St} . The resulting formula is well suited for thicker layers and thinner substrates:

$$\sigma_F = \frac{E_S'}{6} \frac{t_S^3}{t_F^2(1 + t_S/t_F)} \left(\frac{1}{r_0} - \frac{1}{r} \right). \quad (B.2)$$

The error of Atkinson's formula was calculated by [Kle00] and equates to

$$\epsilon_{At} = \epsilon_{St} - \frac{\delta}{1 + \xi\delta^3}.$$

The analysis of Atkinson's formula shows that the film stress is always overestimated but is below 1% for thickness ratios up to $\delta = 10\%$ and modulus ratios ranging between $\xi = 0 \dots 3$ (see [Kle00] for more details).

B.1.4 Vertical stress distribution

A general treatment of stress within a multi-layer structure of arbitrary individual thickness can be found in [Tow87]. Handy equations are given for the simplification of $t_i \ll t_S$, i.e. much thinner layers on a thick substrate, leading to

$$\sigma_S = E_S' \left[\left(\frac{t_S}{2} - z \right) K + \sum_{i=1}^N \frac{E_i' t_i}{E_S' t_S} \ln \left(\frac{d_i}{d_S} \right) \right] \quad (B.3)$$

$$\sigma_i = E_i' \ln \left(\frac{d_S}{d_i} \right) \quad (B.4)$$

where d_S and d_i are the relaxed diameter of substrate and i^{th} layer, respectively. The other variables have their usual meaning. z is zero at the substrate bottom and is counted positively to the substrate surface. The first term in the brackets of (B.3) accounts for stress due to substrate bending whereas the second term describes the contribution of planar stress. The individual films do only interact with the substrate. The presence of neighbor layers and the individual layer order has no significant influence on the resulting stress and strain (the terms considering these effects have been omitted in (B.3) and (B.4)). The overall curvature K

$$K = \sum_{i=1}^N K_i \quad (B.5)$$

is a superposition of the contributions of the individual layers

$$K_i = 6 \frac{E_i' t_i}{E_S' t_S^2} \ln \left(\frac{d_S}{d_i} \right). \quad (B.6)$$

The strain at the substrate surface $z = t_s$ can be calculated as function of curvature by pasting (B.5) into (B.3) yielding

$$\varepsilon_S = \underbrace{-\frac{t_s K}{2}}_{\text{bending}} - \underbrace{\frac{t_s K}{6}}_{\text{plane stress}}. \quad (\text{B.7})$$

This results for a freely bent substrate in a surface strain of

$$\varepsilon_S = -\frac{2}{3} t_s K \quad (\text{B.8})$$

and

$$\varepsilon_S = -\frac{1}{6} t_s K \quad (\text{B.9})$$

for a substrate attached to a vacuum chuck which forces the substrate into a planar shape (K denotes of cause the curvature of the un-clamped substrate).

B.1.5 Surface-micromachined stress indicators

Stress of LPCVD layers can be measured with surface-micromachined indicator structures as proposed by [Dri93] and further worked out in [Sto96], [Elb97] and [Elb98]. The indicator geometries in course of this work are illustrated in Fig. B.1 with the dimensions summarized in Tab. B.5. The indicator displacement expressed as sprocket count N_s can be calculated with the formula

$$N_s = S_i C_H \frac{\sigma_F}{E_F} \quad (\text{B.10})$$

which requires *Young's* modulus E_F and stress σ_F of the deposited. The pointer

Table B.5: Physical dimensions of fabricated stress indicators. All indicators had a sprocket pitch P_S of $5 \mu\text{m}$, a nonius pitch P_N of $4.5 \mu\text{m}$, and a width of W_P of $20 \mu\text{m}$.

pointer identifier	hinge length L_H [μm]	hinge width W_H [μm]	hinge radius R_H [μm]	hinge pitch P_H [μm]	beam length L_B [μm]	beam width W_B [μm]	pointer length L_P [μm]	hinge corr. C_H [1]
i	10	3	3	20	150	30	202.5	0.91
n	20	5	4	20	300	50	202.5	0.86
k	10	3	3	10	400	50	202.5	0.72
b	20	5	4	20	500	50	402.5	0.86

sensitivity is represented by S_i and C_H denotes a correction which accounts for the influence of the hinge deformation generally decreasing the pointer's actual dis-

placement. Pointer sensitivity is calculated with formula [Sto96]

$$S_i = \frac{P_S P_H}{4 L_P (L_B + L_H + \frac{1}{2} W_P)}$$

The meaning and magnitude of all variables are given in Tab. B.5. See Tab. B.6 for a summary of example readings for all fabricated indicator geometries as well as values for the sensitivities S_i .

Table B.6: Sensitivities of fabricated stress pointers. The example indicator displacements are calculated with (B.10).

pointer	sensitivity S_i	PBor560	Nit-Z20	TEOS4Z
		@ $\sigma = 200$ MPa $E = 163$ GPa	@ $\sigma = 1.15$ GPa $E = 240$ GPa	@ $\sigma = 200$ MPa $E = 70$ GPa
	[sprockets]	[sprockets]	[sprockets]	[sprockets]
i	1377	1.54	6.00	3.58
n	2673	2.82	11.01	6.57
k	6804	6.01	23.47	14.00
b	8533	9.00	35.16	20.97

Table B.7: Error of indicator reading caused by support displacement. The given example values represent the deviations from true readings for a PBOR560 film ($\sigma = 200$ MPa, $E_F = 163$ GPa) being supported on a 100 nm Nit-Z20 layer, assuming furthermore, the complete removal of this nitride layer during sacrificial layer etch (see Fig. 2.8 for further illustration).

fused silica					
indicator	i	n	k	b	
strain	43.9×10^{-6}	27.3×10^{-6}	23.1×10^{-6}	20.6×10^{-6}	[1]
reading	0.06	0.06	0.11	0.15	[sprockets]
error	3.6	2.2	1.9	1.7	[%]
error	7.2	4.4	3.8	3.4	[MPa]
silicon					
indicator	i	n	k	b	
strain	14.4×10^{-6}	7.9×10^{-6}	6.3×10^{-6}	5.3×10^{-6}	[1]
reading	0.02	0.02	0.03	0.04	[sprockets]
error	1.2	0.6	0.5	0.4	[%]
error	2.3	1.3	1.0	0.9	[MPa]

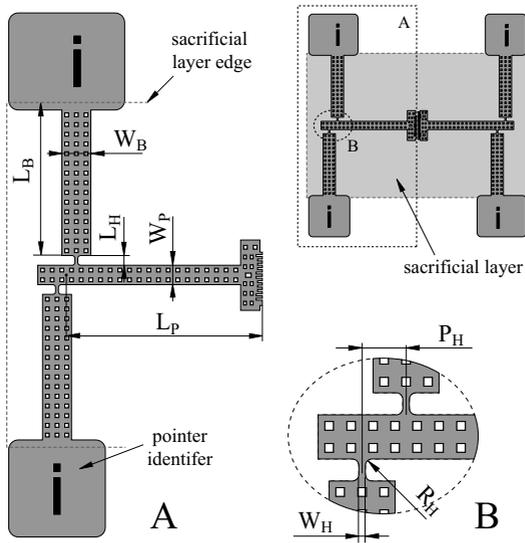


Fig. B.1: Dimensional drawing of the surface micromachined pointer used for stress measurement of deposited materials.

B.1.6 Stress gradient of surface-micromachined layers

Spiral shape test structures for the measurement of average stress gradients in surface-micromachined structures were proposed by [Fan90] and further worked out in [Sto96], [Elb97] and [Elb98]. The most sensitive and reliable structure out of the designs given in [Sto96] was used for this work. The geometry of coil 4A is depicted in Fig. B.2. The spiral has a width of $20\ \mu\text{m}$ and a length L_S of 3.455 mm. Its geometry is defined by eight half circle segments with the radii $85\ \mu\text{m}$, $100\ \mu\text{m}$, $115\ \mu\text{m}$, $130\ \mu\text{m}$, $145\ \mu\text{m}$, $160\ \mu\text{m}$, $175\ \mu\text{m}$ and $190\ \mu\text{m}$.

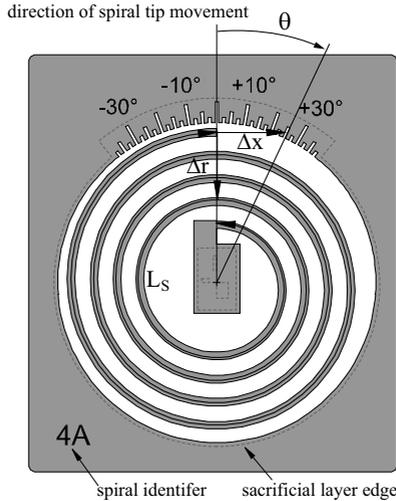


Fig. B.2: Dimensional drawing of the coil structure used for stress gradient measurement surface micromachined LPCVD layers.

The spiral displacement can be sampled by either reading the angular displacement θ from the integrated scale or by measuring the lateral tip displacement Δx . The average stress gradient γ_σ is the product of the corresponding normalized gradient Γ_σ times the *Young's* modulus of the layer under test

$$\gamma_\sigma = E_F \Gamma_\sigma.$$

Negative and positive stress gradients can not be distinguished because the spiral tip displacement is positive in both cases. Discrete computed data from [Sto96] relating spiral displacement to normalized stress gradient is presented in Fig. B.3 and

Tab. B.8. This data can be fitted with a power function for lateral displacement

$$\Gamma_{\sigma} = a_x (\Delta x / 1 \text{ m})^{b_x} \quad \text{with} \quad a_x = 0.13655 \text{ 1/m}, \quad b_x = 0.5128 \quad (\text{B.11})$$

or angular deflection

$$\Gamma_{\sigma} = a_{\theta} (\theta / 1^{\circ})^{b_{\theta}} \quad \text{with} \quad a_{\theta} = 0.2563 \text{ 1/m}, \quad b_{\theta} = 0.50084. \quad (\text{B.12})$$

Table B.8: Displacement data for the stress gradient measurement test structure of Fig. B.2 (data taken from [Sto96]). The absolute stress gradient γ_{σ} is the product of normalized gradient Γ_{σ} times the layer's Young's modulus E_F (data of this table is illustrated in Fig. B.3).

displacement lateral Δx [μm]	displacement radial Δr [μm]	displacement angular θ [$^{\circ}$]	normalized stress gradient Γ_{σ} [1/m]
1.68	4.09	0.5	0.185
4.79	6.80	1.4	0.309
11.01	10.91	3.3	0.463
19.08	13.64	5.8	0.617
42.18	20.25	13.2	0.926
72.80	27.27	22.9	1.235

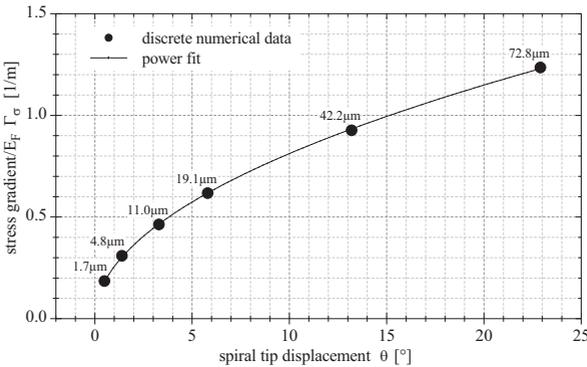


Fig. B.3: Normalized stress gradient versus Γ_{σ} angular coil displacement θ according to [Sto96] fitted with (B.12) (full line). Discrete values at data points indicate the lateral tip displacement Δx .

B.1.7 Measurement of LPCVD film biaxial-moduli

Table B.9: Difference of thermal stress $\Delta\sigma_t$ on silicon and silica due to the difference of thermal strain $\Delta\varepsilon$. Measurement results for CVD-layers (for the deposition parameters see Tab. B.11). The given biaxial moduli were determined by means of the procedure described in Section B.1.7 and can be also compared in Fig. 2.6(a). The temperatures marked with a * for annealed CVD oxides indicated a relaxation of these layers upon anneal resulting in a thermal strain proportional to the anneal temperature.

layer	T_d [°C]	E' [GPa]	$\Delta\varepsilon \times 10^3$ [MPa]	$\Delta\sigma_t$ [MPa]	σ_{FS} [MPa]	σ_{Si} [MPa]
as-deposited						
Nit-Z20	801	291.4	2.617	763	1021	258
Nit-Z10	812	297.5	2.662	791	913	122
Nit-D20	821	293.4	2.702	793	652	-140
PBOR560	554	227.2	1.645	374	-204	-578
PBOR580L	580	151.2	1.732	262	333	71
aSiX585	585	142.8	1.751	250	272	22
Poly4Zol	620	194.4	1.891	368	117	-251
TEOS4Z	705	20.1	2.225	60	81	51
LTO450Z4	450	33.2	1.253	55	76	21
after 12 h@800 °C						
Nit-Z20	801	318.7	2.617	834	1151	317
Nit-Z10	812	284.9	2.662	759	976	217
Nit-D20	821	291.5	2.702	788	660	-128
PBOR560	554	211.1	1.645	347	-94	-441
PBOR580L	580	202.0	1.732	350	392	42
aSiX585	585	219.4	1.751	384	485	101
Poly4Zol	620	203	1.891	385	233	-152
TEOS4Z	(800)*	89.7	2.617	235	198	-37
LTO450Z4	(800)*	89.6	2.617	235	175	-60
after 12 h@800 °C without viscous flow						
TEOS4Z	705	82.3	2.225	235	198	-37
LTO450Z4	450	146.0	1.253	235	175	-60

Table B.10: Literature data for the *Young's* modulus and *Poisson's* number of LPCVD layers. Numbers in brackets indicate assumed values.

layer	<i>Young's</i> modulus [GPa]	<i>Poisson's</i> ratio [1]	biaxial modulus [GPa]	shear modulus [GPa]	comment	source
poly-Si	149.3	0.200	186.6	62.1	[100] texture	[MS95] [MS96]
poly-Si	166.0	0.229	215.3	67.5	[110] texture	[MS95] [MS96]
poly-Si	171.5	0.240	225.7	69.2	[111] texture	[MS95] [MS96]
poly-Si	159.9	0.218	204.5	65.6	[311] texture	[MS95] [MS96]
poly-Si	162.8	0.223	209.5	66.6	no texture	[MS95] [MS96]
TEOS	56.0	0.250	72.0	22.4	as-deposited	[Car02]
TEOS	73.0	0.220	94.0	29.9	anneal 30 min@1160 °C	[Car02]
SiN	256.0	0.280	355.0	100	low-stress	[Car02]
Si ₃ N ₄	250.0	(0.250)	333.3	100	DCS/amonia 1/3	[MS95]
SiN	242.0	(0.250)	322.7	96.8	DCS/amonia 2...5	[MS95]

B.2 Thin-film deposition

B.2.1 LPCVD process parameters

Table B.11: LPCVD process parameters: poly-silicon, nitride, and oxide.

layer	pressure [mTorr/Pa]	gas ₁ door/vac. [sccm]	gas ₂ door/vac. [sccm]	temp. (mean) [°C]	rate (mean) [nm/min]	comment
Nit-D20 (SiN _{0.61})	152/20.3	NH ₃ 11/–	SiH ₂ Cl ₂ 95/–	821	≈ 2.13	$\sigma_{\text{Si}} \approx -200$ MPa SiH ₂ Cl ₂ /NH ₃ = 8.84
Nit-Z10 (SiN _{0.96})	152/20.3	NH ₃ 16/–	SiH ₂ Cl ₂ 87/–	812	≈ 2.48	$\sigma_{\text{Si}} \approx +100$ MPa SiH ₂ Cl ₂ /NH ₃ = 5.44
Nit-Z20 (SiN _{1.04})	152/20.3	NH ₃ 18/–	SiH ₂ Cl ₂ 85/–	801	≈ 3.66	$\sigma_{\text{Si}} \approx +200$ MPa SiH ₂ Cl ₂ /NH ₃ = 4.72
Nit-Z100 (SiN _{1.33})	360/48	NH ₃ 200/–	SiH ₂ Cl ₂ 50/–	765	≈ 3.0	$\sigma_{\text{Si}} \approx +1000$ MPa SiH ₂ Cl ₂ /NH ₃ = 0.25
PBOR560	200/26.7	B ₂ H ₆ 3.3/6.5	SiH ₄ 47/100	559	≈ 3.29	gas ₁ : 10 % B ₂ H ₆ in SiH ₄ B ₂ H ₆ /SiH ₄ = 6.29×10^{-3}
PBOR600	200/26.7	B ₂ H ₆ 3.3/6.5	SiH ₄ 47/100	600	≈ 6.28	gas ₁ : 10 % B ₂ H ₆ in SiH ₄ B ₂ H ₆ /SiH ₄ = 6.29×10^{-3}
PBOR620	200/26.7	B ₂ H ₆ 3.3/6.5	SiH ₄ 47/100	600	≈ 9.69	gas ₁ : 10 % B ₂ H ₆ in SiH ₄ B ₂ H ₆ /SiH ₄ = 6.29×10^{-3}
PBO560BT	200/26.7	B ₂ H ₆ 3.8/7.5	SiH ₄ 46.5/99	554	≈ 3.19	gas ₁ : 10 % B ₂ H ₆ in SiH ₄ B ₂ H ₆ /SiH ₄ = 7.26×10^{-3}
PBOR580L	250/33.3	B ₂ H ₆ 1.3/2.6	SiH ₄ 47/100	580	≈ 4.55	gas ₁ : 10 % B ₂ H ₆ in SiH ₄ B ₂ H ₆ /SiH ₄ = 2.59×10^{-3}
aSiX585	150/20	SiH ₄ 75/70	-	585	≈ 3.93	
Poly4Zol	120/16	SiH ₄ 55/70	-	620	≈ 6.9	
TEOS4Z	280/37.3	SiO ₄ (C ₂ H ₅) ₄ 70/–	-	705	≈ 8.1	
LTO450Z4	400/53.3	O ₂ 60/–	SiH ₂ (C ₂ H ₅) ₂ on/–	450	≈ 2.9	

B.2.2 LPCVD oxide

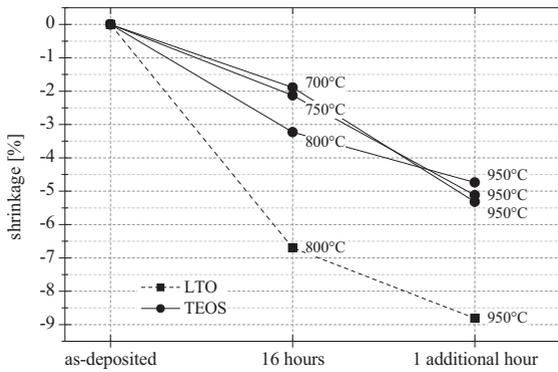


Fig. B.4: Shrinkage of CVD low- and high-temperature oxide during anneal in N_2 ambient.

B.2.3 Deposition of poly-crystalline silicon

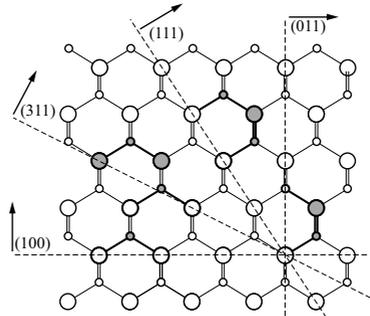


Fig. B.5: Projection of the crystal structure of silicon and the contours of some crystal faces according to [Bis86]. The shaded circles indicate the number of atoms which are required for a growth in the respective crystal direction.

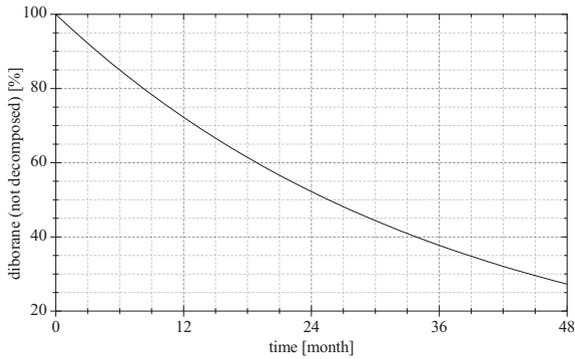


Fig. B.6: Decomposition of diborane versus time. The amount of un-decomposed B_2H_6 N of an initial amount N_0 can be approximated with $R = N/N_0 \exp[-0.02708 \text{ 1/month} \times t]$ [Air06].

Table B.12: Literature sources related to boron-doped LPCVD poly-silicon.

year	precursor ratio[10 ⁻³]	pressure [mTorr]	temperature [°C]	source	comment
1969	cSi/B ₂ O ₃ 0	-	-	[Vic69]	B solid solubility, B diffusion constant
1975	SiH ₄ /Ar 0	atmo	650	[Set75]	boron implantation, res. diffusion model
1982	SiH ₄ /N ₂ 0	500	620	[Lee82]	boron implantation, resistivity
1985	-	-	-	[Sin85]	resistivity, emission diffusion model
1990	-	-	-	[Kim90]	influence of dopant on secondary grain growth
1994	-	-	-	[Ari94]	dopant segregation at grain boundaries
1973	SiH ₄ /B ₂ H ₆ /H ₂ 0 – 5.5	atmo	527-1050	[Eve73]	rate vs ratio, transition temp., res. vs temp., act. energy
1986	SiH ₄ /B ₂ H ₆ /He 0.005 – 3.3	304	520-665	[Nak86]	act. energy, Si-B compound, transition temp., rate vs B inc., B inc. vs ratio, dep. model
1987	SiH ₄ /BCl ₃ /H ₂ not reported	98-750	570-620	[BD87]	transition temperature, grain size, B incorporation
1988	SiH ₄ /B ₂ H ₆ 0-20	350-410	450-600	[Mar88]	rate vs ratio, activation energy, resistivity, transition temp.
1989	SiH ₄ /B ₂ H ₆ /H ₂ 5	2.5-1000	515-700	[Jou89]	crystal structure and size, texture vs temp. and pressure
1989	SiH ₄ /B ₂ H ₆ /H ₂ 5	2.5-1000	515-700	[Haj89]	act. energy, B inc., res. vs pres., B inc, and temp.
1991	SiH ₄ /BCl ₃ /H ₂ 13.5	390	520-620	[BD91]	act. energy, rate enhancement, transition temp., crystal struct. res. vs temp. and thickness, optical constants vs temp.
1995	SiH ₄ /BCl ₃ /H ₂ 0 – 13.5	350	555	[Fre95]	rate enhancement, uniformity, B inc., crystal struct., model
1996	SiH ₄ /BCl ₃ /H ₂ not reported	400	520-605	[Bou96]	crystal struct. and quality as-dep. and annealed, res. vs anneal, oxidation dyn.
2003	SiH ₄ /B ₂ H ₆ /Ar 12.5 – 45.5	100-200	520-560	[Yl603]	stress and res. vs anneal temp., B inc., crystal struct.
2004	SiH ₄ /BCl ₃ /N ₂ 0.8 – 108	76-341	555	[Cau04]	B inc., crystal struct. deposition on SiO ₂ and Si ₃ N ₄

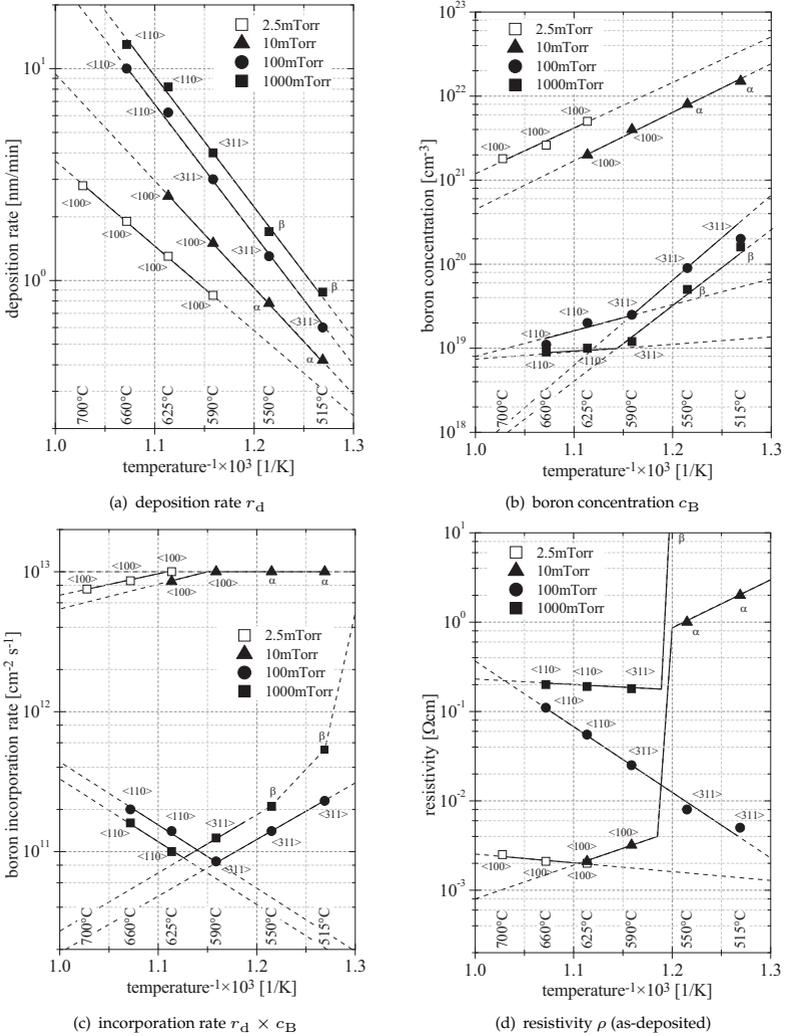


Fig. B.7: Deposition rate, boron concentration, boron incorporation rate, and resistivity of in situ boron-doped poly-silicon according to [Haj89]. All measurement data corresponding to transport limited depositions have been omitted. The boron/silane ratio of the $B_2H_6/SiH_4/H_2$ gas system was fixed to 5×10^{-3} . α and β indicate high boron concentration (Si-B compound) and low concentration amorphous silicon, respectively.

B.2.4 Dopant solubility and diffusivity

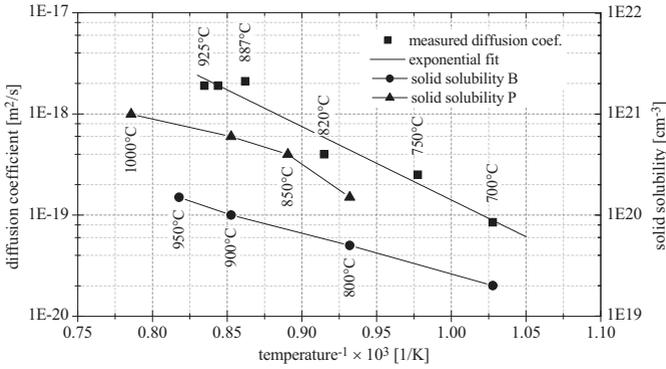


Fig. B.8: Diffusion coefficient of boron and solid solubility of boron in silicon according to data given by [Vic69] (numerical values are given in Tab. B.13). Solid solubility data for phosphorous was taken from [Eve73].

Table B.13: Low-temperature diffusion coefficient and solid solubility of boron in silicon according to [Vic69]. (Diffusion coefficient corresponds to measurement data presented in [Vic69] fitted to $\mathcal{D} = \mathcal{D}_0 \exp[-E_A/kT]$ with $\mathcal{D}_0 = 2.543 \times 10^{-12} \text{ m}^2/\text{s}$ and $E_A = 2.3067 \times 10^{-19} \text{ J}$.)

temperature [°C]	solid solubility [cm ⁻³]	diffusion coefficient [m ² sec ⁻¹]
700	2.0×10^{19}	8.88×10^{-20}
800	5.0×10^{19}	4.40×10^{-19}
900	1.0×10^{20}	1.66×10^{-18}
950	1.5×10^{20}	2.97×10^{-18}

B.2.5 Resistivity of doped poly-silicon films

The resistivity model, as proposed by [Set75], is based on thermionic emission:

$$\sigma_{\text{pSi}} = q \bar{p} \mu_{\text{eff}} \quad (\text{B.13})$$

$$\mu_{\text{eff}} = d_c q \sqrt{\frac{1}{2\pi m^* kT}} \exp\left(-\frac{E_B}{kT}\right), \quad (\text{B.14})$$

where q , d_c , and m^* denote unity charge, grain diameter, and effective mass, respectively. Conductivity σ_{pSi} is considered in analogy to conduction in crystalline silicon but the average carrier concentration \bar{p} and the effective mobility μ_{eff} are functions of dopant density and layer morphology. E_B accounts for the energy barrier at the grain boundary and k , T have their usual meaning.

Two cases exist which can be distinguished by consideration of grain boundary trap density Q_t , grain diameter d_c , and dopant density N .

Case 1: Very fine grained poly-silicon or low dopant levels ($Q_t > d_c N$):

$$\bar{p} = \frac{n_i}{d_c q} \exp\left(\frac{E_B + E_f}{kT}\right) \operatorname{erf}\left[\frac{q d_c}{2} \sqrt{\frac{N}{2\epsilon_{\text{pSi}} kT}}\right] \sqrt{\frac{2\pi \epsilon_{\text{pSi}} kT}{N}} \quad (\text{B.15})$$

$$E_B = \frac{q^2 d_c^2 N}{8\epsilon_{\text{pSi}}} \quad (\text{B.16})$$

$$n_i = N_v \exp\left(-\frac{1}{2} E_g/kT\right) \quad (\text{B.17})$$

$$E_f = E_t - kT \ln\left[\frac{1}{2}(Q_t/d_c N - 1)\right] \quad (\text{B.18})$$

Case 2: Large grained poly-silicon or high dopant levels ($Q_t < d_c N$):

$$\bar{p} = p_b \left(1 - \frac{Q_t}{d_c N}\right) + \frac{1}{q d_c} \operatorname{erf}\left[\frac{q Q_t}{2} \sqrt{\frac{1}{2\epsilon_{\text{pSi}} N kT}}\right] \sqrt{\frac{2\pi \epsilon_{\text{pSi}} kT}{N}} \quad (\text{B.19})$$

$$p_b = N_v \exp[-(E_v - E_f)/kT] \quad (\text{B.20})$$

$$E_f = E_t - kT \ln\left[\frac{1}{2}(Q_t/d_c N - 1)\right] \quad (\text{B.21})$$

$$E_B = \frac{q^2 Q_t^2}{8\epsilon_{\text{pSi}} N} \quad (\text{B.22})$$

E_f , E_g , and E_t are the Fermi level, the band gap, and the trap energy level. ϵ_{pSi} , N_v , p_b denote the permittivity of poly-silicon, the density of states, and the carrier density within the grain bulk (undepleted), respectively.

The presented model was enhanced to an emission diffusion model by [Sin85].

B.2.6 Aluminum deposition

Table B.14: Aluminum sputtering process parameters.

parameter	data
machine	Materials Research Corporation MRCI
temperature	no temperature control, no pre-heating
sputter etch	Ar pressure: 1.1 mTorr, power: 0.3 kW, duration: 2 min
base layer	Ar pressure: 14 mTorr, power: 6 kW, duration: 2 cycles at 24.5 cm ³ /min, bias: non
top layer	Ar pressure: 14 mTorr, power: 6 kW, duration: 2 cycles at 24.5 cm ³ /min, bias: 0.05 A at 90 V

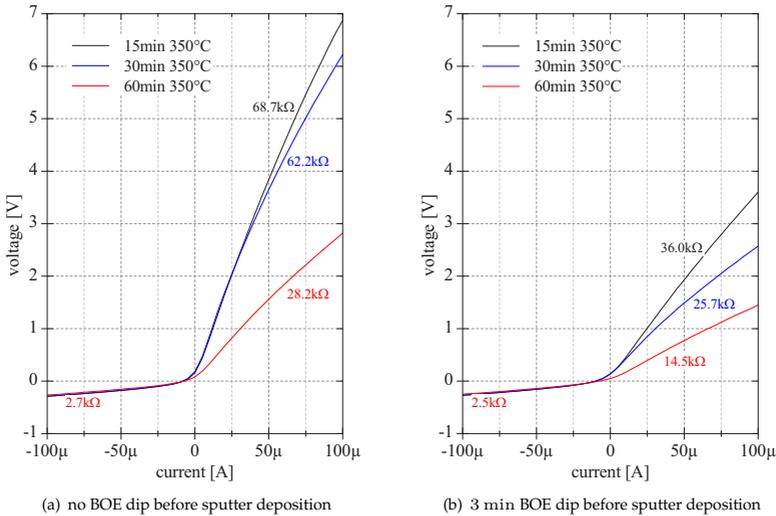


Fig. B.9: IV-plot of pure aluminum contacts to mono crystalline silicon. The round contact pads had a diameter of 95 μm and the grinded wafer backside was metallized with a Cr/Au film. All samples (<100>-Si, 17 Ωcm – 22 Ωcm, p-type boron-doped) were sputter etched prior to metallization. The measurement was conducted with a Keithley Source Measurement Unit. The positive terminal was in contact to the aluminum pad on the wafer front side and the low terminal was connected to the chuck. Annealing took place on a hot plate in ambient atmosphere.

B.3 Wet etching

B.3.1 Recipes and etch rates

Table B.15: Etch rate coefficients and activation energies of fused-silica, LPCVD oxides, and LPCVD nitrides exposed to HF/HCl, 1 %HF, BOE and modified BOE. The presented numerical values are obtained from *Arrhenius* fits of the rate data summarized in Tab. B.17. The etchant recipes can be found in Tab. B.16.

material	etchant	rate coeff. R_0 [nm/min]	activation energy E_A [J]
fused-silica	HF/HCl	12.35×10^6	42.13×10^{-21}
fused-silica	BOE	206.48×10^6	61.10×10^{-21}
TEOS (as-deposited)	HF/HCl	-	-
TEOS (as-deposited)	BOE	60.16×10^9	75.39×10^{-21}
TEOS (1h@950 °C)	HF/HCl	8.73×10^6	35.43×10^{-21}
TEOS (1h@950 °C)	BOE	9.21×10^6	44.34×10^{-21}
LTO (as-deposited)	BOE	91.33×10^9	77.61×10^{-21}
FOX	BOE	0.71×10^6	37.18×10^{-21}
Si ₃ N ₄	HF/HCl	39.53×10^6	64.13×10^{-21}
Si ₃ N ₄	BOE	2.23×10^9	86.82×10^{-21}
Nit-Z20	HF/HCl	7.88×10^6	62.58×10^{-21}
Nit-Z20	BOE	72.21×10^6	76.75×10^{-21}
Nit-Z20	H ₃ PO ₄	90.48×10^9	141.84×10^{-21}
Nit-Z10	HF/HCl	722.14×10^6	76.75×10^{-21}
Nit-Z10	BOE	88.27×10^6	72.96×10^{-21}
Nit-Z10	H ₃ PO ₄	190.72×10^9	145.68×10^{-21}
Nit-D20	HF/HCl	4.88×10^6	68.11×10^{-21}
Nit-D20	BOE	738.48×10^6	89.59×10^{-21}
Nit-D20	H ₃ PO ₄	177.65×10^9	145.86×10^{-21}

Table B.16: Summary of wet-chemical etchant recipes (VP: volume part, WP: weight part).

name	mix	recipe and ingredients
phosphoric acid H_3PO_4	1 VP	<i>Honeywell Speciality Chemicals</i> 85 % H_3PO_4 Ortho-Phosphoric acid
mod. fluoric acid HF/HCl	1 VP	<i>Honeywell Speciality Chemicals</i> 50 % HF Hydrofluoric acid
	1 VP	<i>Honeywell Speciality Chemicals</i> 37 % HCl Hydrochloric acid
buffered oxide etch BOE	1 VP	<i>Honeywell Speciality Chemicals</i> Oxide etch 7:1 modified
mod. buffered oxide etch mod. BOE	50 WP	<i>Honeywell Speciality Chemicals</i> Oxide etch 7:1 modified
	30.5 WP	<i>Honeywell Speciality Chemicals</i> 1 % HF Hydrofluoric acid (50:1)
	19.5 WP	NH_4F ammonium fluoride
sulfo-peroxide-mixture Caro-clean	1 VP	<i>Honeywell Speciality Chemicals</i> 95 – 97 % H_2SO_4 Sulfuric acid
	1 VP	<i>T. J. Baker</i> 30 % H_2O_2 Hydrogen Peroxide
ammonium-peroxide-mixture SC1	1 VP	<i>Honeywell Speciality Chemicals</i> 25 % NH_3 Ammonia solution
	1 VP	<i>T. J. Baker</i> 30 % H_2O_2 Hydrogen Peroxide
	5 VP	H_2O deionized water
HF-dip 1 % HF	1 VP	<i>Honeywell Speciality Chemicals</i> 1 % HF Hydrofluoric acid (50:1)
solvent solvent	1 VP	<i>Honeywell Speciality Chemicals</i> Solvent NMP-AE5050
poly-etch P-etch	3 VP	<i>Honeywell Speciality Chemicals</i> SWF 63-33-4 Nitric acid-etching mixture
	2 VP	H_2O deionized water
	1/1000 VP	<i>3M Corporation</i> FC93 Fluorosurfactant
alu-etch A-etch	1 VP	<i>Honeywell Speciality Chemicals</i> PWS 80-16-4(65) Phosphoric acid etching mix.
chromium-etchant Cr-etch	1 VP	<i>Honeywell Speciality Chemicals</i> Ammonium cerium(IV) nitrate & Perchloric acid
aqua regia aqua regia	1 VP	<i>Honeywell Speciality Chemicals</i> 69 % HNO_3 Nitric acid
	3 VP	<i>Honeywell Speciality Chemicals</i> 37 % HCl Hydrochloric acid

Table B.17: Measured etch rates of fused-silica and LPCVD oxide layers exposed to HF/HCl, 1 %HF, BOE and modified BOE (see Tab. B.16 for etchant recipes).

layer	etchant	temp. [°C]	rate [nm/min]
fused-silica	HF/HCl	0	173.73
fused-silica	HF/HCl	20	372.29
fused-silica	BOE	20	57.40
fused-silica	BOE	40	150.53
TEOS (as-deposited)	HF/HCl	0	≈ 800
TEOS (as-deposited)	HF/HCl	20	-
TEOS (as-deposited)	BOE	20	≈ 490
TEOS (as-deposited)	BOE	40	≈ 1610
TEOS (as-deposited)	mod. BOE	20	105.73
TEOS (as-deposited)	1 %HF	20	≈ 25
TEOS (as-deposited)	H ₃ PO ₄	135	< 0.01
TEOS (1h@950 °C)	HF/HCl	0	653.8
TEOS (1h@950 °C)	HF/HCl	20	1250
TEOS (1h@950 °C)	BOE	20	160.9
TEOS (1h@950 °C)	BOE	40	323.9
TEOS (1h@950 °C)	1 %HF	20	≈ 8.3
LTO (as-deposited)	1 %HF	20	≈ 20.4
LTO (as-deposited)	BOE	20	≈ 429
LTO (as-deposited)	BOE	40	≈ 1460
LTO (as-deposited)	mod. BOE	20	100.1
FOX	1 %HF	20	≈ 5.9
FOX	BOE	20	≈ 72.3
FOX	BOE	40	≈ 130
FOX	mod. BOE	20	21.66

Table B.18: Measured etch rates of LPCVD silicon nitride layers exposed HF/HCl and BOE (see Tab. B.16 for etchant recipes).

layer	etchant	temp. [°C]	rate [nm/min]
Si ₃ N ₄	HF/HCl	0	1.63
Si ₃ N ₄	HF/HCl	20	5.20
Si ₃ N ₄	BOE	20	1.08
Si ₃ N ₄	BOE	40	4.25
Nit-Z20	HF/HCl	0	0.49
Nit-Z20	HF/HCl	20	1.52
Nit-Z20	BOE	20	0.42
Nit-Z20	BOE	40	1.41
Nit-Z20	H ₃ PO ₄	100	0.10
Nit-Z20	H ₃ PO ₄	135	1.06
Nit-Z10	HF/HCl	0	0.35
Nit-Z10	HF/HCl	20	1.31
Nit-Z10	BOE	20	0.40
Nit-Z10	BOE	40	1.39
Nit-Z10	H ₃ PO ₄	100	0.10
Nit-Z10	H ₃ PO ₄	135	1.13
Nit-D20	HF/HCl	0	0.07
Nit-D20	HF/HCl	20	0.24
Nit-D20	BOE	20	0.18
Nit-D20	BOE	40	0.74
Nit-D20	H ₃ PO ₄	100	0.09
Nit-D20	H ₃ PO ₄	135	1.02

B.3.2 Sacrificial layer etching

Table B.19: Summary of sacrificial layer etch rates measured with test structures and during fabrication of sensors with layout DRUCK2004. A graphical summary of the obtained results is presented in Fig. 2.40. The channel layer thickness was fixed to 250 nm throughout all conducted tests. A photo of the test structure with dimensions is presented in Fig. B.11(c).

sacrificial layer height t_S [μm]	channel geometry W_C, L_C, A_C [$\mu\text{m}, \mu\text{m}, \mu\text{m}^2$]	undercut $L_S, L_C + L_S$ [μm]	etch rate $(L_C + L_S)/t$ [$\mu\text{m}/\text{min}$]	comment
0.2	6, 9, 1.5	21, 30	0.50	test structure
0.2	6, 14, 1.5	16, 30	0.50	test structure
0.2	6, 19, 1.5	12, 31	0.52	test structure
0.2	9, 9, 2.25	22.5, 31.5	0.53	test structure
0.2	9, 14, 2.25	18, 32	0.53	test structure
0.2	9, 19, 2.25	13.5, 32.5	0.54	test structure
0.2	12, 9, 3	25, 34	0.57	test structure
0.2	12, 14, 3	19, 33	0.55	test structure
0.2	12, 19, 3	14, 33	0.55	test structure
0.2	6, 9, 1.5	21, 30	0.50	test structure
0.2	14, 9, 0.28	17.5, 26.5	0.44	test structure
0.2	6, 9, 1.78	21.5, 30.5	0.51	test structure
0.95	6, 9, 1.5	35, 44	0.73	test structure
0.95	6, 14, 1.5	28, 42	0.70	test structure
0.95	6, 19, 1.5	24, 45	0.75	test structure
0.95	9, 9, 2.25	35, 44	0.73	test structure
0.95	9, 14, 2.25	29, 43	0.72	test structure
0.95	9, 19, 2.25	25, 44	0.73	test structure
0.95	12, 9, 3	36, 45	0.75	test structure
0.95	12, 14, 3	30, 44	0.73	test structure
0.95	12, 19, 3	25.5, 45.5	0.76	test structure
0.2	4.7, 7, 1.17	31, 38	0.63	70 μm -Array
0.2	6, 9, 1.5	30, 39	0.65	90 μm -Array
0.2	8, 12, 2	30, 42	0.7	120 μm -Array

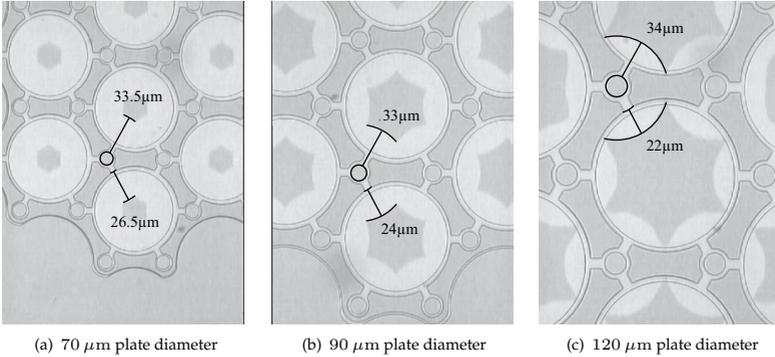


Fig. B.10: Undercut after 60 min sacrificial etch in HF/HCl at 0 °C for different sensor designs of layout DRUCK2004 (plate diameters 70 μm , 90 μm , and 120 μm).

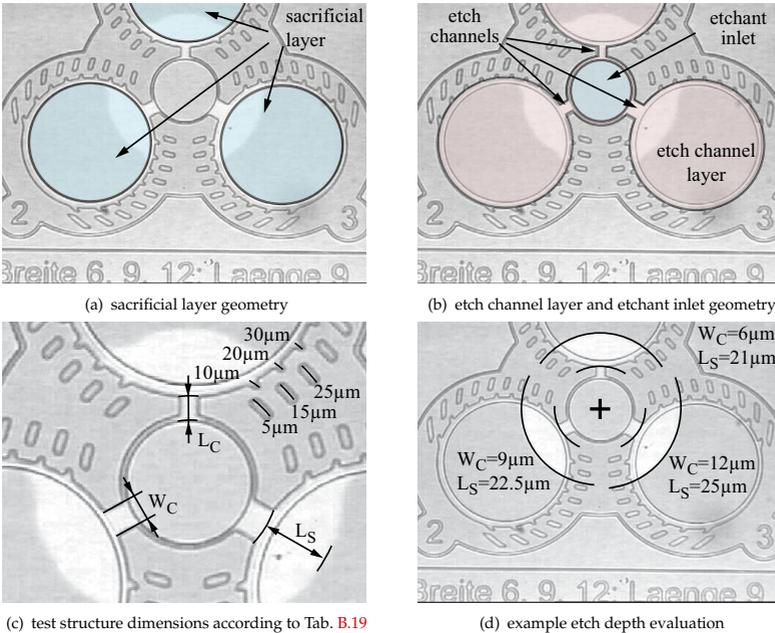


Fig. B.11: Sacrificial layer etch rate measurement test structure geometry and example result after immersion for 60 min in HF/HCl at 0 °C (see Tab. B.19 for more results).

B.4 Wafer thinning

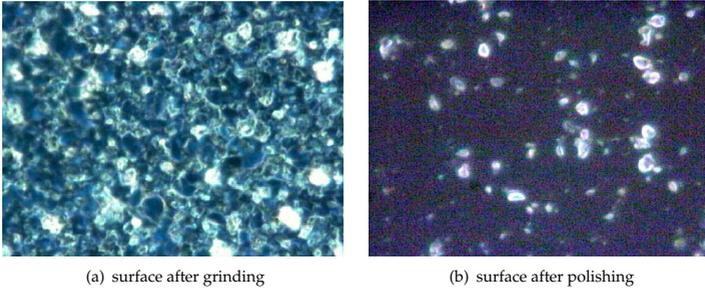


Fig. B.12: Surface roughness after grinding and polishing. Both dark-field microscope photographs are taken at $100\times$ magnification.

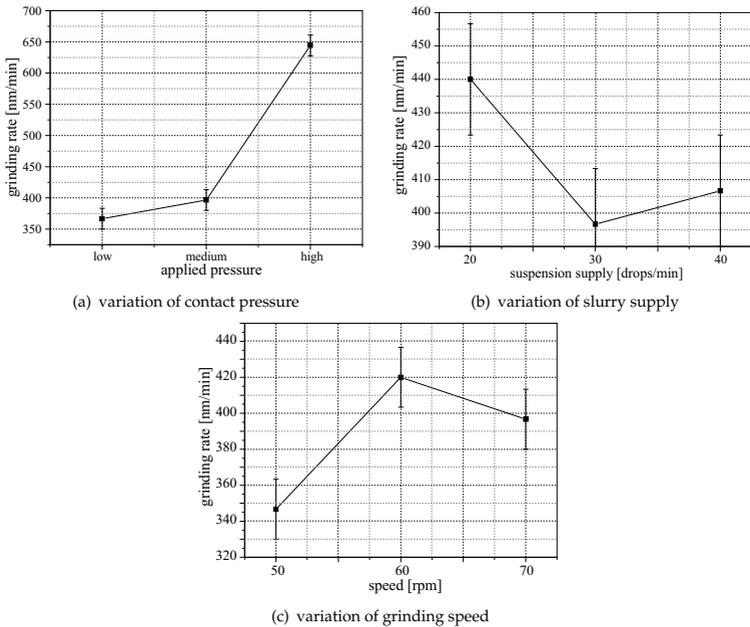


Fig. B.13: Influence of grinding process parameters on the grinding rate of fused silica [Bis05]. A 9:1 DI-water: Al_2O_3 -powder slurry was used on a Logitech PM5.

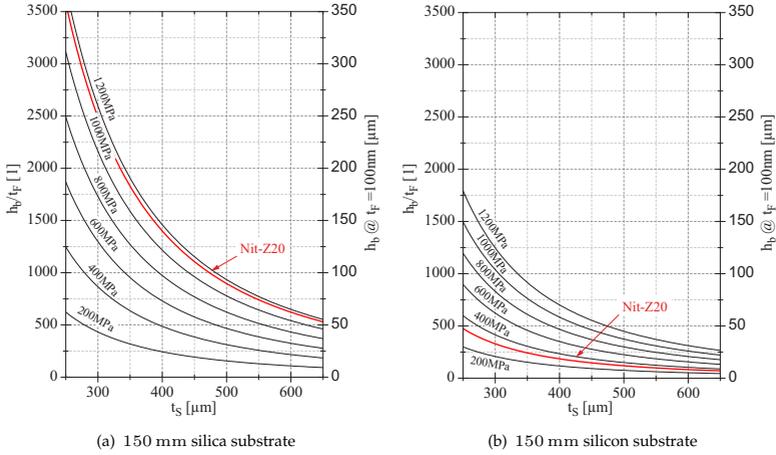


Fig. B.14: Wafer bow versus substrate thickness for various stress levels on 150 mm fused silica and silicon substrates.

B.5 Wafer dicing

Table B.20: Dicing process parameters.

parameter	data
machine	<i>Kulicke & Soffa Model 780</i>
dicing tape	<i>Ultrion Systems 1003R</i> thickness 135 μm
blade type	<i>Advanced Dicing Technologies</i> part no. 00777-6030-005 thickness 127 μm , grain size 30 μm
cutting depth	20 μm into dicing tape
dicing speed	< 3.5 mm/sec entry speed = cutting speed
rotary speed	14000 rpm

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Success consists of going from failure to failure
without loss of enthusiasm.

Sir Winston Leonard Spencer Churchill



Capacitive Pressure Sensor

C.1 Basic theory of circular plates under symmetric load

The mathematical treatment of plates started way back in history. Initially the mathematical work focused on vibrational problems and it was *Euler* who first solved the problem of free vibration of circular and rectangular plates already in 1766. His basic approach of using the analogy of stretched strings was refined by a number of mathematicians. Amongst others *J. Bernoulli Jr.*, *Poisson*, *Germain*, and *Lagrange* contributed in the derivation of the correct differential equations. It was finally *Navier* (1785 – 1836) who was the founder of the modern elastic theory of plates. He derived the exact static differential equations for plates with flexural resistance and solved them for plates with simply supported edges by using *Fourier* series. Today, *Kirchhoff* (1824 – 1887) is considered to be the founder of the plate theory due to his pioneering work. He contributed with a number of solutions for plates under large deflections and combined bending and stretching. Finally, *Love* applied *Kirchhoff's* work to thick plates. Their *Kirchhoff-Love* plate theory can be applied in a large number of cases and will be used in the following sections. More recently, *Timoshenko* made the work of Russian scientists accessible to the Western world and contributed by himself with solutions for large deflections. Finally a rigorous plate theory which also considers transverse shear forces was developed by *Reissner*.

Kirchhoff

Love

The following sections are mainly based on fundamentals that have been summarized by *Timoshenko* [Tim87]. The basic formulas for small and large deflections will be derived according to the *Kirchhoff-Love* plate theory. Furthermore, the applicability of the applied theory will be discussed and the influence of a lateral in-plane stress will be assessed. Finally, a special solution for plates in touch-mode operation will be derived.

C.1.1 Applicability of the *Kirchhoff-Love* plate theory

The following premises must be met for the applicability of the *Kirchhoff-Love* plate theory as summarized in [Szi74]:

1. The material must be elastic, homogenous and isotropic.

2. The plate must be flat.
3. The thickness of the plate must be small compared to its lateral dimensions (one tenth is considered to be a good ratio).
4. The deflection needs to be small compared to the plate dimensions, that is one fifth of the thickness or in terms of lateral dimension one fiftieth of the smallest lateral length.
5. No transverse shear needs not to be considered, that is straight lines normal to the middle surface remain straight and perpendicular to it.
6. Points on the middle surface of the plate are displaced on a line normal to the initial non-deflected surface.
7. Stress normal to the middle surface is of negligible order. (This holds true as long as no high localized forces are applied to the plate.)
8. No strain of the middle surface needs to be considered. (This holds true for small deflections under zero lateral load. But the basic theory can be extended in a simple approach for pre-stressed plates as presented in Section 3.1.5.)

C.1.2 Small deflections

Throughout this section the basic differential equation for small static deflections of plates according to the theory of *Kirchhoff* and *Love* will be derived. The description is kept short and illustrative (for a more detailed derivation please see [Tim87], [Szi74] or [Rei88]).

The basic idea of the theory is to describe the deformation of the three dimensional plate only by the deflection of a two dimensional middle surface. To do this the assumptions listed in Section C.1.1 are applied. The middle surface is represented by w and is a function of the coordinates x and y (or r and φ in case of cylindrical plates).

The solution of a mechanical problem is based on the knowledge about four parts of the problem:

1. material law
2. kinematic relationships
3. equations of equilibrium
4. boundary conditions

material law

The material law relates load to deformation that is stress and strain. Based on assumption 1 of Section C.1.1 and phenomenological observations it is found that it takes a stress σ_i (force per unit area) in direction i to achieve a unit elongation ϵ_i ($= \Delta l/l_0$ elongation per unit length) into the same direction i . Stress and elongation relate linearly (*Hooké's law*).

$$\sigma_i = E \epsilon_i$$

$$\epsilon_i = \frac{1}{E} \sigma_i$$

where E denotes the *Young's* modulus. This relation is found if all other faces normal to i are allowed to move freely. Furthermore it is observed that the strained material contracts perpendicular to the direction of stress proportional to *Poisson's* ratio ν :

$$\epsilon_j = -\frac{\nu}{E} \sigma_i.$$

By means of superposition the whole set of *Hooké's* law equations can be derived. All stresses normal to the plate surface vanish (plane stress) if the law is applied to plates which are only supported along the edge and which are thin compared to their diameter. The material law in its final form is found:

$$\begin{aligned}\epsilon_x &= \frac{1}{E}(\sigma_x - \nu \sigma_y) \\ \epsilon_y &= \frac{1}{E}(\sigma_y - \nu \sigma_x) \\ \epsilon_z &= -\frac{\nu}{E}(\sigma_x + \sigma_y) \\ \epsilon_{xy} &= \frac{1}{2G} \sigma_{xy} \\ \epsilon_{xz} &= \epsilon_{yz} = 0\end{aligned}$$

where

$$G = \frac{E}{2(1 + \nu)} \quad (\text{C.1})$$

denotes the shear modulus. Solving these equations for the stress components yields

$$\begin{aligned}\sigma_x &= \frac{E}{1 - \nu^2}(\epsilon_x + \nu \epsilon_y) \\ \sigma_y &= \frac{E}{1 - \nu^2}(\epsilon_y + \nu \epsilon_x) \\ \sigma_z &= 0 \\ \sigma_{xy} &= 2G \epsilon_{xy} \\ \sigma_{xz} &= \sigma_{yz} = 0.\end{aligned} \quad (\text{C.2})$$

For calculations in polar coordinates these equations change to

$$\begin{aligned}\epsilon_r &= \frac{1}{E}(\sigma_r - \nu \sigma_t) \\ \epsilon_t &= \frac{1}{E}(\sigma_t - \nu \sigma_r) \\ \epsilon_z &= -\frac{\nu}{E}(\sigma_r + \sigma_t) \\ \epsilon_{rt} &= \frac{1}{2G}\sigma_{rt} \\ \epsilon_{rz} &= \epsilon_{tz} = 0\end{aligned}$$

and

$$\begin{aligned}\sigma_r &= \frac{E}{1-\nu^2}(\epsilon_r + \nu \epsilon_t) \\ \sigma_t &= \frac{E}{1-\nu^2}(\epsilon_t + \nu \epsilon_r) \\ \sigma_z &= 0 \\ \sigma_{rt} &= 2G \epsilon_{rt} \\ \sigma_{rz} &= \sigma_{tz} = 0,\end{aligned}\tag{C.3}$$

where index t denotes the transverse coordinate (i.e. φ for polar coordinates). No transverse shear forces need to be considered as long as the thickness of the plate remains small compared to its smallest lateral dimension. That is, in compliance with 1, 5, and 7 of Section C.1.1 σ_{rt} and σ_{tz} vanish.

kinematic relationships

The kinematic relationships describe the geometric deformation of a body in terms of the resulting strain. The relations have to be in compliance with the assumptions 2, 5, 6, 7, and 8 of Section C.1.1. They are derived here for cartesian coordinates first and are in a second step transformed illustratively into the proper form applicable for plates of rotational symmetry.

The z is always measured from the middle surface w positively into the downward direction. It can be concluded by considering the cross-section along the x -axis of a rectangular piece cut out of a plate as depicted in Fig. C.1, that

$$\begin{aligned}\epsilon_x &= \frac{d(x_0 + \Delta x)}{dx} = \frac{d\Delta x}{dx} = -\frac{d(w_{,x} z)}{dx} \\ \epsilon_x &= -w_{,xx} z = \frac{1}{r_x} z\end{aligned}$$

holds, where $w_{,x}$ denotes a partial derivative of w with respect to x . Further follows

$$\epsilon_y = -w_{,yy} z = \frac{1}{r_y} z$$

by considering symmetry. These equations relate the strain in the plate to its curvatures r_x and r_y . They are valid for any independent pair of curvatures, that is the

centers of these curvatures need to be on a straight line and the curvatures must be perpendicular to each other at the same time. The given kinematic can be trans-

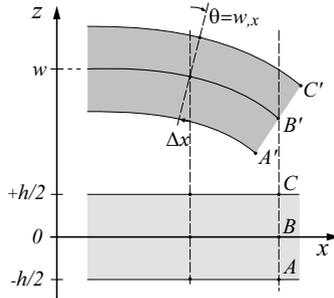


Fig. C.1: Kinematic relations of a plate. Cross-section along the x-axis.

formed with this consideration for the case of circular plates. This is done straightforward for the radial coordinate giving

$$\frac{1}{r_r} = -w_{,rr}.$$

The second independent curvature is found if Fig. C.2 is observed. It can be noted, that

$$\frac{1}{r_t} = \frac{1}{CB} = \frac{1}{r} \sin(\Theta) = -\frac{1}{r} w_{,r}$$

holds and the kinematic relations for circular plates become

$$\begin{aligned} \epsilon_r &= \frac{1}{r_r} z = -w_{,rr} z \\ \epsilon_t &= \frac{1}{r_t} z = -\frac{1}{r} w_{,r} z. \end{aligned} \tag{C.4}$$

It is now possible to express the strains in (C.3) in terms of the plate curvatures giving

$$\begin{aligned} \sigma_r &= \frac{Ez}{1-\nu^2} \left(\frac{1}{r_r} + \nu \frac{1}{r_t} \right) = -\frac{Ez}{1-\nu^2} \left(w_{,rr} + \nu \frac{1}{r} w_{,r} \right) \\ \sigma_t &= \frac{Ez}{1-\nu^2} \left(\frac{1}{r_t} + \nu \frac{1}{r_r} \right) = -\frac{Ez}{1-\nu^2} \left(\frac{1}{r} w_{,r} + \nu w_{,rr} \right). \end{aligned} \tag{C.5}$$

Equilibrium equations must be derived in compliance with the basic assumptions of Section C.1.1. The Kirchhoff-Love plate theory regards the middle surface w to be free of stress. Furthermore, only bending moments act on the middle surface and cause the deformation. All stresses parallel to this surface (membrane stress)

equilibrium equations

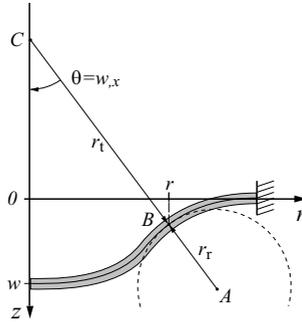


Fig. C.2: Radii of curvature r_r and r_t of a plate with circular symmetry (radial cross-section).

and shearing forces are considered small and are therefore neglected. The special kinematic as chosen above in (C.4) ensures vanishing of these neglected loads. It describes a deformation by considering solely symmetric bending about the middle surface. This approach is useful if the deflection of plates with medium thickness (see C.1.1) need to be modeled. For thicker plates shearing forces must be included. For thinner ones most of the energy is stored in lateral strain which can not be neglected anymore and the plate is referred to in the extreme case as a membrane.

All moments acting on the middle surface (moments from the clamped boundary m_r, m_t) and the forces perpendicular to the surface have to be in equilibrium. The force of the surface load q on a cylindrical part cut out of the plate according to Fig. C.3 is balanced by a shear force Q (force per unit length, $[Q] = \text{N/m}$) acting along the boundary of it. Q is defined per unit length for a pressure load parallel to the z -axis as

$$2\pi r Q = \int_0^r \int_0^{2\pi} q \tilde{r} d\varphi d\tilde{r}.$$

In the special case of a uniform and symmetric pressure load p the shear force becomes

$$Q = \frac{p}{2} r. \quad (\text{C.6})$$

The bending moments are acting on the middle surface of the considered plate

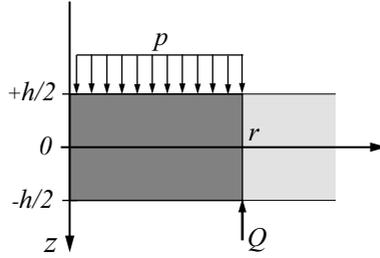


Fig. C.3: Equilibrium of the forces perpendicular to the surface of the plate.

part and are defined per unit length:

$$\begin{aligned}
 m_r &= \int_{-h/2}^{h/2} \sigma_r z \, dz = -\frac{E}{(1-\nu^2)} \left(w_{,rr} + \nu \frac{1}{r} w_{,r} \right) \int_{-h/2}^{h/2} z^2 \, dz \\
 &= -D \left(w_{,rr} + \nu \frac{1}{r} w_{,r} \right)
 \end{aligned}$$

where

$$D = \frac{E h^3}{12(1-\nu^2)} \tag{C.7}$$

denotes the flexural rigidity. The transverse moments per unit length are found in analogy. All moments acting on the middle surface can be expressed in terms of its curvature yielding

$$\begin{aligned}
 m_r &= -D \left(w_{,rr} + \nu \frac{1}{r} w_{,r} \right) = D \left(\frac{1}{r_r} + \nu \frac{1}{r_t} \right) \\
 m_t &= -D \left(\frac{1}{r} w_{,r} + \nu w_{,rr} \right) = D \left(\frac{1}{r_t} + \nu \frac{1}{r_r} \right).
 \end{aligned} \tag{C.8}$$

These moments, the moments caused by pressure load p , and the shear force Q act on the plate part as illustrated in Fig. C.4 and must be in equilibrium. The equilibrium equation reads

$$\begin{aligned}
 0 &= m_r \, r \, d\varphi - (m_r + m_{r,r} \, dr)(r + dr) \, d\varphi - \\
 &\quad \frac{dr}{2} \, r \, Q \, d\varphi - \frac{dr}{2} (Q + Q_{,r} \, dr)(r + dr) \, d\varphi + \\
 &\quad m_t \, dr \, d\varphi
 \end{aligned}$$

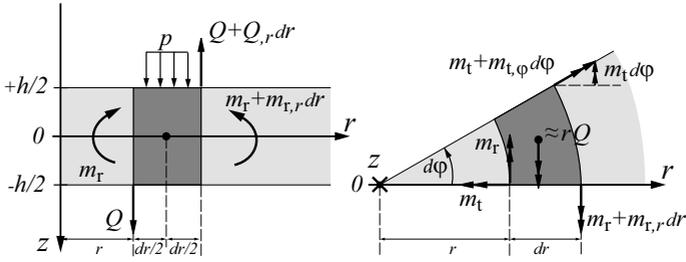


Fig. C.4: Equilibrium of the bending moments acting along the boundary of a plate part.

and can be boiled down to

$$\frac{1}{r}(m_t - m_r - r m_{r,r}) = Q \tag{C.9}$$

by differentiating with respect to φ and by neglecting all terms smaller than $\mathcal{O}(dr)$. The differential equation for the middle surface of the plate is then found by expressing all moments in (C.9) with the relations (C.8). Algebraic manipulations gives

$$\left[\frac{1}{r}(r w_{,r})_{,r} \right]_{,r} = \frac{Q}{D}. \tag{C.10}$$

The shear force Q can be expressed in terms of the applied surface load. This is achieved for a symmetrical uniform load by using (C.6) yielding

$$\frac{1}{r} \left[r \left(\frac{1}{r}(r w_{,r})_{,r} \right)_{,r} \right]_{,r} = \frac{p}{D} \tag{C.11}$$

after taking the derivative with respect to r . Differential equation (C.11) can be integrated directly requiring four boundary conditions. The extra derivative is not necessary if the plate can deflect freely and the uniform load extends about the whole surface. Three boundary conditions can be found in such a case and are sufficient for the solution as demonstrated in Section 3.1.2 and Section 3.1.3. In cases where the load does not extend over the whole surface, an additional boundary condition is necessary for shear force Q and the fourth order differential equation (C.11) must be used. Such a situation occurs e.g. when the plate touches the counter electrode (see Section 3.1.4).

(C.10) and (C.11) can be easily integrated in the presented form. However, in literature often an equivalent expression using the nabla operator can be found. Nabla reads for polar coordinates and angular symmetry as

$$\nabla_r^4 = \Delta_r \Delta_r = \partial_r^4 + \frac{2}{r} \partial_r^3 - \frac{1}{r^2} \partial_r^2 + \frac{1}{r^3} \partial_r$$

and (C.11) changes to

$$\nabla_r^4 w = \frac{p}{D}. \quad (\text{C.12})$$

A normalization of all variables is introduced in sec 3.1.1 which reflects the transducer geometry and simplifies the formulas. Capital letters indicate normalized quantities, e.g. radius r and deflection w are expressed with R and W which run from zero to unity and are scaled with the plate radius r_{\max} and gap height w_{\max} :

$$\begin{aligned} r &= r_{\max} R & R &= 0 \dots 1, & r_{\max} &= \text{plate radius} \\ w &= w_{\max} W & W &= 0 \dots 1, & w_{\max} &= \text{center deflection.} \end{aligned} \quad (\text{C.13})$$

The full set of dimensionless quantities is summarized in Tab. 3.1. Equation (C.10) changes to

$$\left[\frac{1}{R} (RW, R), R \right]_{,R} = \frac{Q r_{\max}^3}{D w_{\max}} \quad (\text{C.14})$$

and integration yields

$$W = P R^4 + \frac{C_1}{4} R^2 + C_2 \ln R + C_3 \quad (\text{C.15})$$

where P denotes the normalized pressure load

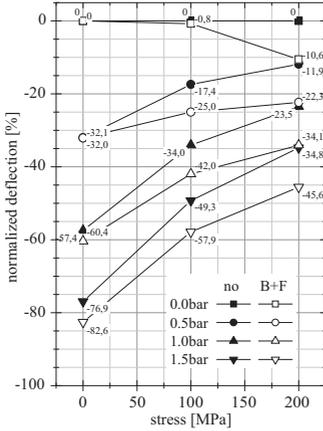
$$P = \frac{p}{p_t} \quad \text{with} \quad p_t = \frac{64 D w_{\max}}{r_{\max}^4}. \quad (\text{C.16})$$

p_t is the touch-down pressure of the rigidly clamped plate as demonstrated in Section 3.1.2. Therefore, the normalized pressure load P and deflection W are unity at plate touch-down. Applying the same normalization to (C.11) yields

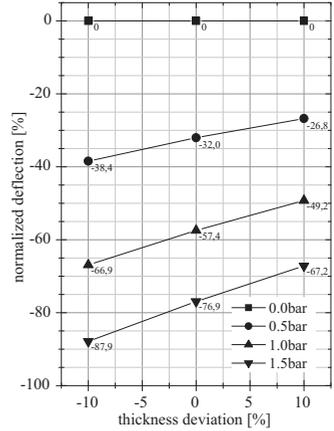
$$\frac{1}{R} \left[\frac{1}{R} (RW, R), R \right]_{,R} = 32 P \quad (\text{C.17})$$

which is the differential equation for the deflection as used throughout this work.

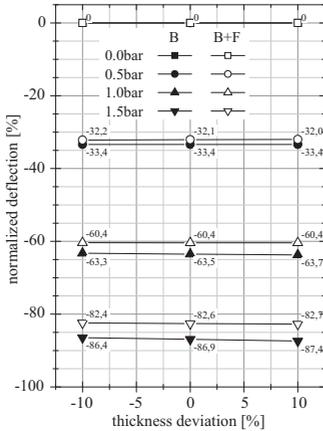
C.2 FEM modeling



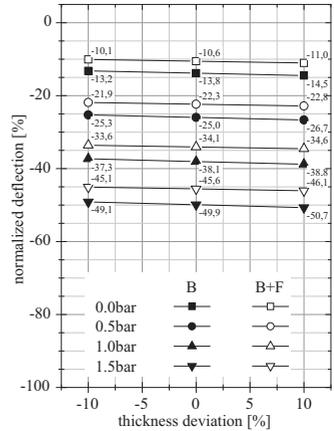
(a) impact of stress on plates with topography (with and without bottom-electrode feedthroughs)



(b) impact of plate thickness variation

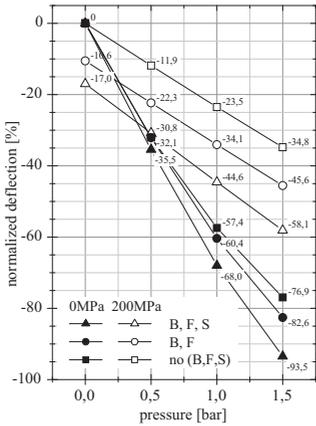


(c) impact of bottom-electrode thickness variation (at 0 MPa stress)

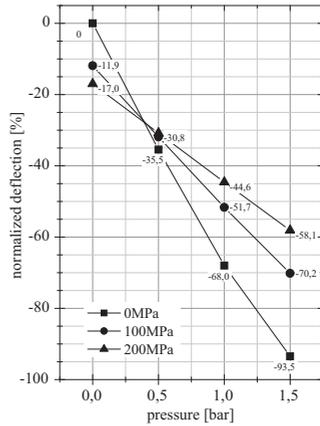


(d) impact of bottom-electrode thickness variation (at 200 MPa stress)

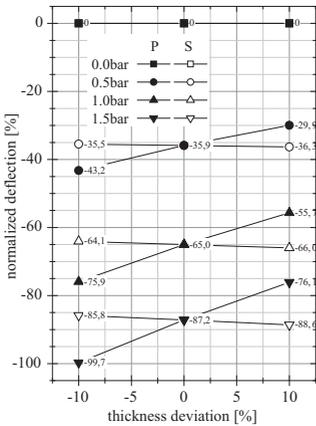
Fig. C.5: FEM simulation results for the center deflection of plates illustrating the mechanical influence of plate and bottom-electrode thickness variations (B: bottom-electrode, F: feedthrough, geometry of model @ presented in Fig. 3.9(c)).



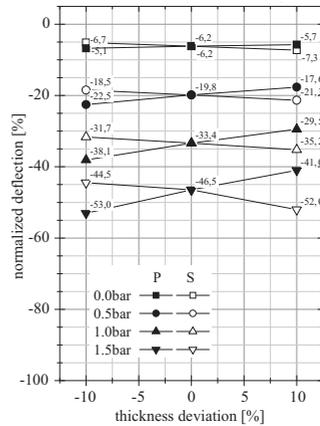
(a) impact of stress on plates with topography



(b) deflection of a plate with the topography of B, F, and S



(c) comparison of plate and sacrificial layer thickness variations (at 0 MPa stress)



(d) comparison of plate and sacrificial layer thickness variations (at 200 MPa stress)

Fig. C.6: FEM simulation results for the center deflection of plates illustrating the mechanical influence of plate and sacrificial layer thickness variations (P: plate, B: bottom-electrode, F: feedthrough, S: sacrificial layer, geometry of model ③ presented in Fig.3.9(c) having a sacrificial layer thickness of 1005 nm = 675 nm + 350 nm).

C.3 Sensor design and fabrication

C.3.1 Stress test standards

Table C.1: Summary of standards providing some additional background information on micro-system qualification.

standard	title/description
JEDEC JESD47E	<i>Stress-Test-Driven Qualification of Integrated Circuits</i> explanation of applicable tests, lot sizes, duration, acceptance criteria
JEDEC JESD74	<i>Early Life Failure Rate Calculation Procedure for Electronic Components</i>
JEDEC JESD91A	<i>Method for Developing Acceleration Models for Electronic Component Failure Mechanisms</i>
JEDEC JESD94	<i>Application Specific Qualification Using Knowledge Based Test Methodology</i> example calculations of test durations for some typical applications
JEDEC JEP70-B	<i>Quality and Reliability Standards and Publications</i> overview of existing JEDEC standards
JEDEC JEP122C	<i>Failure Mechanisms and Models for Semiconductor Devices</i> explanations of existing failures and appropriate models
JEDEC JEP148	<i>Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment</i>
JEDEC JEP149	<i>Application thermal derating methodologies</i> explanation of thermal derating strategies
ISO ISO 2281	<i>Horology water-resistant watches</i> definition of test-conditions for water-resistant watches

C.3.2 Alignment rules

Table C.2: Alignment rules for the presented sensor process.

layer	function	aligned to	comment
LA0	alignment keys	flat	alignment is not demanding
LA1	bottom-electrode	LA0	precision required, alignment deviations influence the sensor cell geometry
LA2	sacrificial layer	LA0	precision required, alignment deviations influence the sensor cell geometry
LA3	etch channels	LA0	precision required, alignment deviations influence the sensor cell geometry
LA4	membrane	LA3	the proceeding RIE step requires a precise alignment to LA3
LA5	contact	LA0	this mask can be used to either pattern a LA2 or a LA6 hard mask
LA6	vacuum seal	LA4	precise alignment required for accurate cavity sealing
LA7	metallization	LA0	alignment is not demanding
LA8	reinforcement	LA0	alignment is not demanding

C.4 Electric sensor model

C.4.1 Lorentz oscillator

The dielectric properties of silicon oxide a silicon nitride can be approximated with a Lorentz oscillator model:

$$\varepsilon = 1 + \frac{Nq^2}{\varepsilon_0} \frac{1}{\omega_0^2 - \omega^2 - i\beta_a\omega} = \varepsilon' + i\varepsilon'' \quad (\text{C.18})$$

where N denotes the number of molecules per unit volume, q the elementary charge, ε_0 the permittivity of space, β_a the attenuation, and ω_0 the frequency of maximum dissipation (maximum of ε''). This results in the optical constants

$$n = \sqrt{\frac{\sqrt{\varepsilon'^2 + \varepsilon''^2} + \varepsilon'}{2}} \quad k = \sqrt{\frac{\sqrt{\varepsilon'^2 + \varepsilon''^2} - \varepsilon'}{2}} \quad (\text{C.19})$$

The real and complex part of ε can be calculated from optical measurement of refraction index n and dissipation coefficient k with

$$\varepsilon' = n^2 - k^2 \quad \varepsilon'' = 2nk \quad (\text{C.20})$$

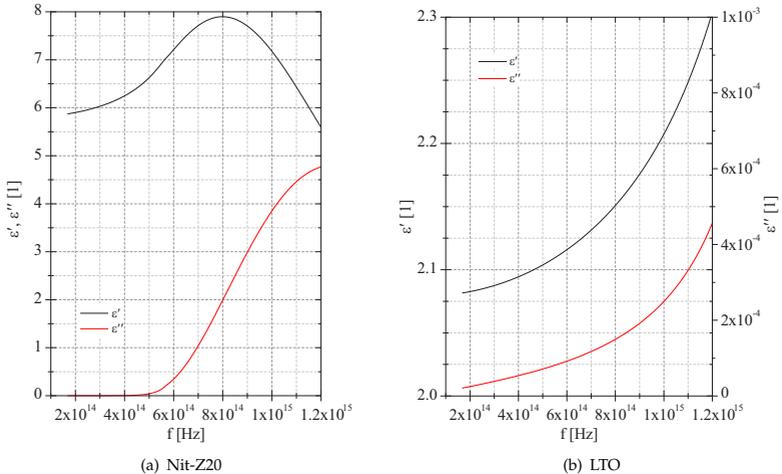


Fig. C.7: Dielectric properties of Nit-Z20 and LTO. (Real and imaginary part of the permittivity calculated with (C.20) from Woollam M-2000 spectroscopic ellipsometry data.

C.4.2 Electrical measurements

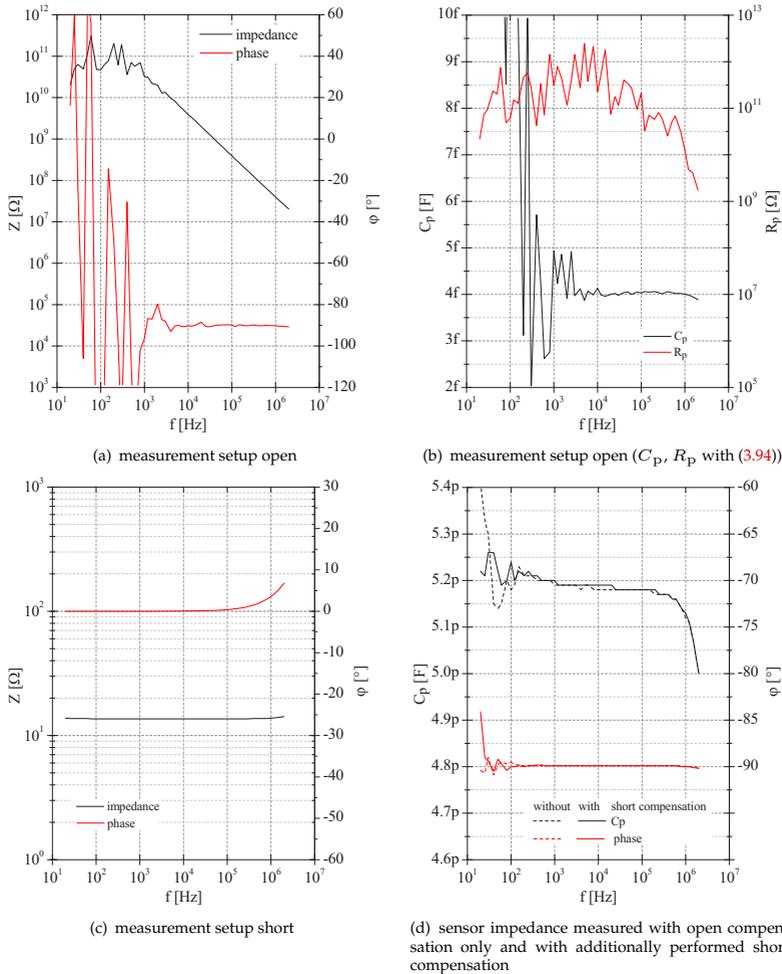


Fig. C.8: Impedance of the measurement setup used for all given *Bode*-plots of this work (*Agilent E4980A Precision LCR meter* in four terminal pair configuration and quasi *Kelvin* contacts). The graphs depict the setup's impedance with open and shortened contacts. The negligible impact of short compensation is demonstrated with a *Design-2* sensor. See Fig. 3.65(b) for an illustration of the electrical wiring.

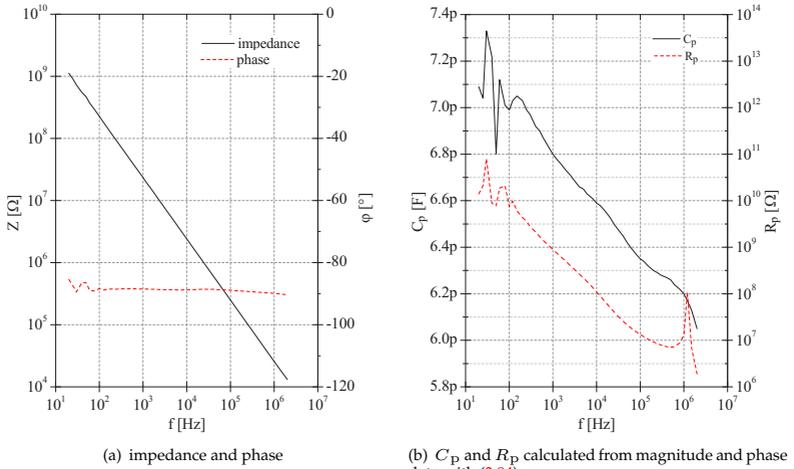


Fig. C.9: Impedance of a capacitor having a 1f-PECVD oxide dielectric. The test structure was fabricated on a fused silica substrate with two counter electrodes made of Cr/Au. The capacitor had no metal/semiconductor interfaces and was measured on wafer-level with an *Agilent E4980A Precision LCR meter* with two quasi *Kelvin* contacts in four terminal pair configuration (see Fig. 3.65(b) for a schematic of the measurement setup).

C.4.3 Series resistance correction

Impedance data acquired as parallel resistance R_p and parallel capacitance C_p can be correct for the influence of a series resistance R_s with [Nic82]:

$$C_p^{(\text{corrected})} = \frac{R_p^{-2} + \omega^2 C_p^2}{a^2 + \omega^2 C_p^2} C_p$$

$$R_p^{(\text{corrected})} = \frac{a^2 + \omega^2 C_p^2}{a(R_p^{-2} + \omega^2 C_p^2)}$$

$$a = R_p^{-1} - (R_p^{-2} + \omega^2 C_p^2) R_s.$$

This set of correction functions also provides the frequency response of R_p and C_p relevant for some readouts concepts.

C.4.4 Equivalent circuit

The electrical sensor characteristics can be modeled with a simplified lumped components equivalent circuits as depicted in Fig. 3.60 and discussed in Section 3.4.2.

The Average series resistance R_{s1t} of the sensor top-electrode can be approximated with

$$R_{s1t} = \left(\frac{3}{16} + 2\frac{3}{16} + 3\frac{3}{16} + 4\frac{3}{16} + 5\frac{3}{16} + \frac{1}{16} \right) \frac{2}{6} R_{\square\text{top}} = \frac{92}{96} R_{\square\text{top}},$$

where $R_{\square\text{top}}$ denotes the top-poly resistance in ohms per square. The remaining lumped components are given by

$$C_{p4} = 5C_{ps} + 11C_{pi} + 3C_{po}$$

$$R_{p4} = \frac{1}{5}R_{ps} + \frac{1}{11}R_{pi} + \frac{1}{3}R_{po}$$

$$R_{s4} = \frac{1}{19}R_{si}$$

$$C_{p3} = 38C_{pi}$$

$$R_{p3} = \frac{1}{38}R_{pi}$$

$$R_{s3} = \frac{1}{19}R_{si}$$

$$C_{p2} = 11C_{ps} + 22C_{pi} + 2C_{po}$$

$$R_{p2} = \frac{1}{11}R_{ps} + \frac{1}{22}R_{pi} + \frac{1}{2}R_{po}$$

$$R_{s2} = \frac{1}{25}R_{si}$$

$$C_{p1} = 25C_{pi} + 25C_{po}$$

$$R_{p1} = \frac{1}{25}R_{pi} + \frac{1}{25}R_{po}$$

$$R_{s1} = \frac{1}{25}R_{so}.$$

C.5 Basic theory of MIS structures

This section briefly summarizes the formulas which were used to fit the CV data presented in Section 3.4.1. CV measurements are very common and many parameters of the semiconductor, the insulator, and their interface can be deduced. However, the assembly of the required equations was time consuming and is therefore summarized briefly. The interpretation of the CV data presented in Fig. 3.57 and Fig. 3.58 of Section 3.4.1 is based on the following equations and the parameters summarized in Tab. C.3

1. CV-curve plotting:

The overall device capacitance c per unit area is the series circuit of the insulator capacitance per unit area c_i (C.31) and the depletion layer capacitance per unit area c_{Si} (C.25)

$$c = \frac{c_i c_{Si}}{c_i + c_{Si}}. \quad (\text{C.21})$$

Capacitance c is plotted versus the gate voltage

$$V_g = -\frac{q_s + q_i}{c_i} - V_t(U_b - U_s) + V_{ms}, \quad (\text{C.22})$$

which is influenced by the work function difference V_{ms} (C.29), i.e. the contact metal choice, and the charge density q_i (C.30) per unit area within the insulator.

An applied external voltage between gate metal and silicon bulk leads to band bending ψ_s at the semiconductor surface, which gives rise to a surface potential U_s (dimensionless), which creates a surface charge q_s (C.27), and determines the depletion layer capacitance c_{Si} . Therefore, all the following potentials and fields can be expressed in terms of the band bending ψ_s . Its magnitude must be swept to calculate pairs of c and V_g which can be plotted as a CV-curve.

The temperature voltage V_t (C.32) and the dimensionless bulk potential U_b (C.28) in (C.22) are only dependent on the operation temperature and do not change with applied voltage.

2. Surface band bending ψ_s and derived quantities:

ψ_s denotes the band bending at the surface of the semiconductor. It determines the dimensionless surface potential [Nic82, p. 51]

$$U_s = \frac{\psi_s}{V_t} + U_b, \quad (\text{C.23})$$

where U_b denotes the dimensionless bulk potential (C.28). The band bending is accompanied by an electric field within the semiconductor which can be

expressed in the dimensionless form [Nic82, p. 56]

$$F = \sqrt{2} \sqrt{(U_b - U_s) \sinh U_b - (\cosh U_b - \cosh U_s)}. \quad (\text{C.24})$$

The deformation of the bands in turn determine the magnitude of the depletion layer capacitance

$$c_{\text{Si}} = \text{sgn}(U_s - U_b) \frac{\epsilon_0 \epsilon_{\text{cSi}}}{\lambda_i} \frac{\sinh U_s - \sinh U_b}{F}, \quad (\text{C.25})$$

where λ_i denotes the intrinsic *Debye* length (C.33). The electric field at the semiconductor surface equates to [Nic82, p. 56]

$$f_s = \text{sgn}(U_B - U_s) \frac{kT}{q \lambda_i} F \quad (\text{C.26})$$

and can be used to calculate the built up surface charge at the Si insulator interface

$$q_s = \epsilon_0 \epsilon_{\text{cSi}} f_s, \quad (\text{C.27})$$

which is required to finally compute the gate voltage (C.22).

Table C.3: Summary of CV measurement fitting input variables.

Symbol	Value	Unit	Quantity
T	300	K	ambient temperature
N_D	0	m^{-3}	donor impurity concentration
N_A	$(0.1 \dots 3) \times 10^{22}$	m^{-2}	acceptor impurity concentration
d_{iso}	$0 \dots 100 \times 10^{-9}$	m	insulator thickness
ϵ_{iso}	0 ... 8	1	insulator permittivity
A^{metal}	7.7124×10^{-8}	m^2	metal area
V_{ms}	$-0.95 \dots -0.98$	V	work function difference (Al on p-Si)
N_Q	$0 \dots 1 \times 10^{-15}$	m^{-2}	surface charge density

3. Additional basic equations:

- dimensionless bulk potential [Nic82, p. 51]

$$U_b = \frac{E_F}{q V_t}, \quad (\text{C.28})$$

where E_F denotes the intrinsic *Fermi* level according to (C.37).

- work function difference [Nic82, p. 465]

$$V_{ms} = \frac{\phi_m - \phi_{Si}}{q} \quad (C.29)$$

Al on p-Si with a dopant level of $N_A = 10^{16} \text{ cm}^{-3} \dots 4 \times 10^{16} \text{ cm}^{-3}$ causes a work function difference of -0.9 V [Nic82, p. 466].

- insulator surface charge per unit area

$$q_i = q N_Q. \quad (C.30)$$

q_i sums up all charges incorporated within the insulation layer and N_Q denotes the surface charge density.

- insulator capacitance per unit area

$$c_i = \frac{\epsilon_0 \epsilon_i}{t_i} \quad (C.31)$$

- temperature voltage

$$V_t = \frac{kT}{q} \quad (C.32)$$

- intrinsic Debye length

$$\lambda_i = \sqrt{\frac{\epsilon_0 \epsilon_{cSi} kT}{2q^2 n_i}} \quad (C.33)$$

- silicon band gap [Sze81, p. 15]

$$E_g = \left[E_{g0} - \frac{\alpha_{Si} T^2}{T + 636 \text{ K}} \right] q \quad (C.34)$$

$$\text{with } \alpha_{Si} = \frac{dE_g}{dT} = 4.73 \times 10^{-4} \text{ eV/K}$$

- number of effective states per unit volume per energy [Nic82, p. 34]

$$N_c = 12 \left[\frac{2\pi m_n kT}{h^2} \right]^{\frac{3}{2}} \quad (C.35)$$

$$N_v = 2 \left[\frac{2\pi m_p kT}{h^2} \right]^{\frac{3}{2}}$$

- intrinsic carrier density per unit volume (with correction $\gamma_i = 3$ based

on experimental data) [Nic82, p. 35]

$$n_i = \gamma_i \sqrt{N_v N_c} \exp \left[-\frac{E_g}{2 k T} \right] \quad (\text{C.36})$$

- extrinsic *Fermi* level measured relative to the intrinsic level

$$E_F = \text{sgn}(N_D - N_A) k T \times \left[\text{sgn}(N_D - N_A) \frac{N_D - N_A}{n_i} + \frac{n_i}{N_D - N_A} \right] \quad (\text{C.37})$$

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